FAA TECHNICAL CENTER LETTER REPORT

AIRCRAFT REPLY AND INTERFERENCE ENVIRONMENT SIMULATOR

DESIGN DATA AND FABRICATION PLAN

by

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1.0 INTRODUCTION.

The Aircraft Reply and Interference Environment Simulator (ARIES) is a special purpose capacity simulator that will have the ability to simulate a heavy target and fruit environment for a Mode S sensor. This capability will initially be used during factory acceptance testing of the production Mode S sensors where the ARIES will be used to verify that the contractor has met the sensor's target capacity and loading requirements.

A summary of the key ARIES features is given in Section 2.0. This is followed by a detailed functional description of the hardware configuration, Section 3.0, and of the software configuration, Section 4.0. Finally a summary on the approach that will be taken in the fabrication of the ARIES is given in Section 5.0.

2.0 FUNCTIONAL CAPABILITIES.

2.1 TARGET AND FRUIT SIMULATION.

The ARIES system will simulate an ensemble of fruit and modeled replies. Up to 50,000 ATCRBS fruit replies per second will be generated within increments of 1,000 fruit replies per second. Up to 500 Mode S fruit replies per second will be generated within increments of 10 replies per second. Up to a total 700 aircraft consisting of any mix of Mode S and ATCRBS will be simulated. In addition ARIES will provide digital radar reports to any of the Mode S sensor's primary interfaces based on the model file.

2.2 ARIES EXTERNAL INTERFACES.

The ARIES unit will be designed to receive coupled RF signals out of the sensor after they have passed through the sensor's transmitter. The simulated transponder replies generated by the ARIES will be provided for the sum, delta, and omni antenna channels. These signals will be provided to the sensor's ARIES reply interface at 1090 MHz. The ARIES will also be capable of providing simulated radar data to any of the Mode S sensor's primary digital radar interfaces. In order to establish an antenna azimuth reference the ARIES will receive azimuth change pulses (ACPs) and azimuth reference pulses (ARPs) from the Mode S antenna system. The ARIES will also monitor the sensor's front/back signal to enable it to operate with the back-to-back Mode S Antenna configuration. The Mode S sensor's time-of-year clock data will be received for the purpose of synchronizing data extraction between the Mode S sensor and the ARIES unit.

2.3 SUMMARY OF TECHNICAL SPECIFICATIONS.

See table 2.1.

3.0 HARDWARE CONFIGURATION.

3.1 OVERALL HARDWARE DESCRIPTION.

Figure 3.1 is an overall block diagram of the ARIES hardware, illustrating also the interfaces to the Mode S sensor, the Mode S antenna, and the remote ARIES units. A single ARIES system is confined within the dotted lines of the figure.

TABLE 2.1 SUMMARY OF ARIES CAPABILITIES

* Uplink Interrogations
  * Non-discrete
    * Standard ATCRBS mode 2, 3/A and C.
    * ATCRBS-Only All Calls, mode 3/A and C.
    * ATCRBS/Mode S all Call, mode 3/A and C.
  * Discrete
    * Mode S short message.
    * Mode S long messages.
  * Receipt of Comm-A messages.
  * Ground initiated Comm-B messages.
  * Pilot initiated Comm-B messages.
  * Support both uplink and downlink ELM protocals.
  * Deterministic traffic models.
  * 700 Target Capacity (of any beacon mix)
    * Up to three simultaneous sychronous garbled replies.
    * Target range from 1 and 255 nautical miles.
  * Beacon fruit generation
    * Parameters defined per sector basis (11.25 degrees).
    * ATCRBS fruit rate: 0 to 50,000 per second (increments 1000).
    * Mode S fruit rate: 0 to 500 per second (increments 10).
  * RF interface with sensor transmitter.
  * RF interface with sensor receiver.
  * Support Back-to-back antenna operation.
  * Operation with or without antenna.
  * Five types of primary radar simulated.
  * Built in self checking.
  * Data extraction.
  * Multisite operations.

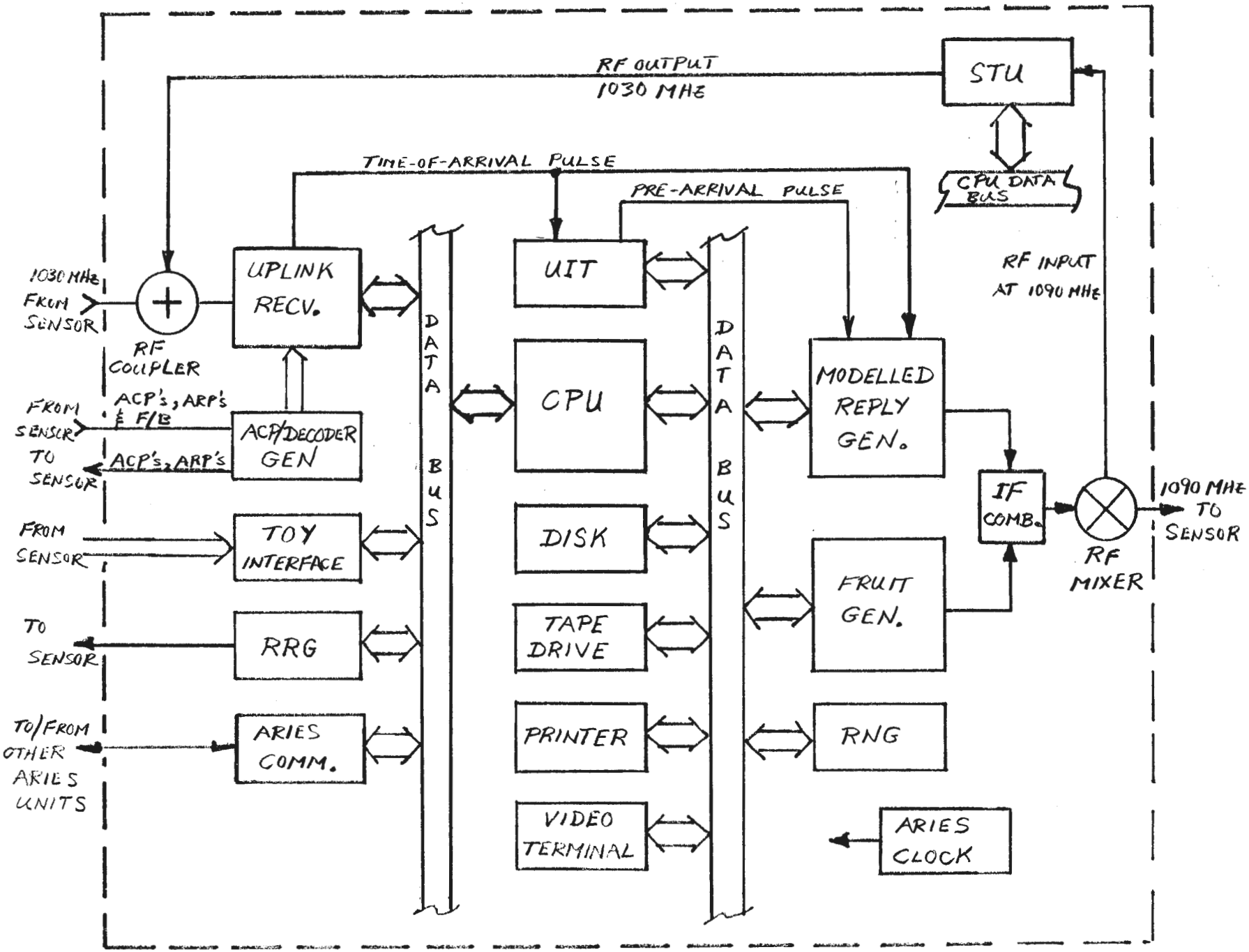


FIGURE 3.1. ARIES FUNCTIONAL BLOCK DIAGRAM

The heart of the ARIES system is a 32-bit computer with two Megabytes of random access memory and with high speed input/output (I/O) interface capability. Peripherals include a video display terminal with keyboard for providing operator communications, a disk unit for storing the system programs and the ARIES predetermined traffic model file, a magnetic tape unit for recording test and diagnostic data, a line printer for generating program listings and data printouts, and a pair of standard communication modems for communicating with two other ARIES units.

The principal special devices connected to the ARIES computer will be the uplink receiver and the reply generators. Separate reply generators will be included for the modeled replies and the fruit replies. Other special devices will be the universal interrupt timer (UIT) used to predict the time of arrival of ATCRBS interrogations, the self test unit (STU) used to verify system operation at the radio frequency level, the ACP Decoder/Generator used to accept antenna azimuth information, the radar report generator (RRG) used to output digital radar reports on modeled targets, and an interface used to receive the sensor time-of-year (TOY) clock data for ARIES data recording. A more detailed functional description of these devices will be given in the following sections.

3.2 UPLINK RECEIVER/DEMODULATOR/DECODER.

The input to the ARIES receiver will be coupled from the Mode S sensor transmitter at 1030 MHz. The interrogation signal level received will be within -10 to -1 dBm. The analog circuitry of the ARIES receiver is presented on figure 3.2 As shown on figure 3.2 the Mode S interrogations will be fed through a 20 dB directional coupler prior to the 1030 MHz preselector. The purpose of the directional coupler is to provide an input port to receive interrogations generated by the ARIES self test unit. The preselector eliminates undesirable, out of band interference (image, spurious, etc.) before being fed to a radio frequency (RF) mixer. The RF mixer will modulate the 1030 MHz signal to 60 MHz using a local oscillator (LO) operating at 970 MHz. The 60 MHz signal then will be amplified and conditioned by the log amplifier to provide two output signals, a log video signal and a 60 MHz Intermediate Frequency (IF) signal. The log video will be demodulated by the threshold circuit generating the pulse amplitude modulation (PAM) demodulation signals compatable to standard transistor-to-transister logic (TTL). The 60 MHz IF signal will be decoded by the differential phase shift keying (DPSK) demodulator into a TTL compatable output signal that will contain the Mode S phase modulation information. Both of these signals will be sent to the digital circuitry of the ARIES uplink receiver.

The uplink receiver digital circuitry will decode and identify the following interrogation types:

Non-discrete interrogations

- Standard ATCRBS; mode 2, 3/A, and C (No P4 pulse)
- ATCRBS-Only All Call; mode 3/A and C (0.8 μs wide P4 pulse)
- ATCRBS/Mode S Call Call; mode 3/A and C (1.6 μs wide P4 pulse)

Discrete interrogations

- Mode S Short interrogation (56 bits)
- Mode S Long interrogation (112 bits)

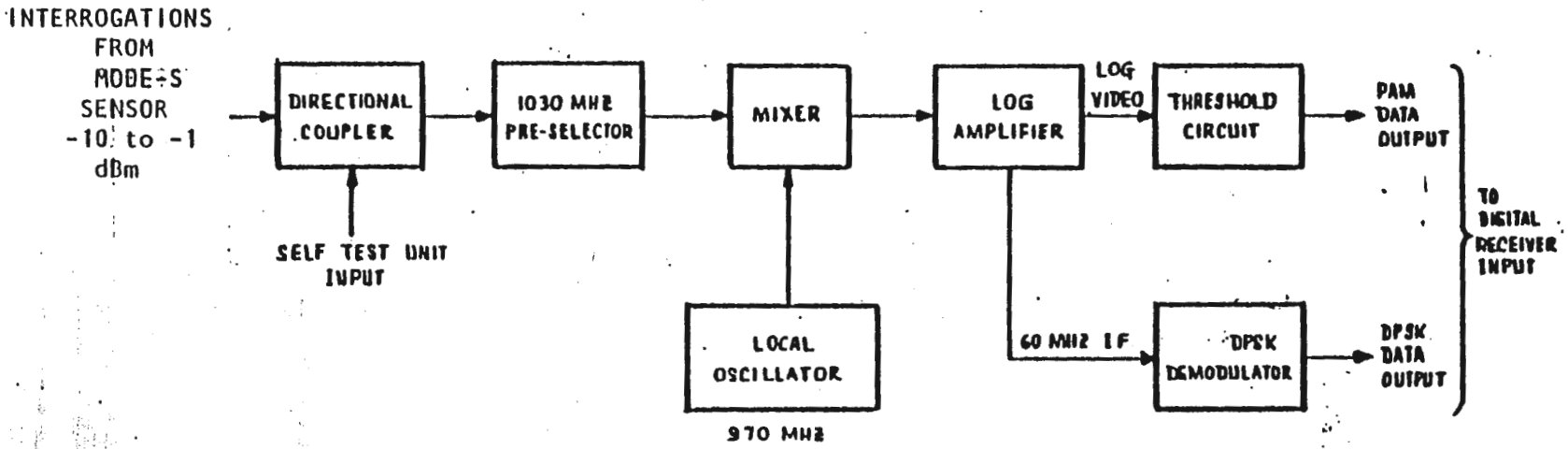


FIGURE 3.2. ANALOG RECEIVER, BLOCK DIAGRAM

A ten word data block will be assembled for each interrogation received and an interrupt will be generated to inform the ARIES computer of the arrival of an interrogation. This will allow the computer to prepare to receive a ten word interrogation data block using direct memory access (DMA) data transfer.

One of four types of interrogation data blocks will be generated depending on the interrogation received. The format of these data blocks is presented on figure 3.3. As shown on this figure each data block will contain the time of arrival of the interrogation with respect to the last non-discrete interrogation received, the type of interrogation received, which antenna it was received by, and the antenna boresight azimuth at the time the interrogation was received. When a Mode S interrogation is received the message field and the Mode S address field will be included.

As shown on figure 3.4 the uplink digital circuitry will consist of mode decoding logic, and for Mode S signals, a 24 bit parity decoder. Also, an azimuth register to accept a 14 bit azimuth work from the ACP Decoder/Generator unit discussed in Section 3.6 and a 20 bit clock register driven at 16 MHz will be included.

3.3 MODELED REPLY GENERATOR.

The Modeled Reply Generator (MRG) will simulate both ATCRBS (modes 2, 3/A, and C), and Mode S (short and long) replies as prepared by the ARIES computer. The computer software will generate any data pattern into a reply and transfer the reply to the MRG. The MRG will create properly formatted and sequenced modulation control signals for the reply generator analog circuitry. These control signals will consist of the reply range delay, power, target off boresight azimuth (monopulse) and reply content.

The major sections of the MRG depicted in figure 3.5, will be the modeled controller interface to the ARIES computer, a microprocessor controller, and three reply generators refered to as modeled ARIES targets (MATs). Each reply generator will be made up of digital circuitry and analog circuitry. Only the digital circuitry will be discussed in this section. The MATs analog circuitry is discussed in section 3.6.

The MRG interface will serve as a link between the ARIES computer and the microprocessor controller. The interface will provide buffer space for the CPU to store ATCRBS and Mode S reply message blocks as they are generated.

The microprocessor controller which is the heart of the MRG will determine (under microprogram control) if a reply block is available in the interface buffer, select which of the three MATs can accept the new reply block, and transfer the block to the available MAT.

The digital circuitry of the MAT, after being given reply data from the controller, will serially encode the reply data to create the pulse amplitude modulation (PAM) signal and the pulse position modulation (PPM) signal that will be sent to the MAT analog circuitry. Along with the modulation signals, the power, monopulse, boresight, and mainbeam/sidelobe information characterizing the reply will be past to the analog circuitry.

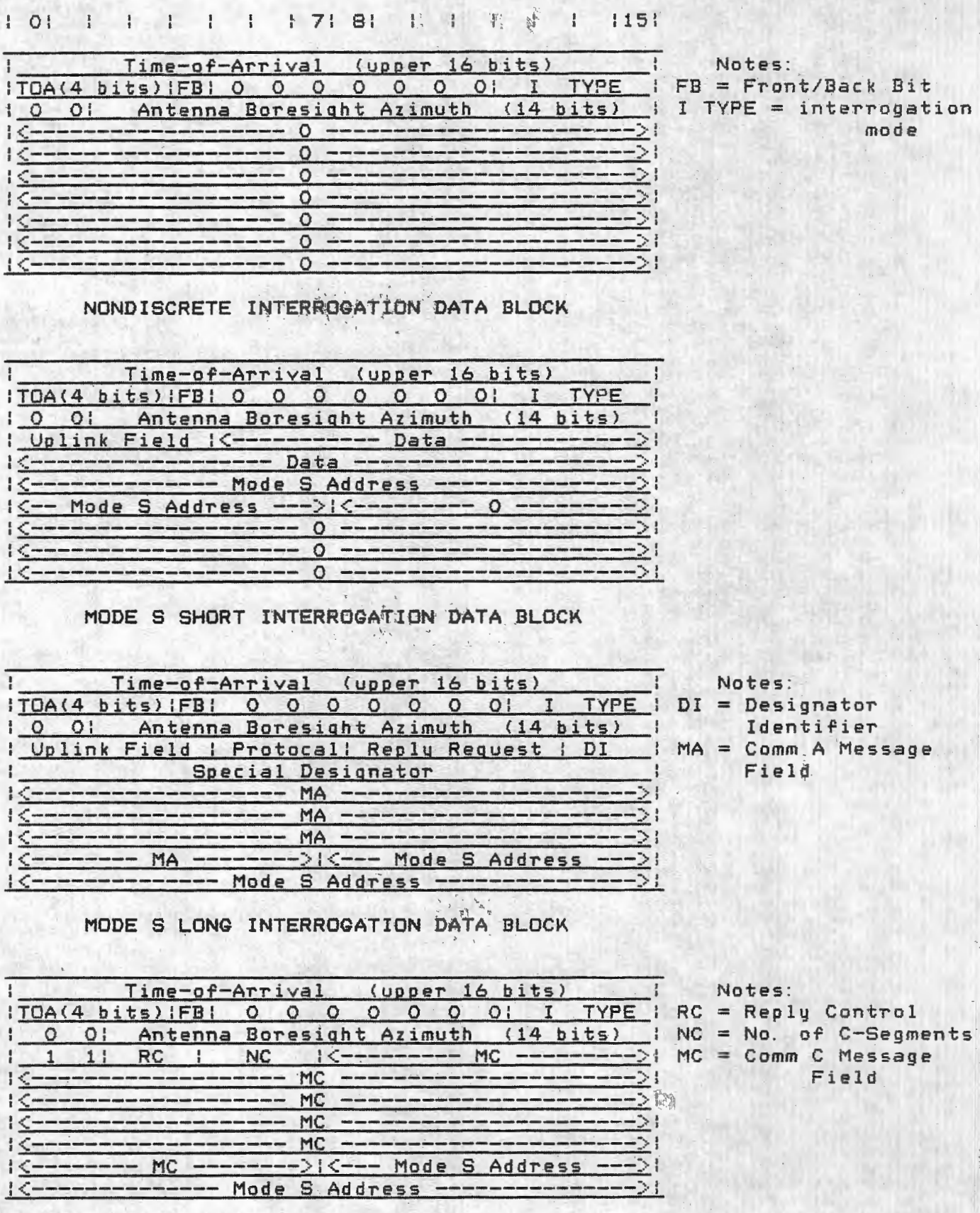


Figure 3.3. Uplink Reciever Interrogation Data Block Formats

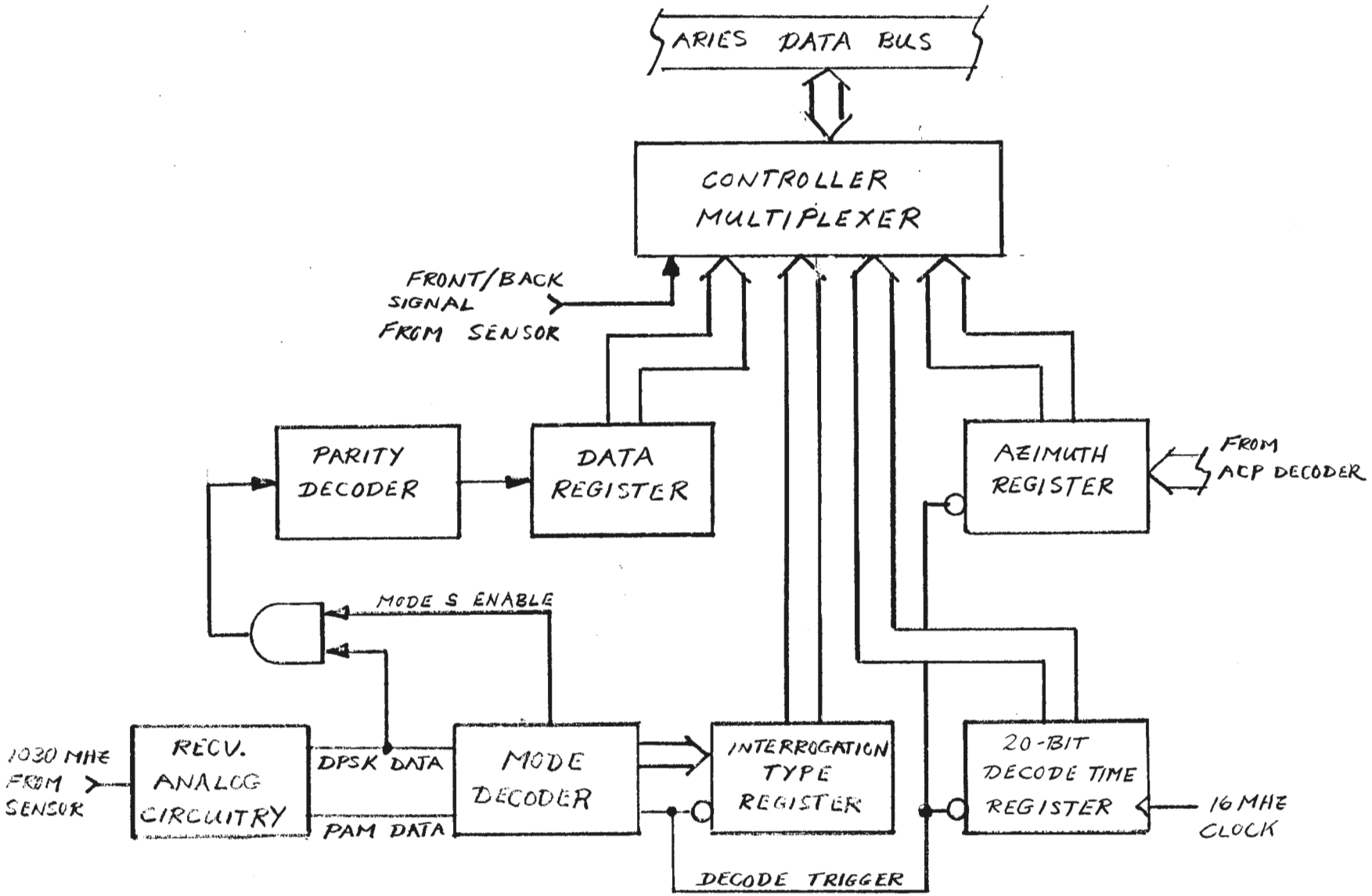
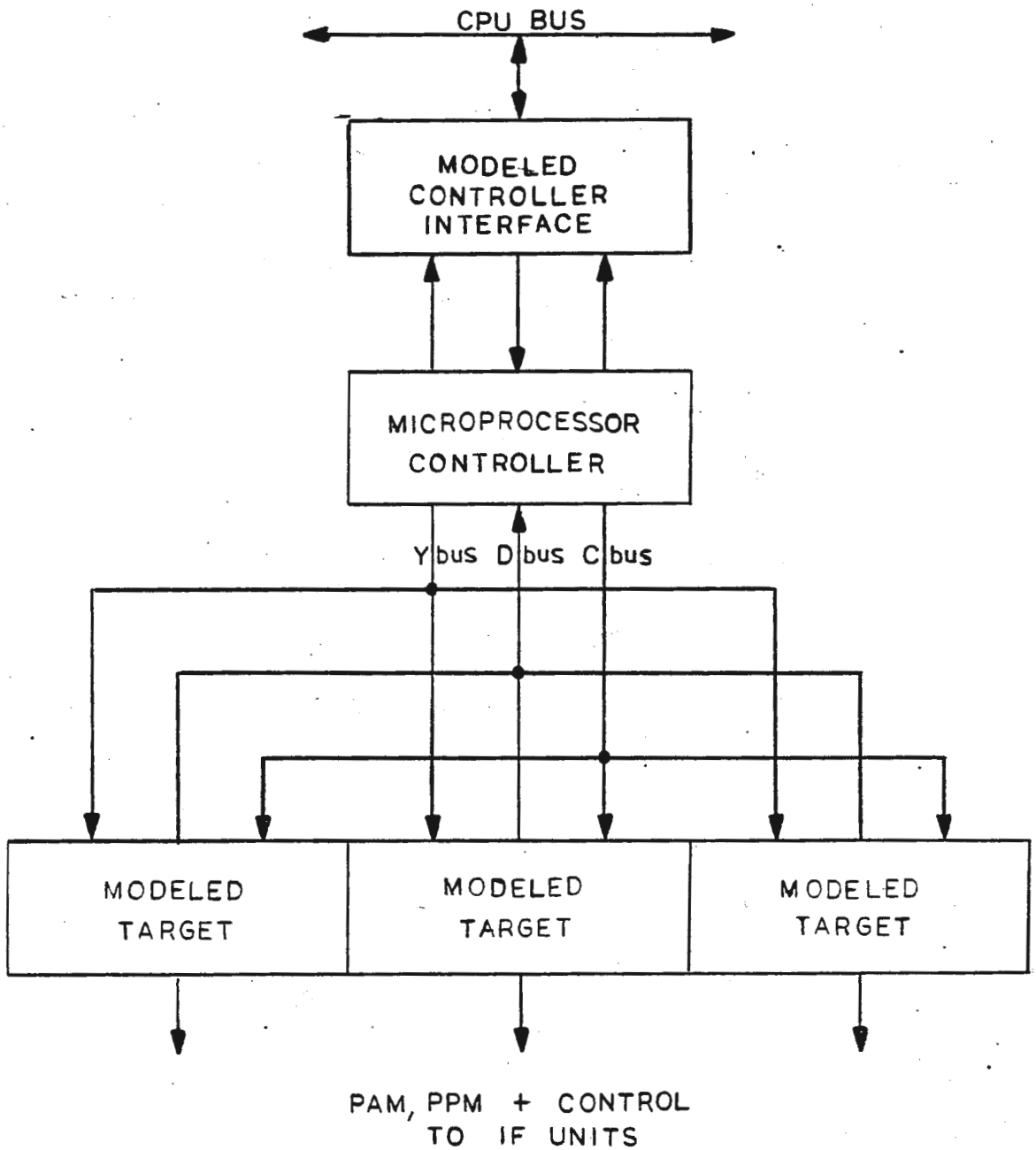


FIGURE 3.4. UPLINK RECEIVER DIGITAL CIRCUITRY



MODELED REPLY GENERATOR

FIGURE 3.5. MODELED REPLY GENERATOR BLOCK DIAGRAM

3.4 FRUIT REPLY GENERATOR.

The Fruit Reply Generator (FRG), although similar to the MRG, operates independently in simulating ATCRBS and Mode S fruit. The FRG will receive reply message blocks by reading pseudo-random fruit reply data from the random process generator (RPG). The RPG will be controlled by fruit control parameters specified in the traffic model. These parameters will control the average fruit per sector, the fraction of replies in the main antenna lobe (as opposed to being in the sidelobe), the fraction of ATCRBS replies having a fixed or known data content, and the fraction of long versus short Mode S replies. The fraction of long versus short Mode S replies will be controlled over the range of 0 to 1 in increments of 1/15. The FRG will provide an average ATCRBS fruit rate between 0 to 50,000 replies per second in increments of 1,000 replies per second, and an average Mode S fruit rate between 0 to 500 replies per second in increments of 10 replies per second.

The major sections of the FRG are depicted in figure 3.6. The FRG will consist of a fruit controller interface to the ARIES computer, the microprocessor controller, the random process generator, and four fruit reply generators refered to as fruit ARIES targets (FATs). Three of the FATs will be used to generate ATCRBS fruit replies and the fourth FAT will be used to generate Mode S fruit replies. The Mode S fruit will be generated independant of the ATCRBS fruit.

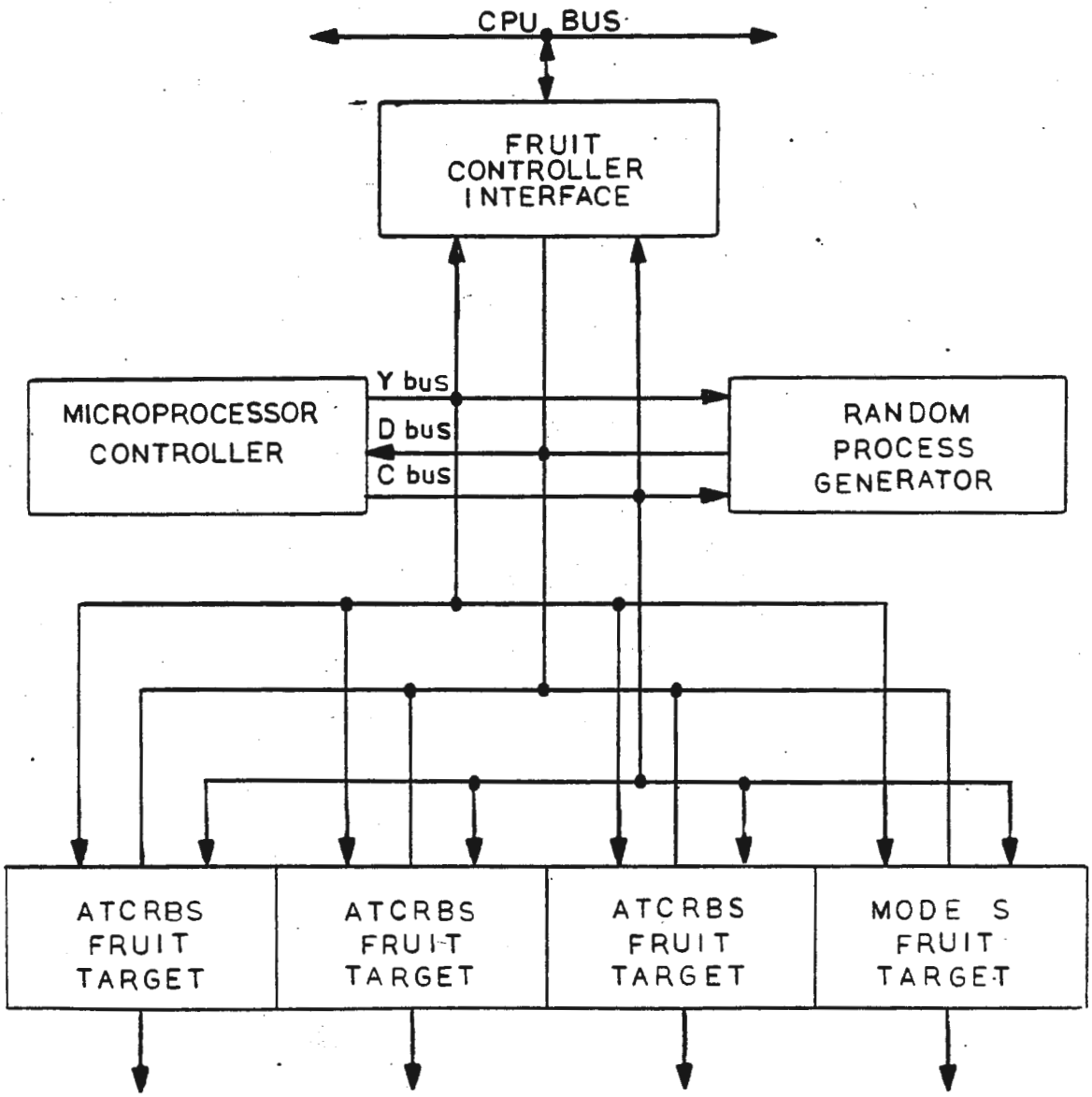
The FRG interface will provide all the logic and control functions required to connect the FRG to the ARIES computer. In addition it will contain registers for storing the fruit control parameters.

The microprocessor controller will obtain the fruit control parameters from the interface and transfers them to the RPG. The controller will then read a fruit reply message block from the RPG, selected which FAT can accept it, and transfer the reply information to the available FAT. The FATs will be completely identical in hardware capability to the MATs specified in Section 3.3.

The RPG will determine the parameters and timing of each fruit reply according to a set of pseudo-random sequences providing inputs to the FAT controller identical to the inputs the ARIES computer provides to the MAT controller.

3.5 IF REPLY GENERATORS/COMBINER AND RF MODULATOR NETWORK.

The IF Reply Generators/Combiner and RF Modulator Network will consist of the analog block diagrams shown in figures 3.7 A/B and 3.8. Refering to figure 3.7A, each ARIES modeled reply generator and fruit reply generator will contain a crystal-controlled oscillator. Each oscillator will be off set from the others at a multible of 500 KHz centered around the intermediate frequency of 60 MHz to eliminate potential coherent interference at the Mode S receiver. The oscillator output will be modulated by a pulse amplitude modulation (PAM) switch and will provide a minimum on/off isolation of 80 dBm. The PAM switch output will be attenuated by a 6-bit digitally controlled attenuator which will be used to control the ARIES reply output power level to the Mode S sensor. The digitally controlled attenuator will provide a 64 dB range in 1 dB increments. The attenuated signal will be split into the Main and Omni simulated antenna channels.



FRUIT REPLY GENERATOR

FIGURE 3.6. FRUIT REPLY GENERATOR BLOCK DIAGRAM

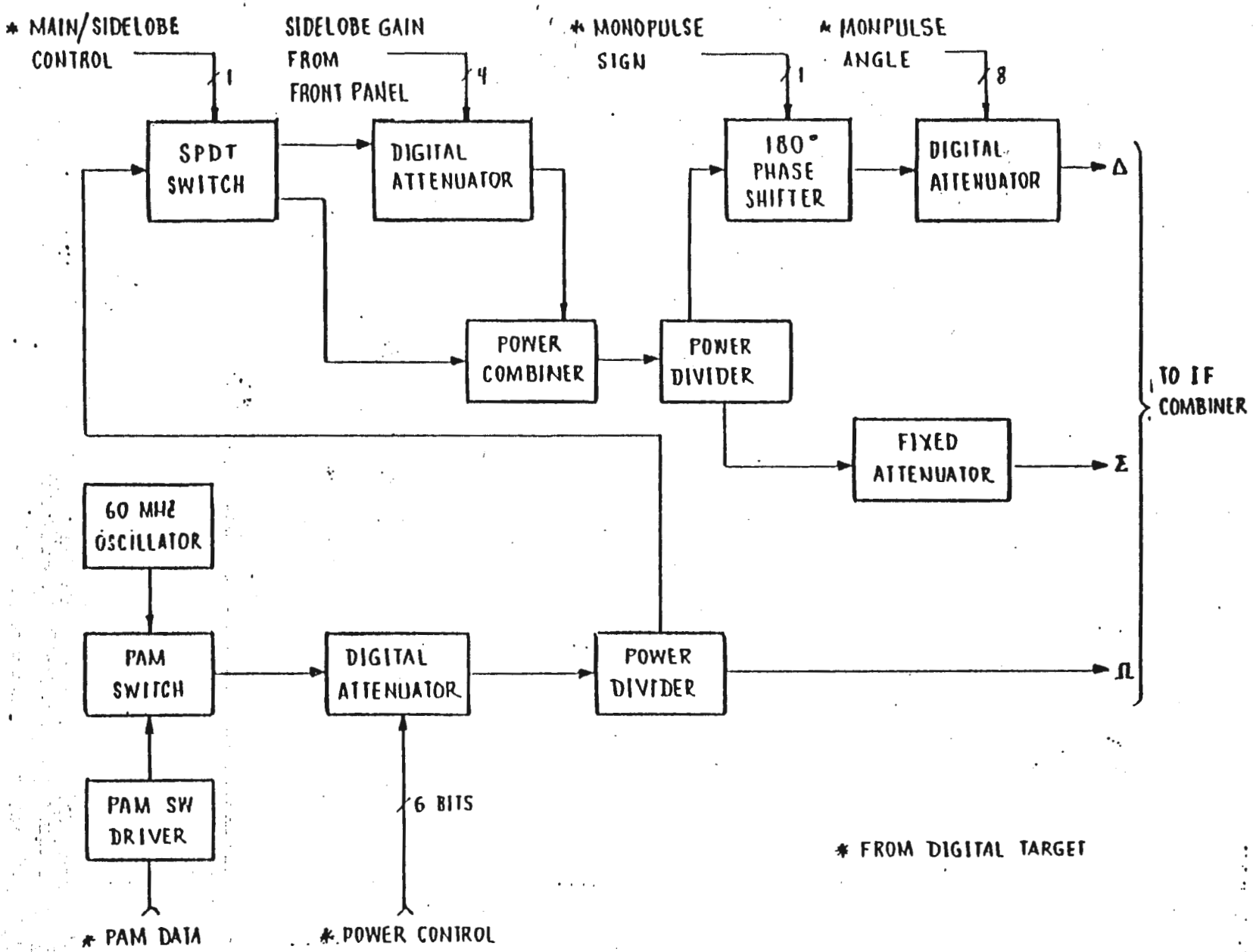


FIGURE 3.7A IF UNIT, BLOCK DIAGRAM

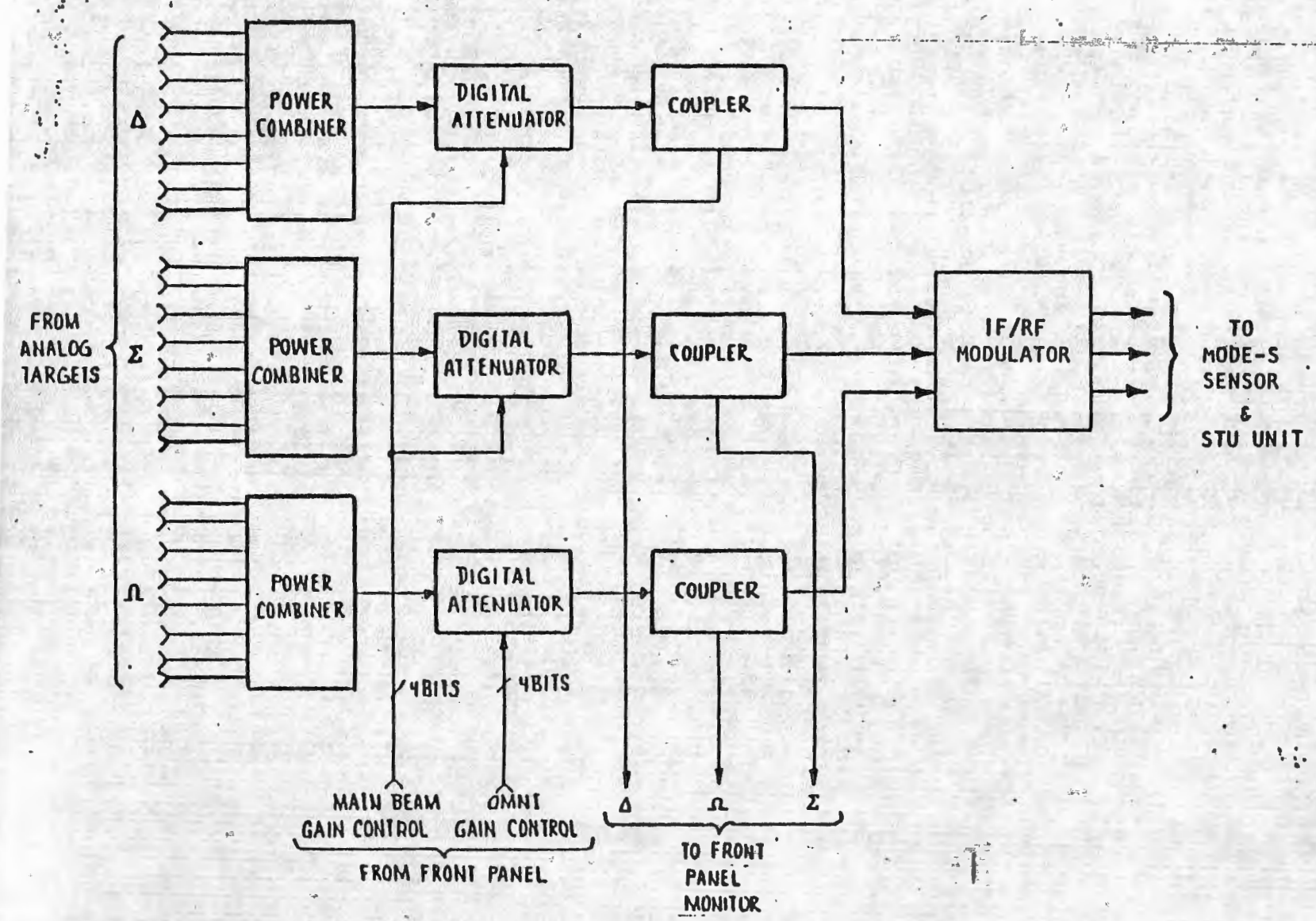


FIGURE 3.7B IF UNIT, BLOCK DIAGRAM

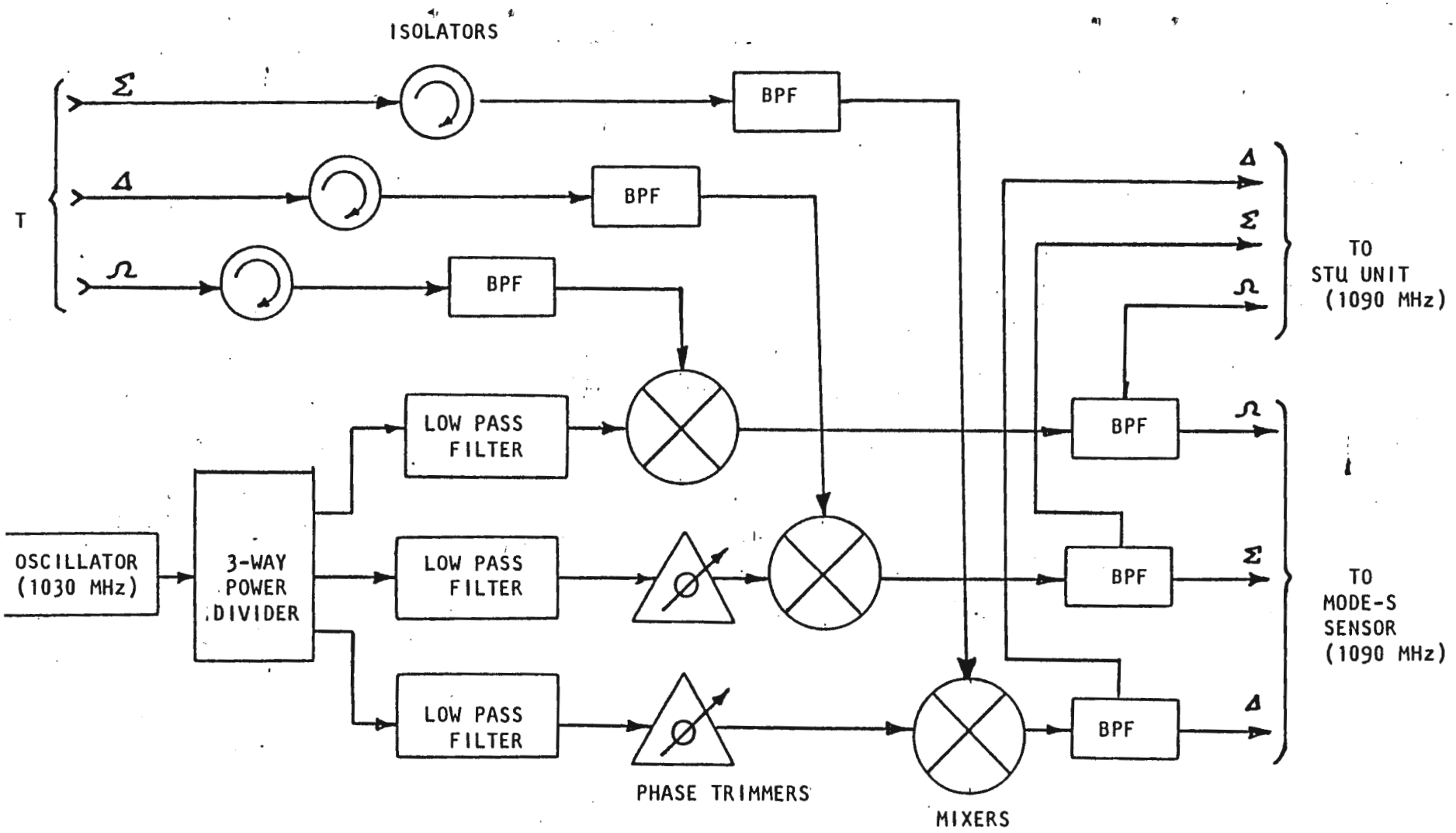


FIGURE 3.8 IF/RF MODULATOR

The Main antenna channel will go to a second PAM switch and allow the option of simulating mainbeam or sidelobe signal levels at the Mode S sensor. The sidelobe level will have the capability of being adjusted manually with a sidelobe gain attenuator over a 15 dB range from a preset level of -36 dBm below the mainbeam. This resulting signal will then be power divided to form the Sum channel and the Delta channel going to the IF combiners.

The off-boresight angle simulation will be done by changing the gain setting of the Delta channel with respect to the Sum channel. This will be accomplished by an 8-bit digitally controlled attenuator. Each bit will represent attenuation of the Delta channel with respect to the Sum channel with 0 corresponding to delta equal to sum. The sign of the off-boresight angle will be simulated digitally by controlling a 180° phase shifter. To compensate for losses contributed by the phase shift network a fixed attenuator will be installed in the Sum channel which will allow balancing of the Sum and Delta channels.

Figure 3.7B is a block diagram of the IF combiner and RF modulator circuitry. The three IF power combiners will combine the Sum, Delta, and Omni IF inputs signals from the three reply generators and the four fruit reply generators to provide a single set of sum, delta, and omni IF outputs. An eighth input port of each combiner will be available for injecting an external IF interference source.

To establish the relative mainbeam to omni levels for a particular Mode S antenna system and to compensate for cable losses between the ARIES and the sensor the three combiner output signals will be attenuated by a set of manually controlled 4-bit attenuators. Each attenuator will provide from 0 to 15 dB of attenuation in 1 dB increments. Each sum, delta, and omni signal will be coupled through a directional coupler to provide ARIES front panel monitoring of the IF signals prior to RF mixing. The IF signals of each directional coupler will be fed to an RF mixer as shown on figure 3.8. A single LO at 1030 MHz will be used as the mixer frequency. The LO signal will be amplified and connected to the three mixer stages. The RF mixers will then modulate the 60 MHz sum, delta, and omni signals to 1090 MHz RF output signals after filtering. Each 1090 MHz RF signal will be split by a directional coupler to provide two sets of signals. One set of RF signals will be fed back to the self test unit of the ARIES to support system verification tests. The other set of RF signals will be phased and amplitude adjusted before being fed into the appropriate Mode S sensor ARIES input ports.

3.6 AZIMUTH CHANGE PULSE DECODER/GENERATOR.

The ACP Decoder/Generator will receive azimuth signals from the Mode S sensor's antenna system in the form of ACP's and ARP's. There are 16,384 ACP's and a single ARP for each complete revolution of the antenna. Azimuth conversion logic will be provided to adjust the antenna azimuth reference to an alternate reference such as to true north. The amount of correction will be adjustable over the full azimuth range in increments of 1 ACP.

The ACP Decoder/Generator will be capable of generating simulated ACP's and ARP's whether it is operating with an antenna or not. In this simulation mode the ACP's and ARP's from the antenna are ignored. The simulated ACP's and ARP's will be transfered to the Mode S sensor identical to those which would be generated by the antenna rotating at a specified constant rotation rate. The simulated rotation

period will be adjustable over the range of 3.5 to 15 seconds in increments of 250 nanoseconds.

The mode of operation will be selectable by the operator using a front panel toggle switch. In both modes of operation the ACP Decoder/Generator will generate a 14-bit azimuth word that will be used by the receiver's digital circuitry noted in Section 3.3 so that each interrogation received is assigned a specified azimuth. The self test unit will receive corrected ACP's and ARP signals.

3.7 SELF TEST UNIT.

The STU will be a diagnostic tool used to verify the correct operation of the ARIES system. It will perform all testing at the RF input and output ports of the ARIES. The STU will be self contained unit comprised of all analog and digital processing circuitry which are necessary for routine verification of the ARIES. A communication path between the STU processor and the ARIES processor will be provided for initial loading and data transfers. The STU will have no operator console or recording peripherals so all communications will be via the ARIES.

The STU will provide diagnostic capabilities which will, in conjunction with ARIES resident diagnostics, verify the operation of the receiver, reply generator and fruit generator subsystems. The data transfer capability, reply power, range accuracy, and monopulse accuracy of each subsystem will be tested throughout their dynamic range. The ARIES will test the Mode S sensor for a very simplistic case. The overall ARIES system operation will be verified by having the STU generate interrogations and listen for appropriate replies. The ARIES will use, for this diagnostic, unmodified operational software and a test scenario of two targets, one Mode S and one ATCRBS. The STU will provide interrogations to the ARIES and store the range, azimuth, and reply data of each reply received for subsequent analysis. A functional block diagram of the digital circuitry of the STU is given on figure 3.9.

3.7.1 Interrogation Generation Circuitry.

The interrogation generation digital circuitry will provide all the digital preamble and message gate modulation pulses to the analog circuitry. The digital circuitry will also provide the DPSK modulation pulses for Mode S type interrogations. The data content of the Mode S interrogations will be under software control. Generation of up to 50 unique interrogations of any type during a 5 to 20 millisecond period will be possible. These interrogations will be made time dependent by referencing a 20-bit time word whose LSB is 62.5 nanoseconds. The time word circuitry will count down from a value preset by software and automatically reiterates that same time interval unless the present value has been changed. Each interrogation will have associated with it a transmission time which, when equal to the decrementing time word value, will initiate the transmission. The STU processor will dynamically modify the set of interrogations for each succeeding interval. Also, reference corrected antenna azimuth information will be available from the ACP Decoder/Genertor.

The analog circuitry for the STU uplink simulation mode will support all types of Mode S and ATCRBS interrogations as specified in the Mode S National Standard (dated 1/3/83). Figure 3.10 is a block diagram of the interrogation generator RF circuitry. The modulation signals (Preample/message gate input and the DPSK input)

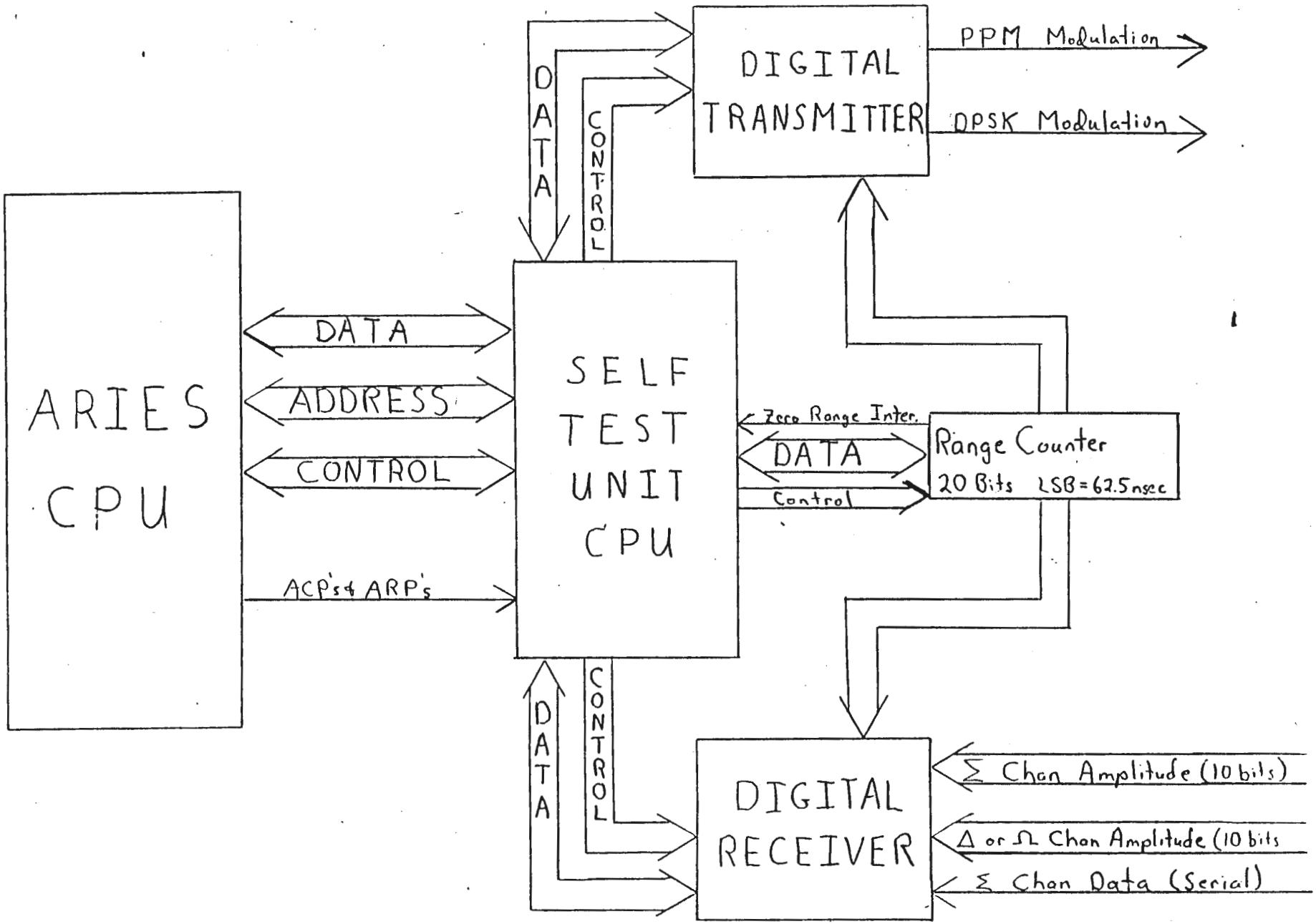


FIGURE 3.9. SELF TEST UNIT BLOCK DIAGRAM

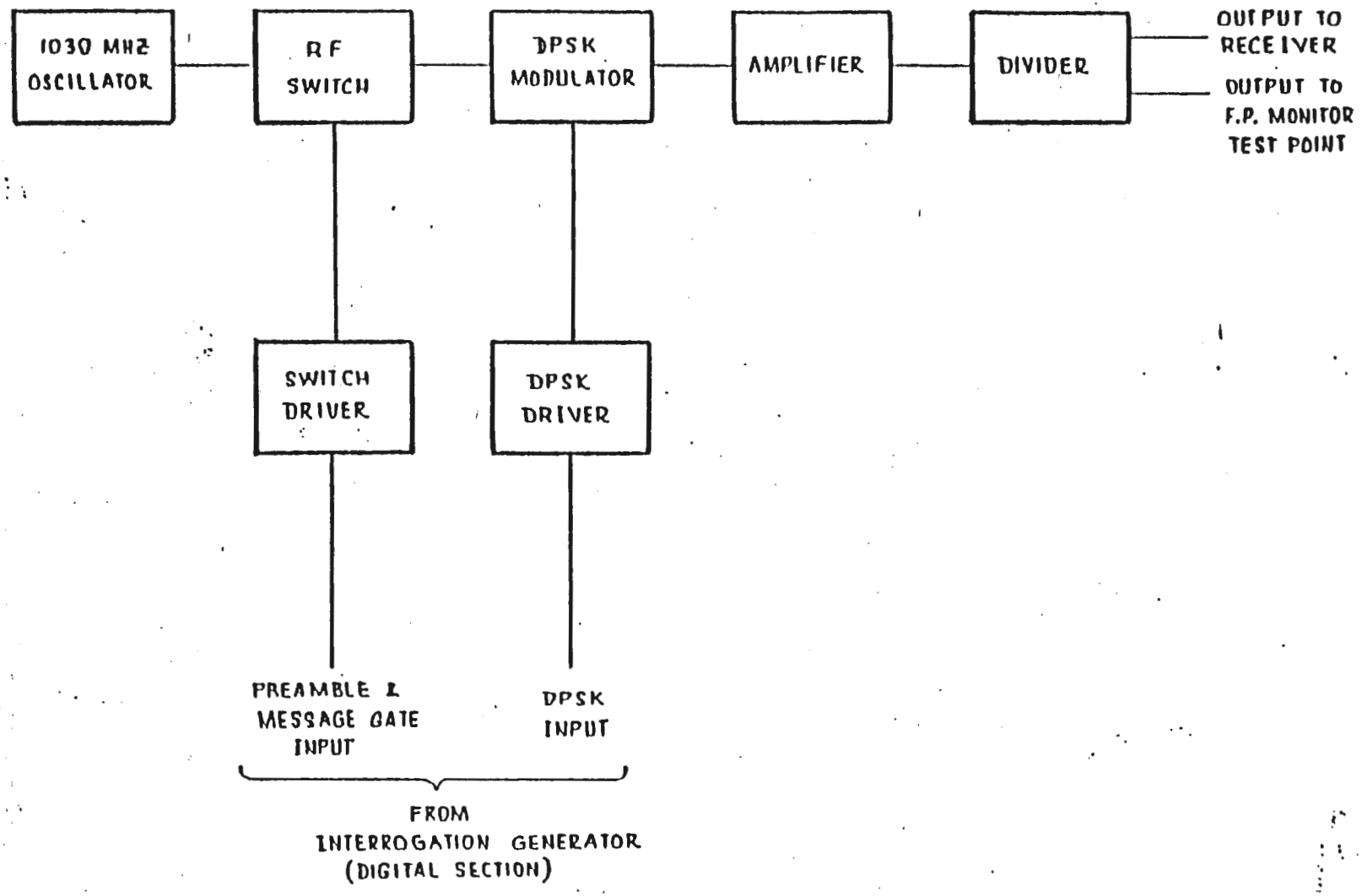


FIGURE 3.10. INTERROGATION GENERATOR (RF SECTION)

will be received from the interrogation generator digital circuitry. The simulated Mode S interrogation will be amplified and then split using a power divider into two channels. One RF output will be coupled into the 1030 MHz receiver input port of the ARIES. The power level will be fixed to match the normal interrogation power level coupled out of the Mode S sensor. The other RF output will be used for front panel monitoring.

3.7.2 Reply Receiver Circuitry.

The Reply Receiver Circuitry will be capable of receiving ATCRBS and Mode S replies from any of the ARIES reply generators. Couplers will permit the reply signals from the ARIES 1090 MHz output to be fed-back to the STU receiver circuitry. The reply data content of the Sum channel will be placed in STU memory for analysis or for subsequent transfer to the ARIES to view or record the data. The signal levels of the Sum, Delta, and Omni channels will be measured. This will be performed by converting the received signal to a log video signal and then sampling the video amplitude with a 10 bit analog-to-digital converter. This will result in a signal level resolution of approximately 0.1 dB.

A block diagram of the reply sampling RF and IF circuitry is shown on figure 3.11. Couplers will permit the reply signals from the ARIES 1090 MHz output (Sum, Delta, and Omni) shown on figure 3.8 to be fed-back to the STU's receiver circuitry. The 109U MHz RF signals will be modulated with a LO operating at 1030 MHz using a mixer to produce the 6U MHz IF signals.

As shown on figure 3.12, any of the three IF signals will be available for amplitude sampling. The Sum channel will be available for sampling all of the time and either the Delta channel or Omni channel will be selected. The outputs to be sampled will be amplified and detected by a log amplifier. The resultant video signals will then be amplified by a linear amplifier. The resultant video signals will be sampled and converted into binary words by separate sample and hold (S/H) amplifiers and analog to digital (A/D) converters.

The phase difference (assumed to be 0° or 180°) between the Sum and Delta channels will be measured. This will be accomplished by multiplying the Sum and Delta channels together. The result will be used to set a phase bit which will provide a means of checking the phase shifter in the analog reply generators.

3.8 RADAR REPORT GENERATOR.

The RRG will be capable of simulating radar data to any of the Mode S sensor's five primary interfaces listed below:

Air Surveillance Radar (ASR-9)/Moving Target Detector (MTD)
Common Digitizer Model 2 (CD-2)
Production Common Digitizer (PCD)
Radar Data Acquisition System (RDAS)
Air Route Surveillance Radar (ARSR-3)

At most only one of the type of primary radars will be simulated during any simulation run. During system initialization the RRG will be placed in an inactive mode, that is no primary interface selected. The primary interface to be used for a particular test will be specified either by the traffic model or by operator command.

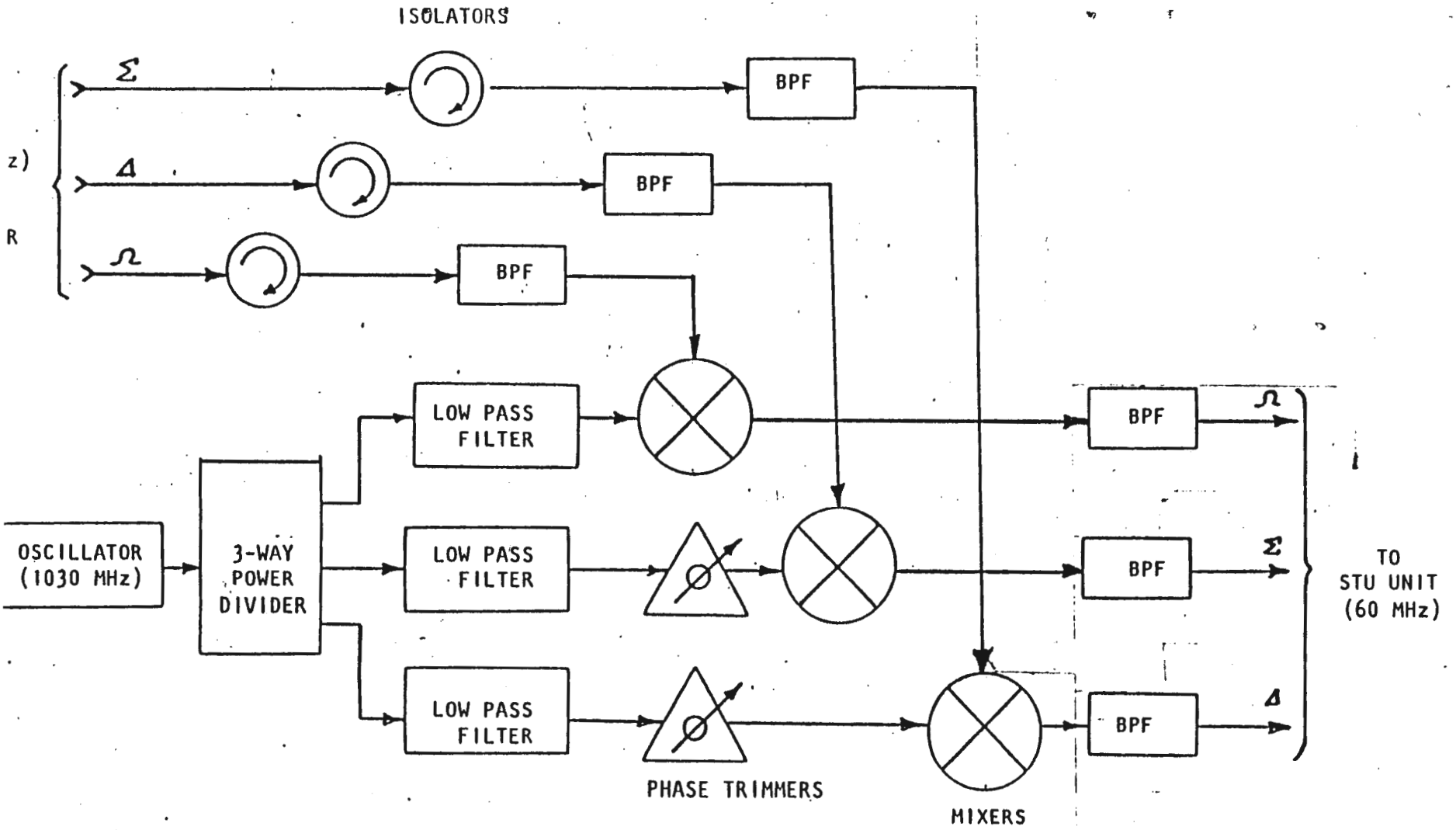


Figure 3.11. RF/IF MODULATOR

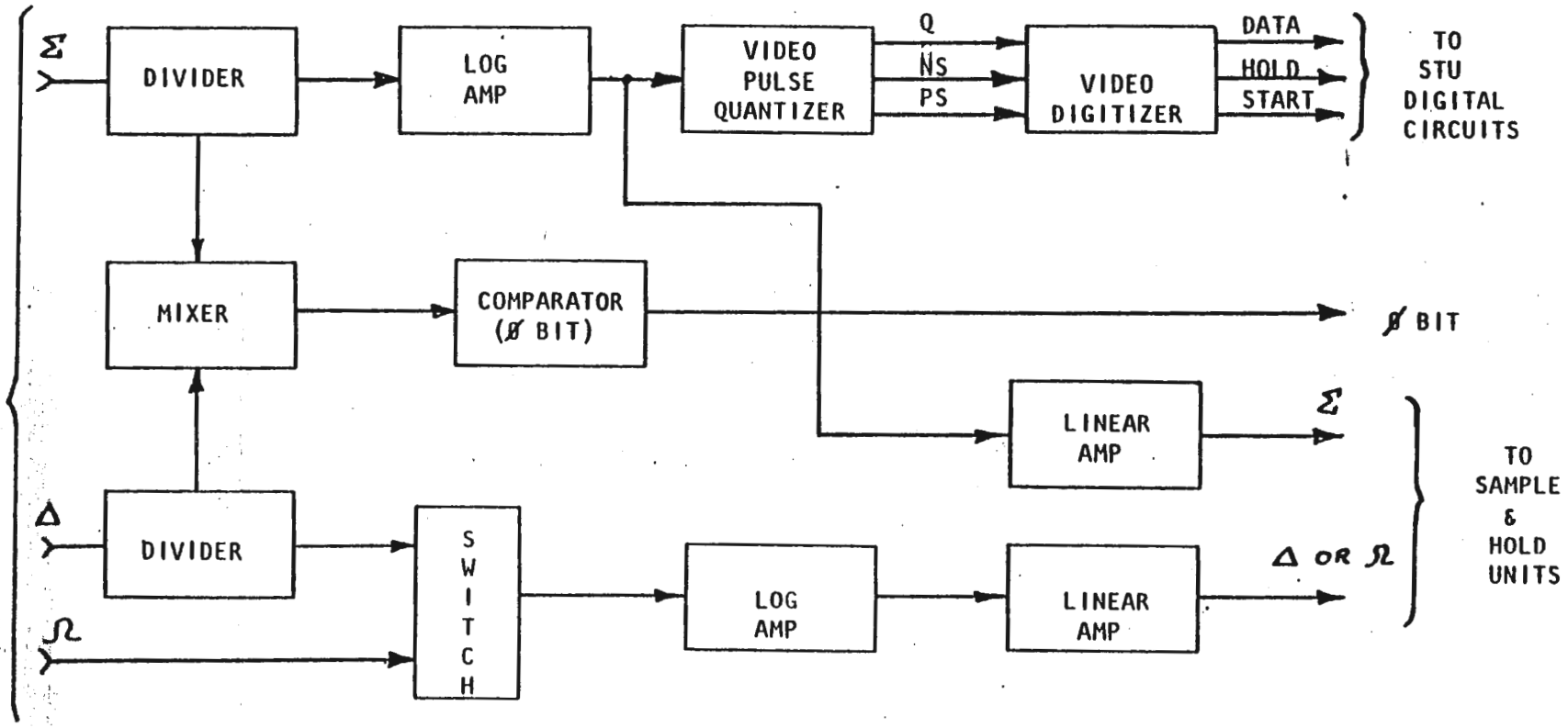


FIGURE 3.12. P/O STU UNIT (ANALOG)

As depicted on figure 3.13, the RRG will consist of an interface to the ARIES CPU, a microprocessor, read only memory (ROM), random access memory (RAM), a command register, five primary interfaces, and control logic. The ROM will house all the software routines necessary to simulate each of the primary interfaces plus perform off line diagnostics. Operating instructions will be past to the RRG via the command register.

The RRG will receive radar report data blocks from the radar report generation routine via the RRG interface using DMA data transfers. These data blocks will be prepared based on the traffic model. The microprocessor will read the data blocks and format radar reports identical to those that are outputted by the primary interface selected. The radar reports then will be loaded into the appropriate primary output port for transfer. Each output port will be capable of transmitting data over a 300-foot cable.

In the diagnostic mode each of the primary interfaces will support loop-back verification tests. Also the RRG will perform hardware validation checks on the RAM and interface.

3.9 OTHER SUBCIRCUITS.

There are several other subcircuits identified in the overall block diagram of figure 3.1. These circuits are the universal interrupt timer (UIT), the ARIES clock, a poisson sequence generator referred to as the random number generator (RNG), Inter ARIES communications, and sensor's time-of-year (TOY) clock interface.

3.9.1 Universal Interrupt Timer.

The UIT will consist of a 16-bit hardware countdown timing register, with a resolution of 1 microsecond, and associated computer control circuitry. The device will have three modes of operation:

1. Generation of timing signals at a periodic rate over the range of 1 microsecond to 64 milliseconds.

2. Generation of timing signals after a time interval of which the start time and duration is determined by software functions.

3. Providing software functions with the value of the time remaining before the current time interval is completed.

During the normal mode of operation, the UIT will provide timing information to the software about the ATCRBS/All Call interrogations. Diagnostics will use the UIT to time the occurrence of events or to initiate events.

3.9.2 ARIES Clock.

The ARIES clock circuitry will be the main timing reference for the ARIES digital system, with the exception of the central processing unit. The circuitry will provide synchronous timing operation to the ARIES digital system through the generation of a 16 MHz and a 4 MHz clock output. The 16 MHz clock signal will be a symetrical digital waveform and the 4 MHz clock signal will be an asymetrical digital waveform with a 25 percent duty cycle.

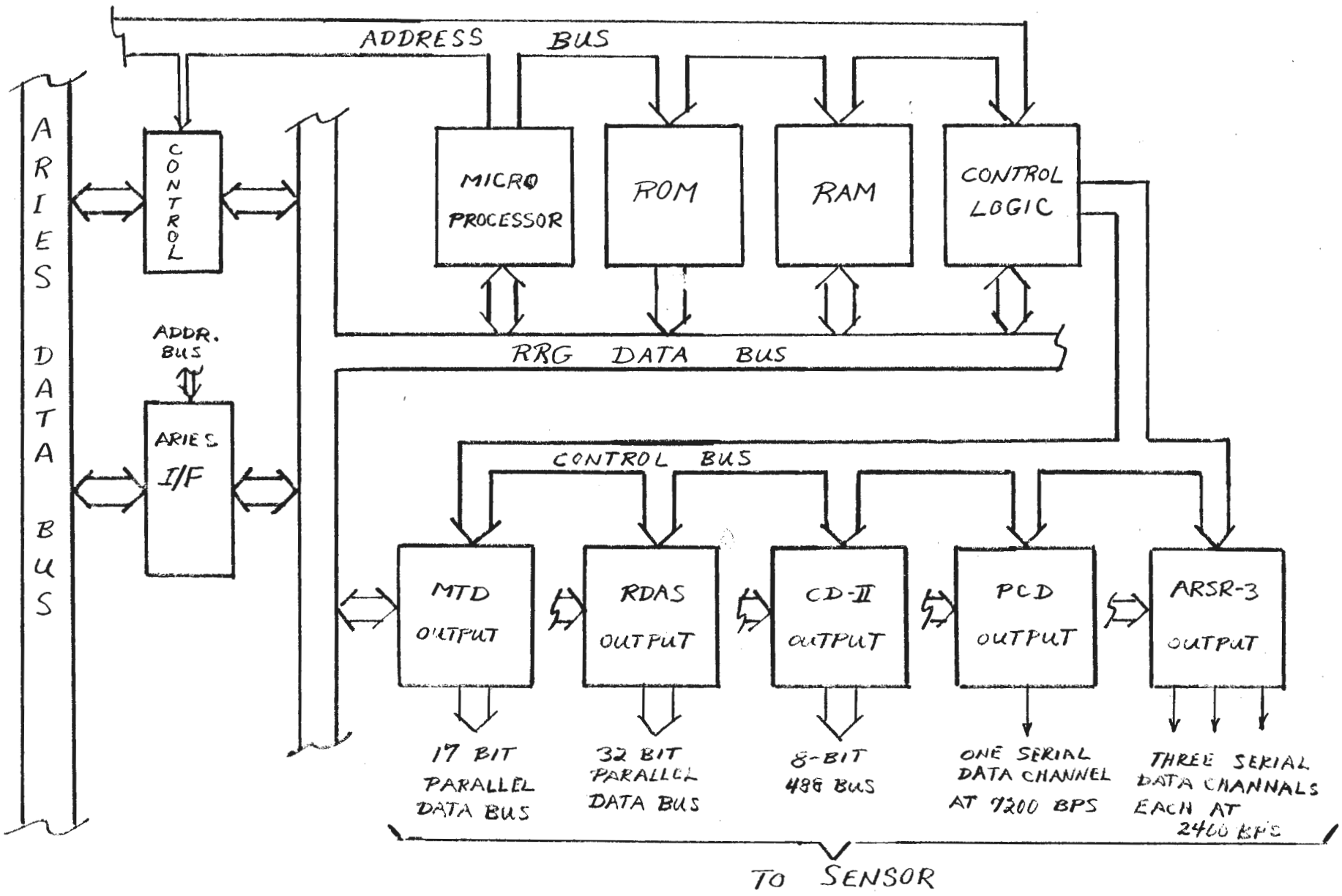


FIGURE 3.13. RADAR REPORT GENERATOR BLOCK DIAGRAM

A diagnostic mode will be available to provide single step operation. This will produce either a single clock pulse or a group of four 16 MHz clock pulses along with one 4 MHz clock pulse when selected by a manually operated switch.

3.9.3 Random Number Generator.

The RNG will provide to the CPU a 16-bit uniformly distributed random integer. The circuitry will consist of a 17-bit maximum length sequence generator which will generate a sequence of (2**7)-1 states before repeating. In order to prohibit the zero state, the generator will be preset to a non-zero condition during system initialization.

The generator will remain static until such time that the CPU reads the current value. Immediately following the read sequence, the generator will be clocked once to produce a new random number in preparation for the next CPU read.

3.9.4 Inter ARIES Communications.

The simulation of multisite operation, both netted and unnetted, will be supported using an ARIES-to-ARIES interface. This interface will provide time synchronization with other ARIES and will allow the simulated aircraft to have the same transponder state. The scenario for each ARIES will be coordinate converted during scenario generation, so that no positional data will be transferred.

Time synchronization between each ARIES will be kept to within 0.1 seconds. The primary data flow will be to provide Mode S lockout, Comm A/B and Comm C/D transponder state changes.

3.9.5 Time-of-Year Clock Interface.

The TOY clock interface will store the buffered outputs of the Mode S sensor's TOY clock. This time information will be referenced to universal time clock time with an accuracy of ±2.5 milliseconds. The TOY interface will store the entire output of the Mode S sensor's TOY clock. This will include the days, hours, minutes, seconds, and fraction of seconds with a resolution of 1/128 of a second. The TOY clock information will be formatted into four 16-bit words and be made available to the ARIES data recording function for time tagging events and also to other ARIES functions which may require it.

4.0 SOFTWARE CONFIGURATION.

4.1 OPERATIONAL SOFTWARE OVERVIEW.

The primary function of the ARIES operational software will be to process interrogations from the ARIES receiver and provide modeled beacon replies and fruit replies to the appropriate reply generators and radar reports to the appropriate radar interface.

The devices that will provide input to the ARIES software are:

1. Receiver - will provide input in the form of 10-word interrogation data blocks. Their format is shown on figure 3.3.

2. Universal Interrupt Timer - will generate an interrupt after an interval determined by the sensor's ATCRBS/All Call interrogation pattern.

3. Time-of-Year Clock Interface - will provide real time-of-day and date from the sensor's WWVB clock in the form of a 4-word data block.

4. Fruit Reply Generator - In the diagnostic mode the FRG will send fruit replies to the processor instead of the FATs. The format of these replies will be the same as that of the modeled ARIES targets, i.e., a 4-word data block for ATCRBS fruit and a 10-word data block for Mode S fruit.

5. Disk Drive - will provide traffic model input.

The ARIES system will provide output to the following devices:

1. Modeled Reply Generator - will expect output in 4-word (ATCRBS) or 10-word (Mode S) data blocks. The formats are shown on figures 4.1 to 4.4.

2. Fruit Reply Generator - In the normal mode of operation the FRG will expect fruit parameter data from the processor in the form of a 10-word data block. The format of this data block is shown on figure 4.5.

3. Radar Report Generator - will expect a 6-word data block for each primary radar report to be transmitted. The format of the radar report data block is shown on figure 4.6.

4. Magnetic Tape - Magnetic tape will be used to store data extraction data.

4.2 SYSTEM TASKS AND TASK SCHEDULING.

The ARIES operational software will be broken down into two groups of tasks. Each task will perform a distinct logical function, with shared data structures stored in a section of memory devoted to global data. The first group will consist of the time critical tasks, which are invoked by hardware interrupts. These include Interrogation Processing and ATCRBS/All Call Reply Generation, which will be scheduled by a timer interrupt, and all the hardware interrupt handlers.

The second group will consist of "background" tasks. The ARIES main program will consist of an "idle loop" in which task enable flags are continually checked. These tasks will not interrupt each other, but may be interrupted by tasks in the first group. The tasks in this group will include Data Extraction, Pre-Interrogation Processing, Traffic Model Input, and Timer Countdown.

4.3 PRE-INTERROGATION PROCESSING.

This task will be executed every 0.1 seconds. It searches the Track File for Aircraft that will be interrogated within the next 0.1 seconds, updates the aircraft's position to the time at which it will cross the antenna boresight, and places a pointer to the track entry into the Reply Time Sorted Index for the appropriate antenna (front or back face). The two indexes then will be sorted by reply time and replace the current copies of these tables.

```
| 0|  |  |  |  |  |  | 7| 8|  |  |  |  |  |  |15|
 _______________________________________________
|                  Reply Time                   |
| X|      Power       |LR|        Monopulse     |
|       <-------X------>      |MS| X| 0| 0| 0| 1|
|                 ATCRBS Code                   |
```

LR=Left/Right bit
MS=Mainlobe/Sidelobe bit

FIGURE 4.1 ATCRBS REPLY DATA

```
| 0|  |  |  |  |  |  | 7| 8|  |  |  |  |  |  |15|
 _______________________________________________
|                  Reply Time                   |
| X|      Power       |LR|        Monopulse     |
|       <-------X------>      |MS| X| 0| 0| 1| 0|
| 1| 0|    Capability    |                      |
|              Mode S Address                   |
|             <--------- 0 --------->           |
|  <------0------>        |   <-------X------>  |
|             <--------- X --------->           |
|             <--------- X --------->           |
|             <--------- X --------->           |
```

FIGURE 4.2 MODE S ALL CALL REPLY

```
| 0|  |  |  |  |  |  | 7| 8|  |  |  |  |  |  |15|
 _______________________________________________
|                  Reply Time                   |
| X|      Power       |LR|        Monopulse     |
|       <-------X------>      |MS| X| 0| 1| 0| 0|
|  <----0----> | A| S|AI| <----0---->  | PBUT| B|
| 0| 0|FR|         Altitude/Identity            |
|            Mode S Address                     |
|                         |   <-------X------>  |
|             <--------- X --------->           |
|             <--------- X --------->           |
|             <--------- X --------->           |
```

A=Pilot Alert bit
S=Synchro Mode-S bit
AI=Altitude/Ident bit
PBUT=Pilot Ack. bit
B=Comm-B Request
FR=Flight Rules bit

FIGURE 4.3 MODE S ROLL CALL REPLY

```
| 0|  |  |  |  |  |  | 7| 8|  |  |  |  |  |  |15|
 _______________________________________________
|                  Reply Time                   |
| X|      Power       |LR|        Monopulse     |
|       <-------X------>      |MS| X| 1| 0| 0| 0|
| 0| 1| 0| 0| 0| A| S|AI| <----0---->  | PBUT| B|
| 0| 0|FR|         Altitude/Identity            |
|                                               |
|               Message Field                   |
|                         ______________________|
|_________________________|                     |
|             Mode S Address                    |
```

FIGURE 4.4 MODE S COMM-B REPLY

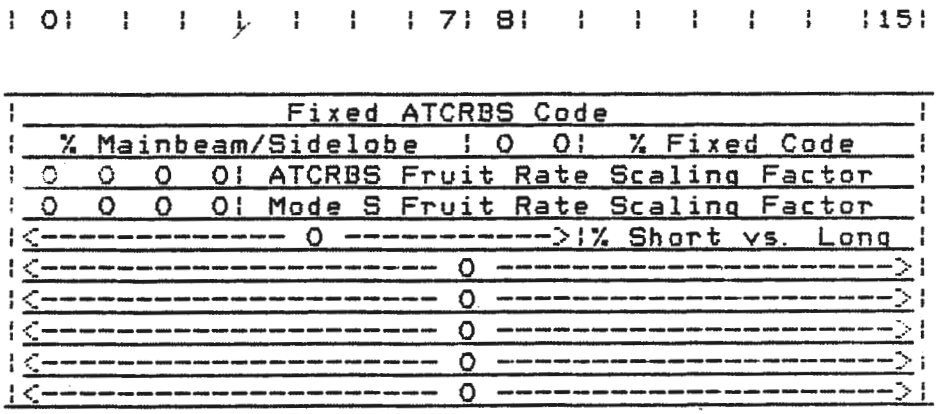


Figure 4.5. Fruit Parameter Data Block

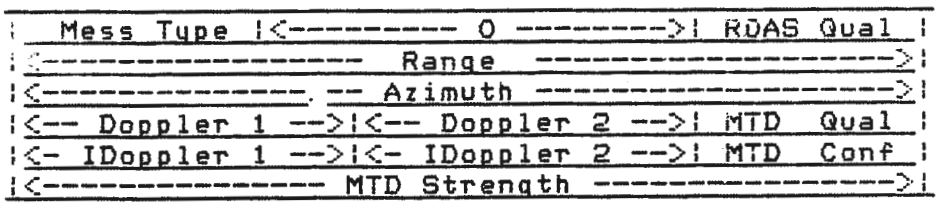


Figure 4.6. Radar Report Data Block

Another function of the Pre-interrogation Processing task will be to generate simulated radar reports for each target. These reports are placed in radar report buffers, each one corresponding to one azimuth bin of the Azimuth Sorted Index.

The following is a description of each of the subfunctions:

1. Track File Search - A scan will be divided into 256 azimuth bins, each containing a linked list of aircraft in the corresponding azimuth sector.

There will be a special bin for aircraft within five nautical miles of the sensor. The antenna azimuth at the beginning and end of each 0.1 second period will be estimated using the Antenna Azimuth Rate and Data file. These values will determine the start and end azimuth bins for further processing.

2. Track File Update - The time at which the target will cross boresight will be estimated using the Antenna Azimuth Rate and Data file and the Track File. The Track File then will be updated to this time. If this update causes the track to change bins, the track will be removed from Track File. After all bins have been processed, these tracks will be placed in the proper bin.

3. Reply Time Sorted Index Preparation - As each Track file entry is updated, a pointer to the entry will be placed in the Reply Time Sorted Index. At the conclusion of the update subtask, this list will be sorted by reply time. It then will be passed to Interrogation processing. Care must be excercised in this, so that Interrogation Processing (which is interrupt driven) will not attempt to access the index before the process is complete.

4. Radar Report Generation - Each time a beacon report is generated for a target in the main beam of the front antenna, a radar report also will be generated. The range, time, and azimuth units are then converted to be compatible with the radar interface type selected during system initialization. A random number then will be obtained and compared to the radar blip/scan ratio to determine whether the report will be disseminated.

4.4 INTERROGATION PROCESSING.

4.4.1 Discrete Interrogation Processing.

The Discrete Interrogation Processing sub-task will be initiated by a hardware interrupt generated by the receiver. The Mode S discrete address in the interrogation will be used as an index into the Track File in order to obtain the record for this aircraft. The next step then will be to determine whether the target is to reply. A random number will be read from the hardware random number generator and compared to the reply probability in the track file. If it is greater than the reply probability, then the reply will not be generated. The reply off-boresight angle will be calculated and if it is greater than half the effective beam width, the reply will not be generated. The contents of the reply block then will be determined and placed in the reply buffer for the modeled reply generator hardware.

4.4.2 ATCRBS/All-Call Interrogation Processing.

Because of the short time available (about 15 usec.) to respond to an ATCRBS interrogation, replies will be generated at the time of the previous interrogation.

At that time the UIT will be set to interrupt shortly before the replies are due, at which time they will be transferred to the modeled reply generator hardware.

The first step in generating a reply will be to obtain the Interrogation Pattern File, which will contain:

1. Time of next interrogation

2. Mode of the next interrogation (2, 3/A, or C)

3. Front or back antenna

Next, the Antenna Azimuth Rate and Data File will be updated. The subtask then will access the Reply Time Sorted Index for the appropriate antenna azimuth, obtain each entry in turn and determine if it will reply (as above), format the reply, and place it in the reply buffer.

4.5 TRAFFIC MODEL INPUT.

This procedure will have the function of updating track records in the Track File based on the traffic model on disk. Tracks are updated at time specified in the model records which cause the updates. In addition to updating the Track File; Traffic Model Input may update the track's position in the Azimuth Sorted Index; add tracks to, or delete them from that index; add tracks to or delete them from the Mode S ID Lookup Table; and delete tracks from the Reply Time Sorted Index.

4.6 SYSTEM INITIALIZATION.

This program will control the initialization of the ARIES system. It will initialize the system data structures, initialize the various I/O devices, create the system tasks, and read data from the disk to initialize the micro-code and certain Site Characterization Tables.

System Initialization also will send an initialization message to all the other ARIES sites to inform them of the fact that the local site is initializing and also to specify the initial model time.

Once System Initialization has completed its initialization functions it will reduce itself to being the lowest priority task, and take on the combined functions of the system idle loop and the background task scheduler. The system idle loop will check the system status flags every millisecond and if they have all been cleared by Operator Communications due to a reinitialize command, System Initialization will resume highest priority and reinitialize the system.

4.7 OPERATOR COMMUNICATIONS.

Each ARIES site will have a terminal which will allow the local operator to interact with the system and control its operation. Operator Communications will prompt the operator to enter a command number. Once this is done, it will prompt the operator to provide any needed input parameters. After receiving all needed parameters, Operator Communications will execute the desired function and, unless the operator has requested that the system be halted or reinitialized, again will prompt the operator for a new command number.

The available commands and the corresponding command numbers are listed below.

1. Start the simulation running from the current initial time.
2. Halt the simulation and restore the normal operating system.
3. Halt the simulation and reintialize to a time specified by the operator.
4. Print system status information.
5. Allow the operator to create a target.
6. Allow the operator to drop a target from the system.
7. Allow the operator to change data recording modes.
8. Enable/disable interrogation data recording.

4.8 TIMER COUNTDONW.

The Mode S transponders will have a timeout feature whereby they reset their state if no discrete interrogations are received for a period of 16 seconds. Resetting will involve setting the lockout state to unlocked and setting the acknowledgement request (AC) protocol to state 0. The air initiated downlink (B-bit) will not be affected.

Timer Countdown processes each track once a second. When it recognizes the timed out condition it resets the L, AR, and PB bits. The I bit is also reset to satisfy New Track Initiation. Adjacent ARIES Input performs a similar timeout function if all the timeout conditions are satisfied after receipt of the T bit from another site. Thus, a transponder times-out only when all sites agree it has timed out.

4.9 INTER-ARIES.

The ARIES software will have the capability of coordinating its activities with ARIES systems located at other Mode S sites for the purpose of testing the Mode S system in a netted or unnetted environment.

5.0 HARDWARE FABRICATION.

Currently two approaches of packaging the ARIES unit are being considered. They are shown on figures 5.1 and 5.2. Figure 5.1 depicts a three rack system. The tape drive and disk unit will be mounted together in one rack. The CPU and digital expansion chassis will be mounted in the second. The STU and all the analog circuitry will be mounted in the third rack. Figure 5.2 depicts a two rack system. One rack will house the tape drive, CPU, disk unit and the digital expansion chassis. The other rack will house the STU and all of the analog circuitry. In addition each system will contain a video display terminal and line printer as separate peripherals. The actual approach taken will be determined by the CPU selected.

Improvements to system reliability will concentrate in three general areas:

1. Separation of major functions
2. Minimization of interconnections
3. Improvements in design

Area one will be achieved by keeping the ARIES computer separate from the rest of the ARIES unit, i.e., no ARIES digital devices will be mounted within the ARIES computer chassis. Instead, these devices will be contained in their own separate

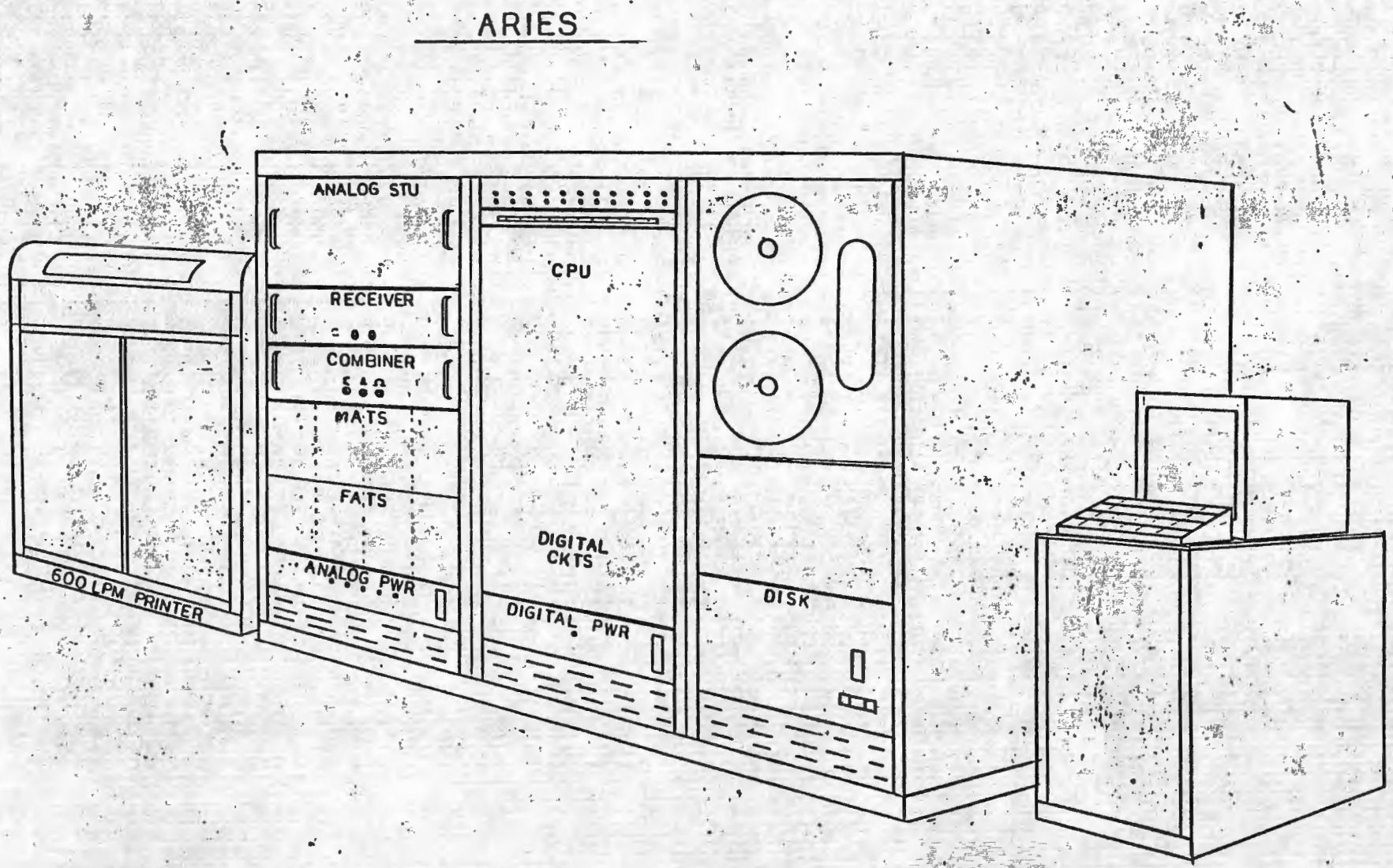


FIGURE 5.1. ARIES THREE RACK LAYOUT

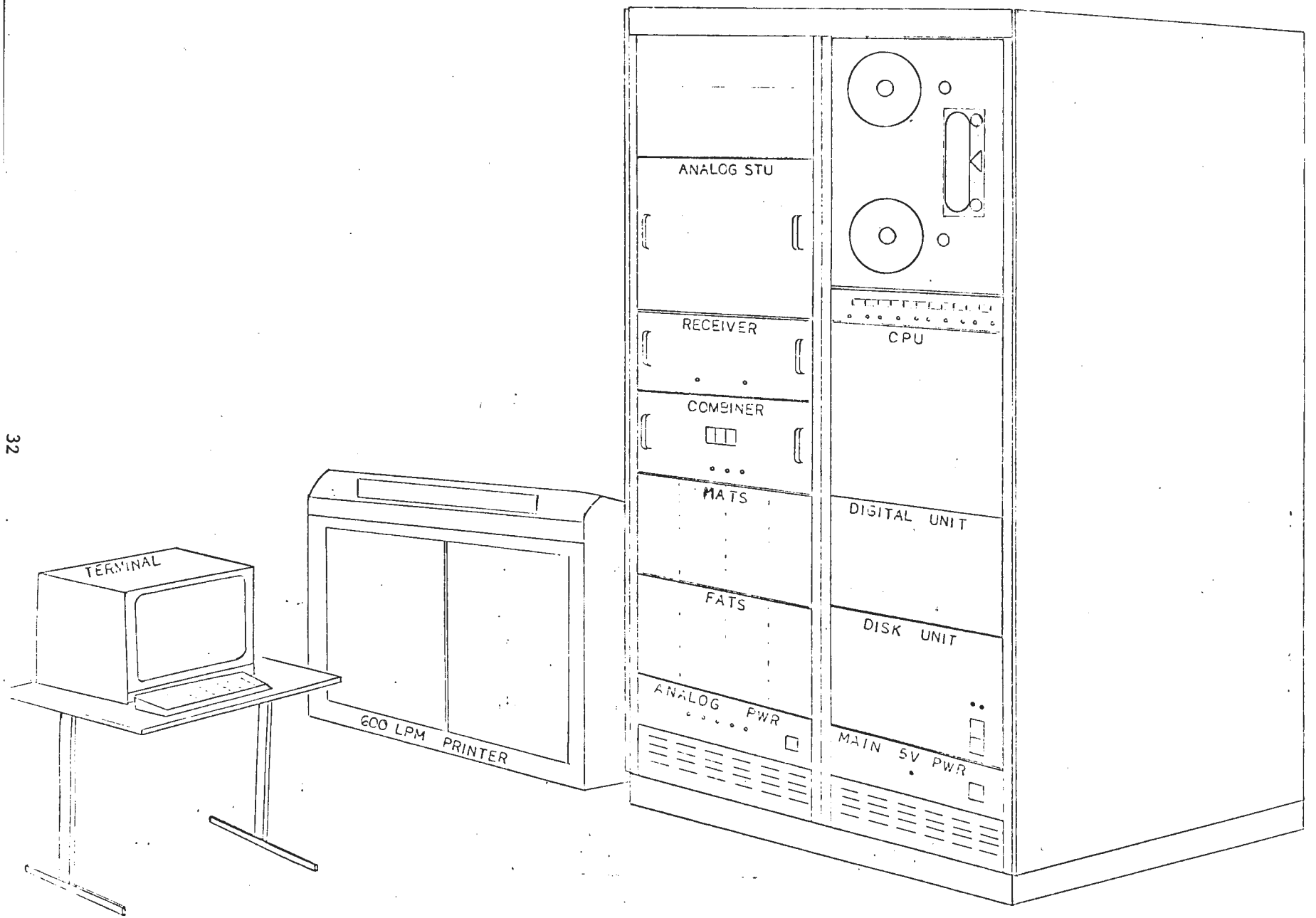


FIGURE 5.2. ARIES TWO RACK LAYOUT

expansion chassis. This chassis will be connected to the ARIES computer via a single cable or other suitable interface. This scheme will allow the separation of the computer and the hardware by a single disconnect, thus allowing a fault to be isolated between the two.

Area two will be achieved by combining, wherever possible interrelated digital hardware functions on to a single circuit card, thus reducing the amount of interconnections from function to function. An example will be to combine the functions of the FAT controller, it's interface to the computer, and the RPG on the same circuit card, thus eliminating any cabling and backplane wiring between these functions.

The third area will be achieved through the use of large and medium scale integration wherever possible to minimize component count and improve system performance. Also, extensive diagnostic paths will be provided within the hardware for isolating faults at the lowest possible level.