REPORT NO. FAA-RD-76-16

DIGITAL TONE RANGING MODEM
Design and Implementation

P. G. Mauro

U.S. Department of Transportation
Transportation Systems Center
Kendall Square
Cambridge MA 02142

MAY 1976

FINAL REPORT

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
Systems Research and Development Service
Washington DC 20591

Technical Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
FAA-RD-76-16		

4. Title and Subtitle	5. Report Date
DIGITAL TONE RANGING MODEM Design and Implementation	May 1976
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
P. G. Mauro	DOT-TSC-FAA-75-24
9. Performing Organization Name and Address U.S. Department of Transportation Transportation Systems Center Kendall Square Cambridge MA 02142	10. Work Unit No. (TRAIS) FA611/R6108
	11. Contract or Grant No.
12. Sponsoring Agency Name and Address U.S. Department of Transportation Federal Aviation Administration Systems Research and Development Service Washington DC 20591	13. Type of Report and Period Covered Final Report July 1971 - June 1972
	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

This report describes a digital ranging modem implementation based on side-tone ranging concepts.

The ranging technique implemented and tested in the DOT/TSC avionics laboratory has direct application to the AEROSAT surveillance system. The performance of a breadboard unit was observed in the laboratory as well as under actual aeronautical and maritime experiments conducted with the NASA ATS-6 satellite.

The technique demonstrated an acquisition probability of 0.98 for a signal-to-noise power density ratio, C/No, of 37 dB-Hz.

The ranging precision of the modem (for C/No>50 dB-Hz) is less than 66 meters.

Circuit schematics, test data, test results and analyses are included in this report along with recommendations for future applications of the demonstrated hardware.

17. Key Words	18. Distribution Statement
Ranging Modem ATS-F Position Determination Side Tone Ranging ATS-6 Satellite	DOCUMENT IS AVAILABLE TO THE PUBLIC THROUGH THE NATIONAL TECHNICAL INFORMATION SERVICE, SPRINGFIELD, VIRGINIA 22161

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	70	

Form DOT F 1700.7 (8-72) Reproduction of completed page authorized

PREFACE

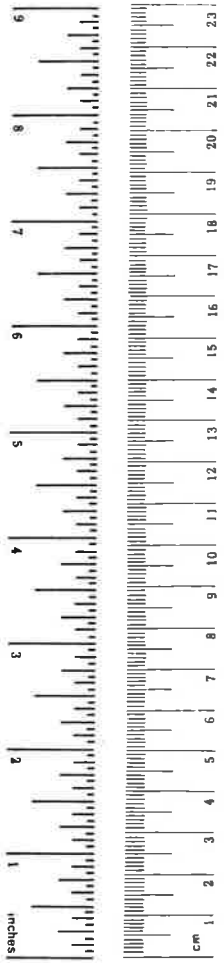
The work described in this report was performed in the context of an overall program at the Transportation Systems Center (TSC) supporting system design and development, avionics design, and test evaluation programs that influence the design of an aeronautical satellite system (AEROSAT) for an en-route-over-ocean-traffic, advanced air traffic control system.

This program is sponsored by the Department of Transportation through the Federal Aviation Administration (FAA), Systems Research and Development Service.

METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
		AREA		
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	square yards	0.8	square meters	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C



Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F

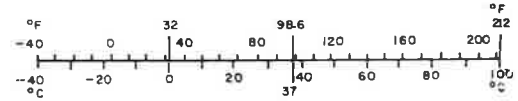


TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

LIST OF ILLUSTRATIONS

1. ATS-6 DIGITAL RANGING MODEM DESCRIPTION

1.1 BACKGROUND

The ATS-6 Digital Ranging Modem was designed to experimentally verify a ranging technique originally analyzed by J.J. Stiffler,[1] and later investigated by Thompson, Ramo and Woolridge (TRW) under a National Aeronautics and Space Administration - Electronics Research Center contract.[2]

Stiffler showed that in a tone ranging system, the optimum rate of information transfer would be achieved if a 2:1 tone ratio was used.

TRW's study led to a particularly simple implementation scheme. In essence, it is a simple way of digitally generating and detecting signals used for sidetone ranging.

In a separate study at TSC, a ranging modem was designed, implemented and tested.[3] This modem operated at baseband and used analog techniques for clocktone processing. The ATS-6 modem was developed subsequently using all digital techniques for ranging signal processing.

In addition, a phase-modulated 70 MHz signal is generated for transmission to the spacecraft, and a coherent demodulator is provided for demodulation of the received signal.

1.1.1 Simplified Description of Operation

The ATS-6 Digital Ranging Modem can be separated into the following four parts:

a. Ranging Code Generator

b. Phase Modulator

c. Coherent Demodulator

d. Ranging Code Processor.

The Ranging Code Generator provides a set of squarewaves that are generated by successive 2:1 frequency division from the system

frequency standard. The highest frequency tone of a given set is designated the clocktone. In the phase modulation process it can be weighted relative to the other tones to optimize the distribution of power. The complete set of weighted tones are combined together in a majority logic combiner. In the phase modulator, the combined tones phase-modulate a 70 MHz carrier. This carrier is then externally translated in frequency to the desired output, and transmitted to the mobile via satellite.

At the mobile terminal, a receiver filters, amplifies and down-converts the received signal. This receiver output, at 70 MHz, is then supplied to the coherent demodulator. The demodulator provides a phase-locked loop, which locks to the carrier component of the received signal and provides a reference for coherent phase demodulation of the ranging signal. The demodulated output then, is a replica of the tone generator output, to which has been added receiver noise.

In the ranging code processor a digital phase-locked loop extracts the clock tone which is used as the input to a digital frequency divider. Successive division by factors of two produces another set of square-wave tones, identical in frequency to the transmitted tones but with a phase ambiguity of 180°. In the processor, these tones are digitally compared with their equivalent in the received signal, and a sequential set of binary decisions are made to resolve the phase ambiguity. The result, then is a set of tones which are identical in frequency and phase with the received set, but which have been digitally filtered for signal-noise ratio improvement. A counter then measures the time delay between the processor's output, and a local phase reference to determine the one-way relative range.

1.1.2 Code Properties

The code sequence chosen is generated from a series of coherent square waves which are harmonically related by multiples of two. These are refered to as the "components" of the code, or "ranging tones."

The binary code is generated from the square waves by the following rule. During each bit time of the highest frequency square-wave or "top tone," the number of square-waves in binary state "zero" are subtracted from the number of square-waves in binary state "one."

If the result of this subtraction is negative, the code is put in the binary state "zero," and if the result is positive, the code is put in the binary state "one." The total number of square-waves can be kept odd to avoid a "zero" or an indeterminate subtraction result.

This code generating process has a bit rate equal to twice the highest square-wave frequency, and a code period equal to the period of the lowest frequency. The code displays mirror symmetry about the center of its period.

Of great importance is that the code contains elements of each of the input frequencies and, in the most straightforward system, each component represents $\frac{1}{n}$ of the signal power, where n is the number of components. This makes it possible to correlate the code against any of its components. The limiting action, which was needed to produce a binary output, introduces other elements into the code so that correlation with the original components is reduced somewhat. The reduction, however, is only about 2 dB, which for this design is not considered significant.

The code used in the model implementation encompasses twelve components (n = 12) ranging from 156.25 kHz to 76.5 Hz. Thus, the bit rate is 312.5 kilo bits/sec and the ambiguity range is in excess of 2100 nmi. The clock and ranging tones are derived from a stable 5 MHz source by digital division.

1.1.3 System Description

For any application, a system built to utilize the code as described above will embody the principles of operation discussed briefly here.

The processor will acquire the transmitted code and output its lowest frequency component. This square-wave is then compared in phase with a locally generated square-wave.

A time interval meter providing the necessary resolution is a convenient means of measuring the relative phase. This phase represents both the absolute time difference between the clocks and the propagation time.

From the foregoing description, it is clear that the basic system principles are no different from those of any ranging system. The important area of difference is in the process referred to as "acquiring the transmitted code." In this system, the acquisition is accomplished in sequential steps or stages starting with the top frequency or clock component. A digital phase-lock loop tracks this component, filtering out the rest of the code and the additive noise. When lock is achieved, the phase of the transmitted signal is known to be one of the 2^{n-1} possible phases of the top frequency component that occur within one cycle of the lowest frequency component, where n is the number of code components.

The received code is now correlated with the first subfrequency (second highest frequency) and this subfrequency is derived from the phase-locked clock component. Accordingly, it is coherent with the incoming code with a phase ambiguity of 180 degrees and will correlate to a maximum value over one code period. The correlation will be either positive or negative in sign and, if it is the latter, the derived subfrequency is inverted in sign (shifted 180 degrees) and the number of possible phases is now reduced to 2^{n-2}. By performing a sequence of n-1 similar subfrequency correlations, all phase uncertainties are removed and the lowest frequency tone counted down from the locked oscillator will be in phase with the received code. It can then be compared to the local clock for a relative-phase measurement, or retransmitted to the source for a round-trip measurement.

The important feature of this system is that acquisition consists of locking to the clock tone and then making n-1 binary decisions in sequence. With a pseudo-random (PRN) code of the same

length, and with no a priori knowledge of phase, it is possible that 2^{n-1} decisions would have been necessary for acquisition. Thus under the same set of conditions, the acquisition time of the modem is considerably shorter than its PRN counterpart.

Another feature of equal significance is that although the phase measurement is made at the lowest subfrequency, the phase resolution is derived from the clock tone. This implies that phase differences will be measured with a precision equivalent to the phase jitter on the clock tone, but with a range ambiguity equal to the wavelength of the lowest frequency tone.

Three figures, presenting different views of the ATS-6 Digital Ranging Modem, are included on pages 1-6, 1-7, and 1-8. Figure 1-1 is a three-quarters view of the ATS-6 Digital Ranging Modem. Figure 1-2 is a front panel view. Figure 1-3 is an interior view.

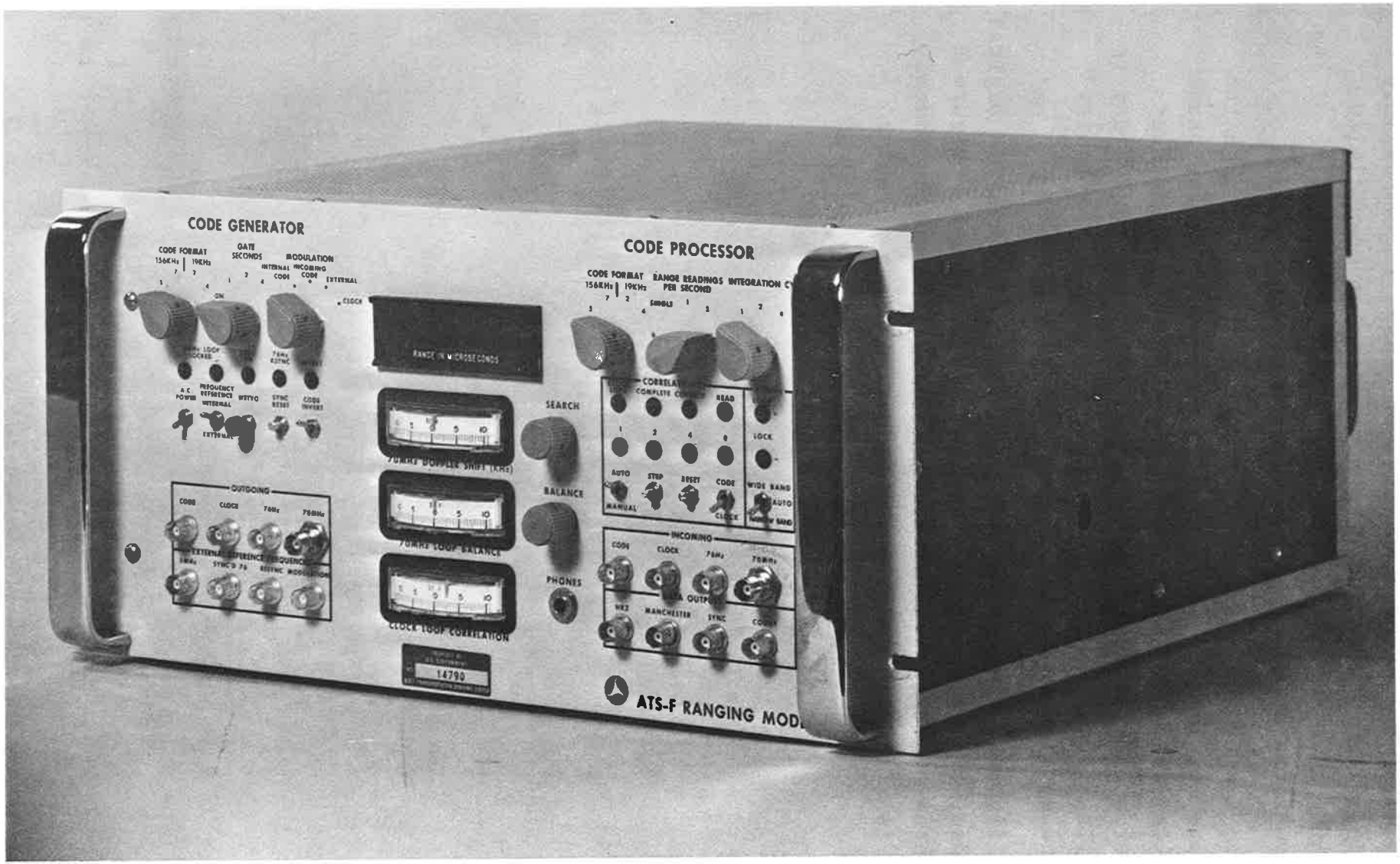


Figure 1-1. Three-Quarters View of the ATS-6 Digital Ranging Modem

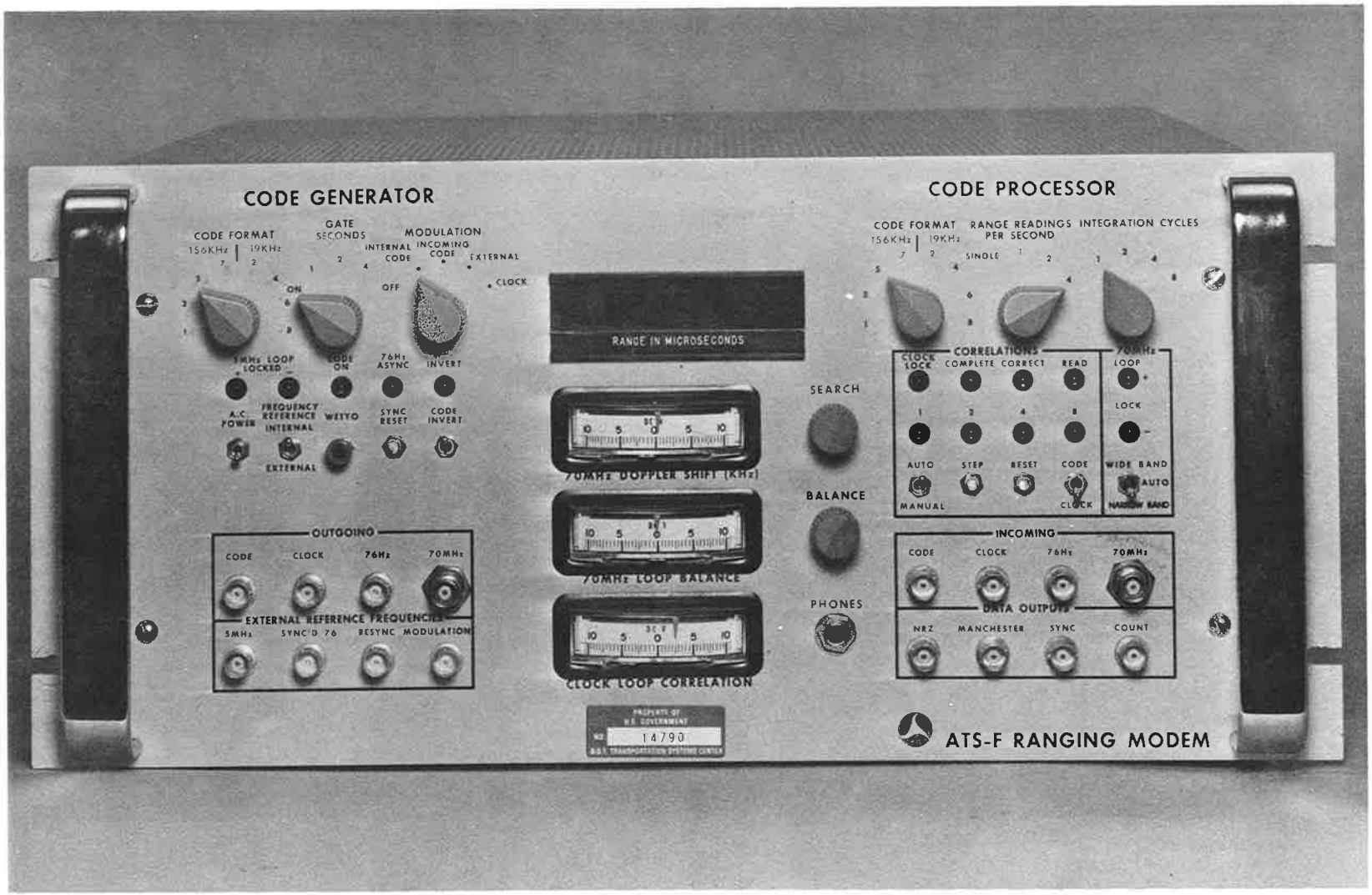


Figure 1-2. Front Panel View of the ATS-6 Digital Ranging Modem

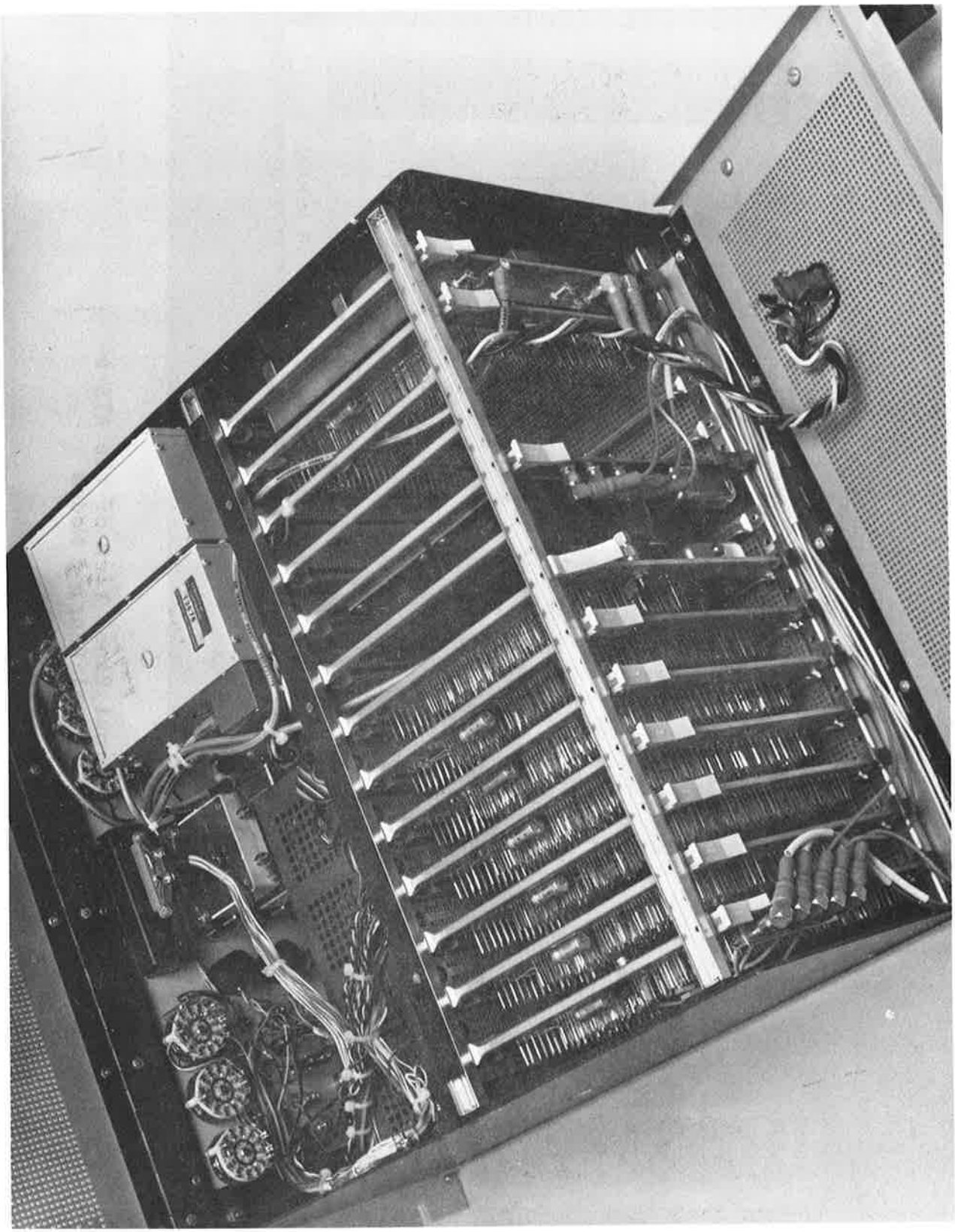


Figure 1-3. Interior View of the ATS-6 Digital Ranging Modem

2. ATS-6 RANGING CONFIGURATION

For the ATS-6 tests, the system was configured as shown in Figure 2-1. Ranging experiments were deliberately limited to one way ranging, i.e., a signal, originating at the ground station, is transmitted through the satellite and received at the two mobile terminals. The time delay of this signal is measured by comparison with a local onboard clock. If all clocks were synchronized, it would be possible to make absolute ranging measurements, but, because this was not an objective of the experiment, the additional complexity required was rejected in favor of simple relative range measurements. Three identical modems each containing a code generator and code processor were used in the ATS-6 tests with one located at the NASA ground station at Rosman, North Carolina; one model onboard a Coast Guard cutter, and the third modem onboard an FAA aircraft. Range measurement data were recorded onboard the cutter and the aircraft on analog tape. Four different codes were employed during the course of the experiments. The results are presently being analyzed, and will be available in a subsequent report.

2.1 RANGING CODE GENERATOR

The ranging code generator, as shown in Figure 2-2, accepts a 5 MHz reference frequency, and divides this successively by two, to a final output of 76.294 Hz. This process generates the components required to produce the ranging code. The ranging code is formed from a subset of the code generator outputs. First a highest frequency component, known as the clock tone is generated. The clock tone frequency is determined by the available bandwidth and the required precision. The ATS-6 modem provides two clock frequencies, 19.531 kHz and 156.25 kHz. The other code components are then 1/2 f_{CL}, 1/4 f_{CL}, etc., down to the lowest code component which is 76.294 Hz (in all cases).

The ranging code is formed by hard limiting the algebraic sum of the code components. This is implemented digitally by forming

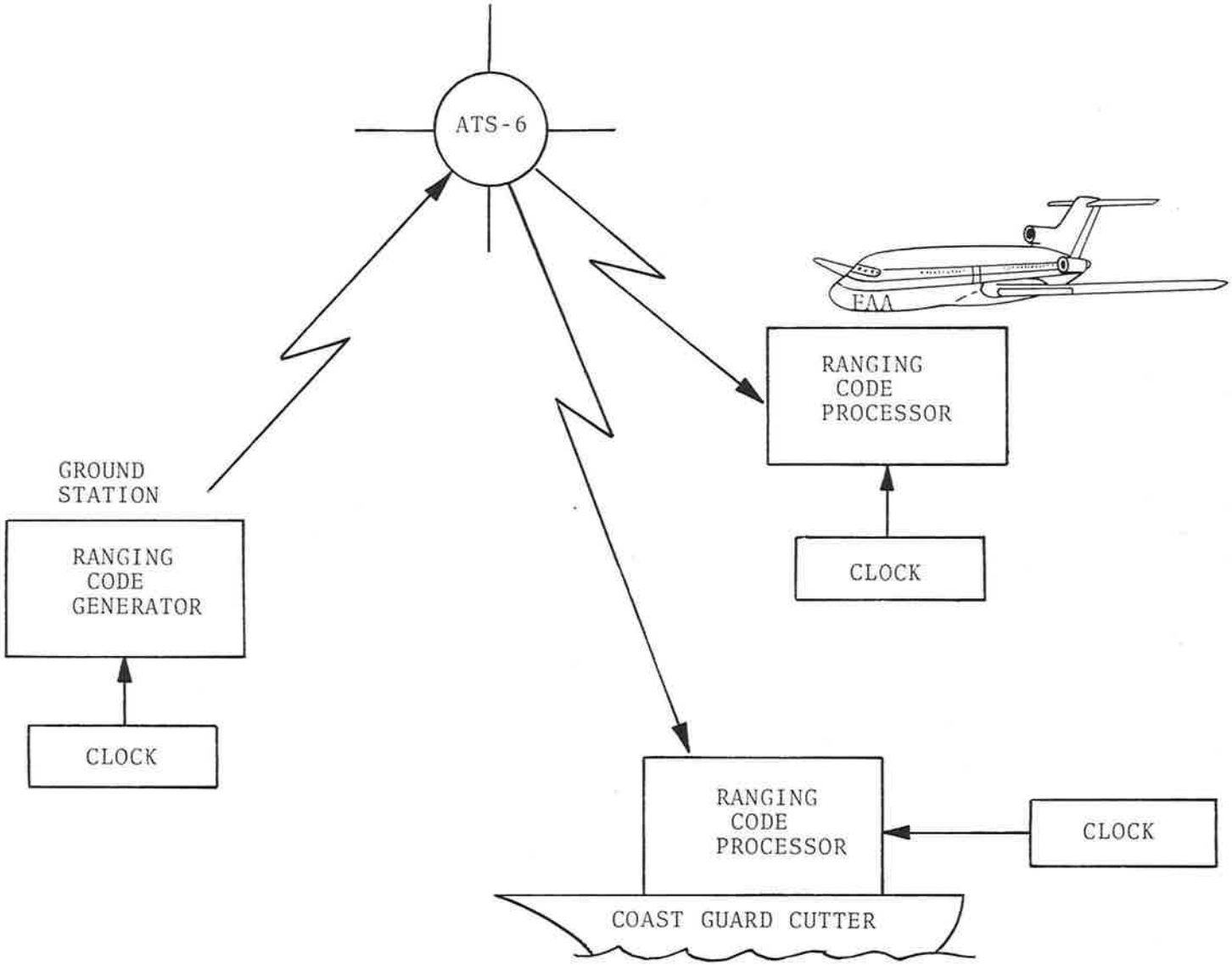


Figure 2-1. ATS-6 Ranging System (One Way)

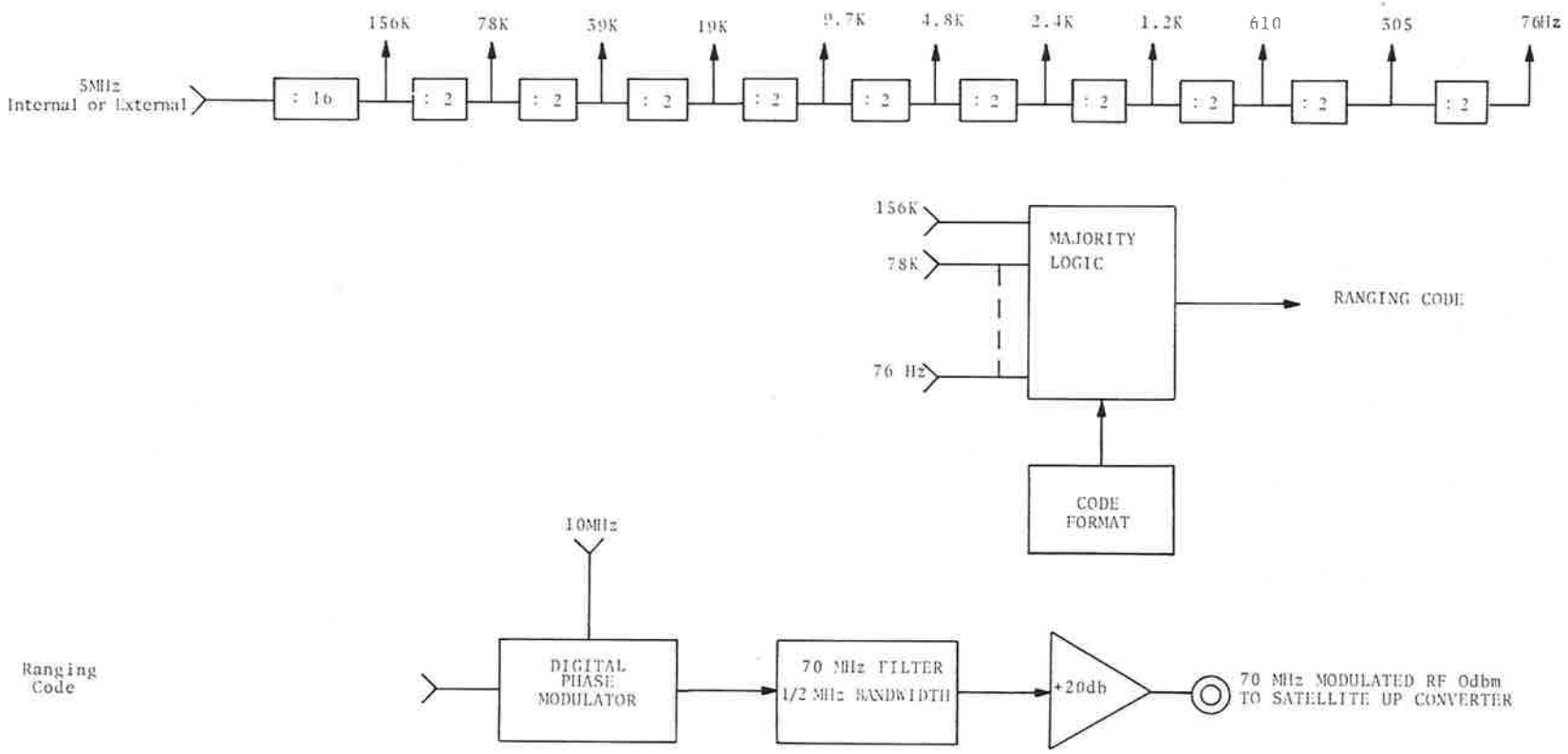


Figure 2-2. Ranging Code Generator Block Diagram

a majority logic sum of the components. In the summing process, different weights can be assigned to the clock tone, which has the effect of increasing clock tone energy, relative to the other code components. The summation must be in the form Code = a f_{CL} + b $f_{comp.}$ where a and b integers, a is the clock weighting and b represents the number of other code components. Practical considerations require the sum a+6 to be an odd integer otherwise the phase demodulator used for range code extraction in the receiver will encounter serious d.c. level shift problems. Thus, in the ATS-6 modem, with a clock of 156.25 kHz and a lowest component of 76.294 Hz, the design provides clock weightings of 2, 4, 6 or 8 while a clock of 19,531.25 Hz combined with the lowest tone of 76.293 Hz has clock weightings of 1, 3, 5 or 7. The different formats are selectable by front panel switch.

2.2 DIGITAL PHASE MODULATOR

The selected code is then phase-modulated on a 70 MHz carrier. The modulator is clocked by a 10 MHz square-wave. The square-wave transitions are advanced or retarded in phase at the code rate, thus generating true phase modulation. The 7th harmonic of the 10 MHz signal is selected by filtering, and amplified to the desired output level of 0 dBm. The amount of phase shift may be internally changed in binary increments, to set the modulation index.

2.3 COHERENT DEMODULATOR

The Coherent Demodulator is a 70 MHz phase-locked loop. The loop locks to the 70 MHz carrier component of the received signal. Referring to Fig. 2-3, the loop is locked around an internal IF frequency of 11 MHz. The IF is generated by the difference between the loop VCo frequency of 81 MHz, and the incoming frequency (70 MHz). The loop bandwidth is approximately 30 Hz. The loop incorporates a wide-band phase demodulator at 11 MHz, whose output is the demodulated ranging signal.

ATS-6 code components are present in Figure 2-4.

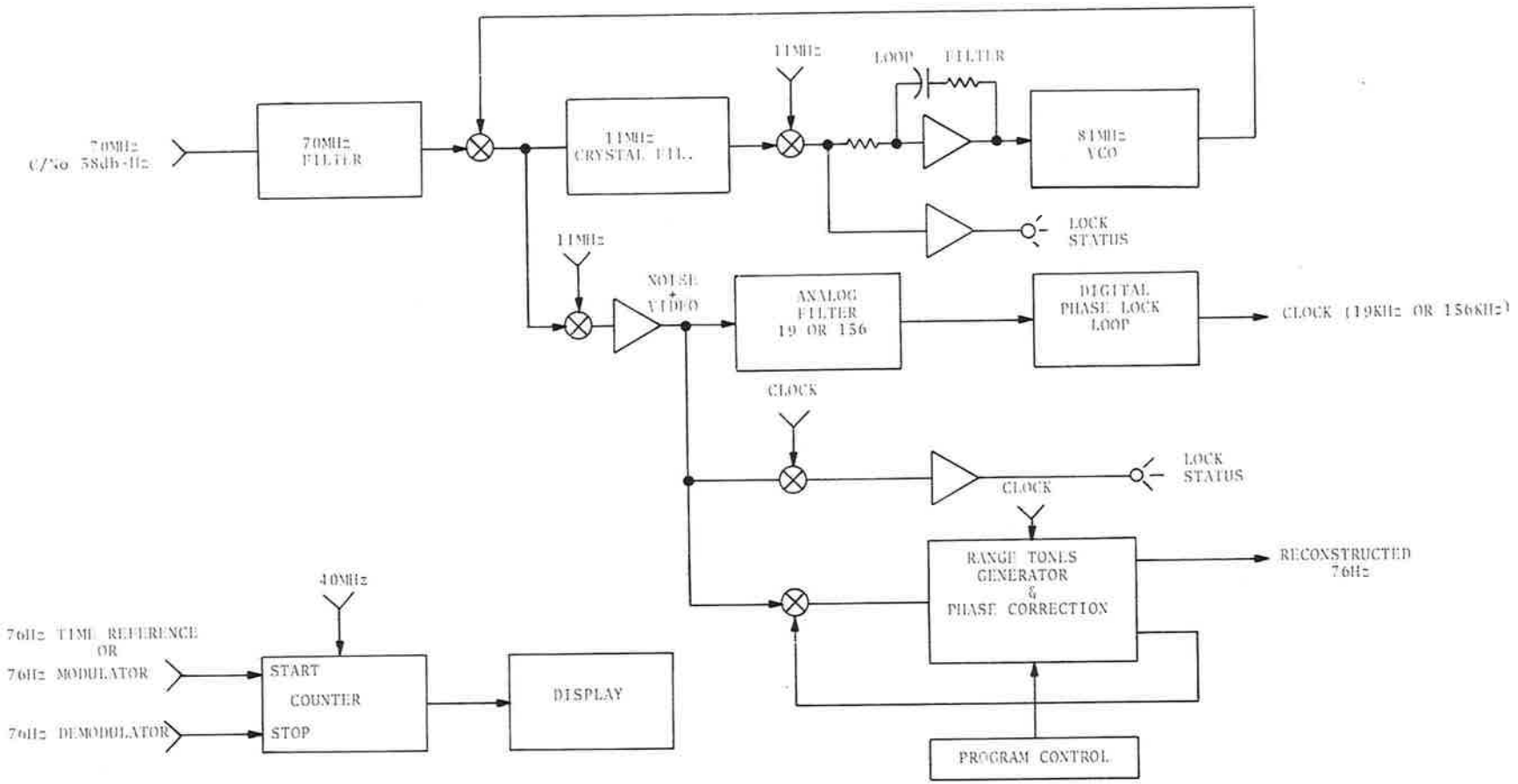


Figure 2-3. Ranging Code Processor Block Diagram

Clock	156.250 kHz	19,531.25 Hz	1
Comp:	78.125 kHz	9,765.625 Hz	2
	39,062.5 Hz	4,882.8 Hz	3
	19,531.25 Hz	2,441.4 Hz	4
	9,765.625 Hz	1,220.7 Hz	5
	4,882.8 Hz	610.3 Hz	6
	2,441.4 Hz	305.1 Hz	7
	1,220.7 Hz	152.5 Hz	8
	610.3 Hz	76.293 Hz	9
	305.1 Hz		10
	152.5 Hz		11
	76.293 Hz		12

Figure 2-4. ATS-6 Code Components

2.4 RANGING CODE PROCESSOR

The processor input signal consists of the ranging information plus noise and can be a minimum of -26 dB signal-to-noise ratio. This signal is cleaned up in an analog filter centered at 19 or 156 kHz (depending on which clock tone is selected) before being fed into the digital phase lock 10 op. The digital loop performs the function of phase acquisition and tracking of the clock tone. The digital loop produces a replica of the transmitted clock tone, containing phase-noise ("jitter") resulting from system additive noise. This jitter represents the relative accuracy of the ranging processor. There is a lock status indicator which indicates acquisition and lock of the clock tone. When clock loop lock is complete, program control begins to correlate the internally generated range tones with the incoming code. Upon completion of code correlation, a correlation check is made by generating a replica of the acquired code, and correlating this with the received code. If correlation is correct, the "code correlation complete" light lights. The local code replica is then fedback to the processor input, where it is combined in an exclusive - OR with the input code. This results in code wipe-off of the input signal, such that the only component entering the system is the clock. In effect, the clock power has been increased by the square of the code correlation coefficient, resulting in improved signal-to-noise ratio, and less jitter.

2.5 SUMMARY OF CIRCUIT DESIGN BLOCK DIAGRAM DESCRIPTION

Refer to Figure 2-5 titled ATS-6 Ranging Modem Block Diagram, and begin with Board 6, the Ranging Code Generator. Five megahertz obtained either internally or externally is divided down by 16 binary stages to 76 Hz. Nine or thirteen of the above frequencies are combined with selectable weightings of the clock tone in a majority logic circuit to produce the ranging code. A more detailed explanation of this process is given in paragraph 2.7.

The locally generated code is fed to Board 7 where it phase modulates a 10 MHz carrier. The seventh harmonic is filtered out

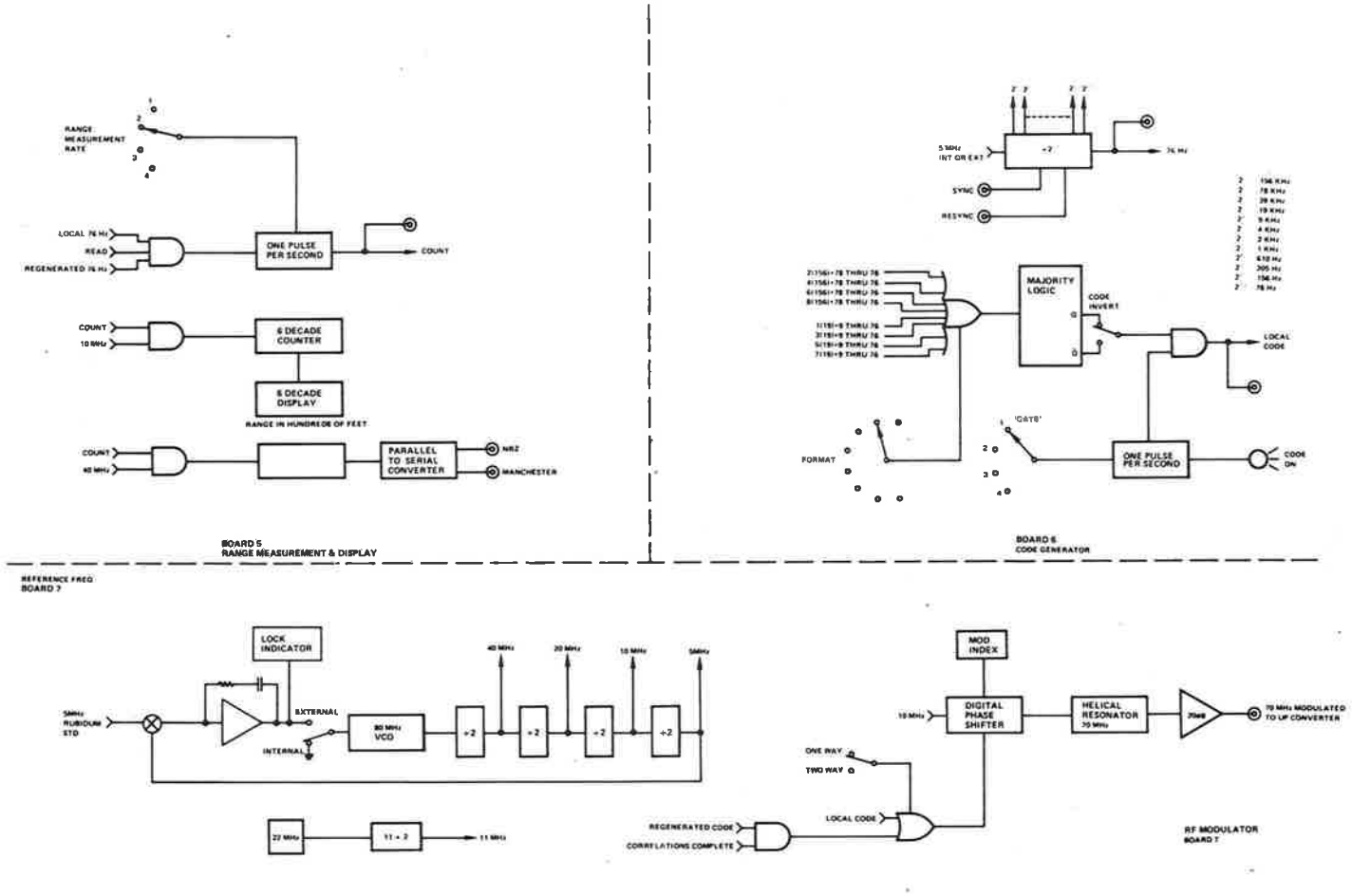


Figure 2-5. ATS-6 Ranging Modem Block Diagram

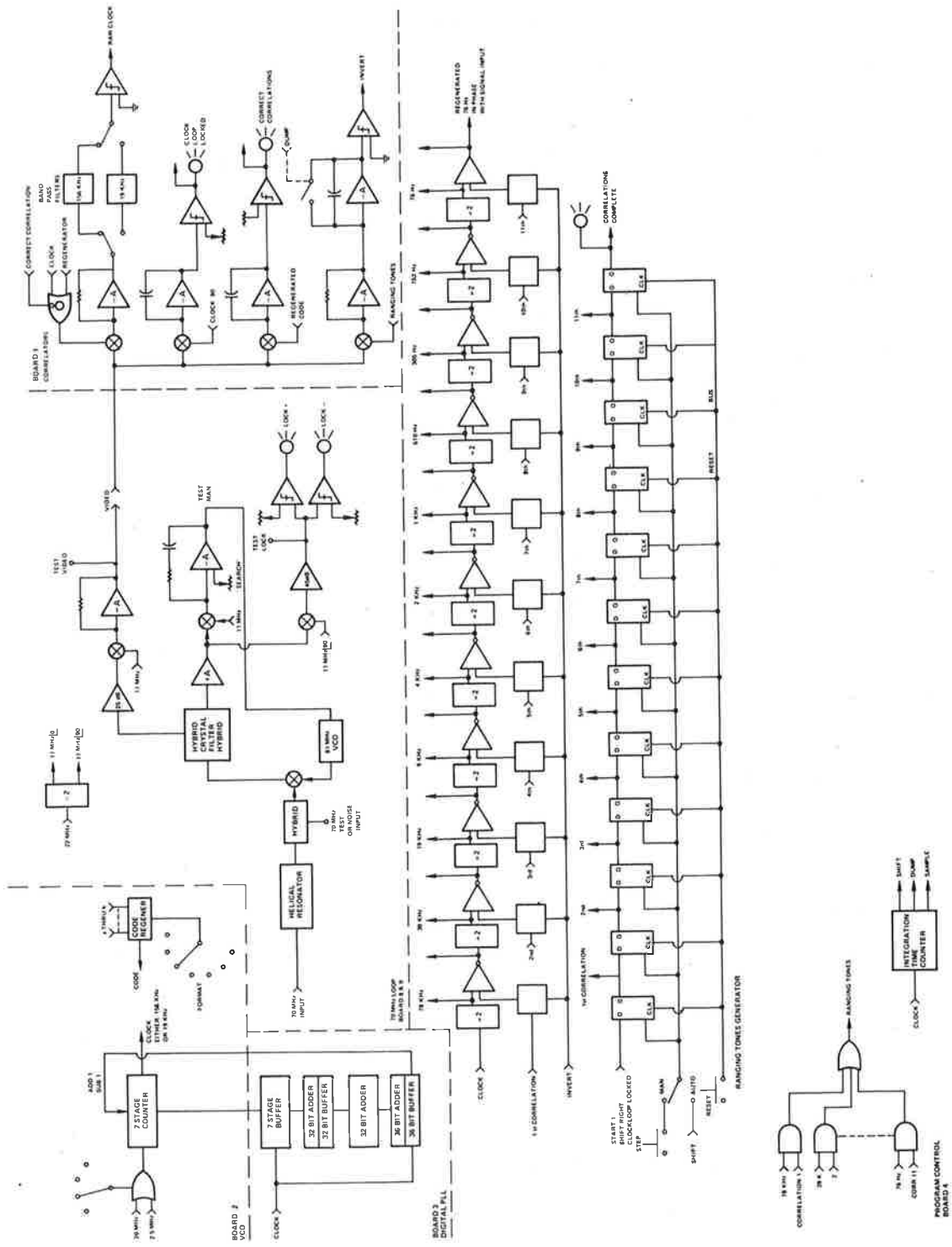


Figure 2-5. ATS-6 Ranging Modem Block Diagram (Continued)

of the 10 MHz carrier and amplified to produce a zero dBm 70 MHz phase modulated signal to drive the transmitter up-converter.

The 70 MHz IF frequency from the satellite down-converter is accepted by the 70 MHz loop located on Board 8 and 9. A wide passband sharp skirt filter shapes the incoming signal before it is mixed with the local VCO and locked by a conventional phase lock loop. The video information is demodulated, amplified and sent to Board 1 which contains the four video correlators to perform the following multiplications:

1. Incoming signal + local clock for the clock tracking loop
2. Incoming signal + local clock shifted by 90° for clock loop status indicator
3. Incoming code + each of the Ranging Tones successively for phase formation about the ranging tone
4. Incoming video + the regenerated code for indication that the correct correlations have been made.

Following the first correlator in the clock loop, preliminary analog bandpass filtering of the clock frequency improves the signal-to-noise ratio of the signal fed to the digital PLL. This signal is threshold detected and fed to Board 3 where it serves as clocking for digital phase lock loop. Part of this loop is contained on Board 2. A detailed description of loop operation is contained in paragraph 2.4.

The Program Control is located on Board 4. It provides the proper sequencing of correlation tones, interrogation, shifting and dumping operation. It also generates system timing waveforms. On the same board is located the Ranging Tones Generator which divides the acquired clock by 212 to generate the frequencies representing the ranging tones. Each tone is gated out separately and sequentially to be correlated against the incoming signal through the proper selection matrix.

Board 5 contains the range measurement and display circuitry. The time interval between the local 76 Hz and the incoming 76 Hz waveforms is counted by both a 10 MHz counter and a 40 MHz counter.

The 10 MHz counter drives a front panel display to observe system operation. The 40 MHz counter generates a Manchester encoded data stream for recording purposes.

Reference frequencies used throughout the modem are generated on Board 7. Accepting either an internal or external 5 MHz standard which is phased locked to an internal 80 MHz VCO, the following reference frequencies are obtained: 40, 20, 10 and 5 MHz. A second internal 22 MHx oscillator is divided in half to provide the 11 MHz required for the RF loop.

3. DETAILED CIRCUIT DESCRIPTION

3.1 PHASE DETECTORS, CORRELATORS, STATUS INDICATORS BOARD 1 (FIGURE 3-1)

The differential video signal from the RF loop is fed to Board 1 where it goes directly to four switching type phase detectors, packages 5, 6, 7 and 8. Each of these switches is driven with a multiplying signal obtained from various locations throughout the processor. Each of these switches is followed by a differential operational amplifier to obtain a single ended output.

For the first correlator, package 5, the switches are off until the code has been acquired and the correlations made correctly, until then, the balanced differential signal being fed to package 5 is simply converted to single end in package 17 and fed to the two bandpass filters. These filters improve the signal-to-noise ratio of the two clock tones. The outputs of both filters are amplified having a gain of 100. For the higher (156 kHz) clock tone, an ANALOG Device AD507 operational amplifier is used. For the lower (19 kHz) clock tone, Signetics 531 amplifiers are adequate. The signal is then threshold detected in the voltage comparator packages 29 and 40. The jittery square-wave representing raw clock is now fed to one shots, packages 37 and 38. These allow an adjustment in the phase of each clock to be made. A reed relay, package 28b, selects which of the clock frequencies is being used.

When an incoming code has been acquired with all of the correlations made correctly, a regenerated code exclusively ORed with clock in package 3a is allowed to drive the phase detector switch 5 through AND gating 4a and 4b. The multiplication of incoming code with regenerated code exclusively ORed with clock, provides a signal at the output of switch 5 which is pure clock. This greatly enhances the signal fed to the bandpass filters and increases the signal strength throughout the loop. The loop now locks with much less jitter. However, there remains the problem of phase shift through the clock loop which is different for this

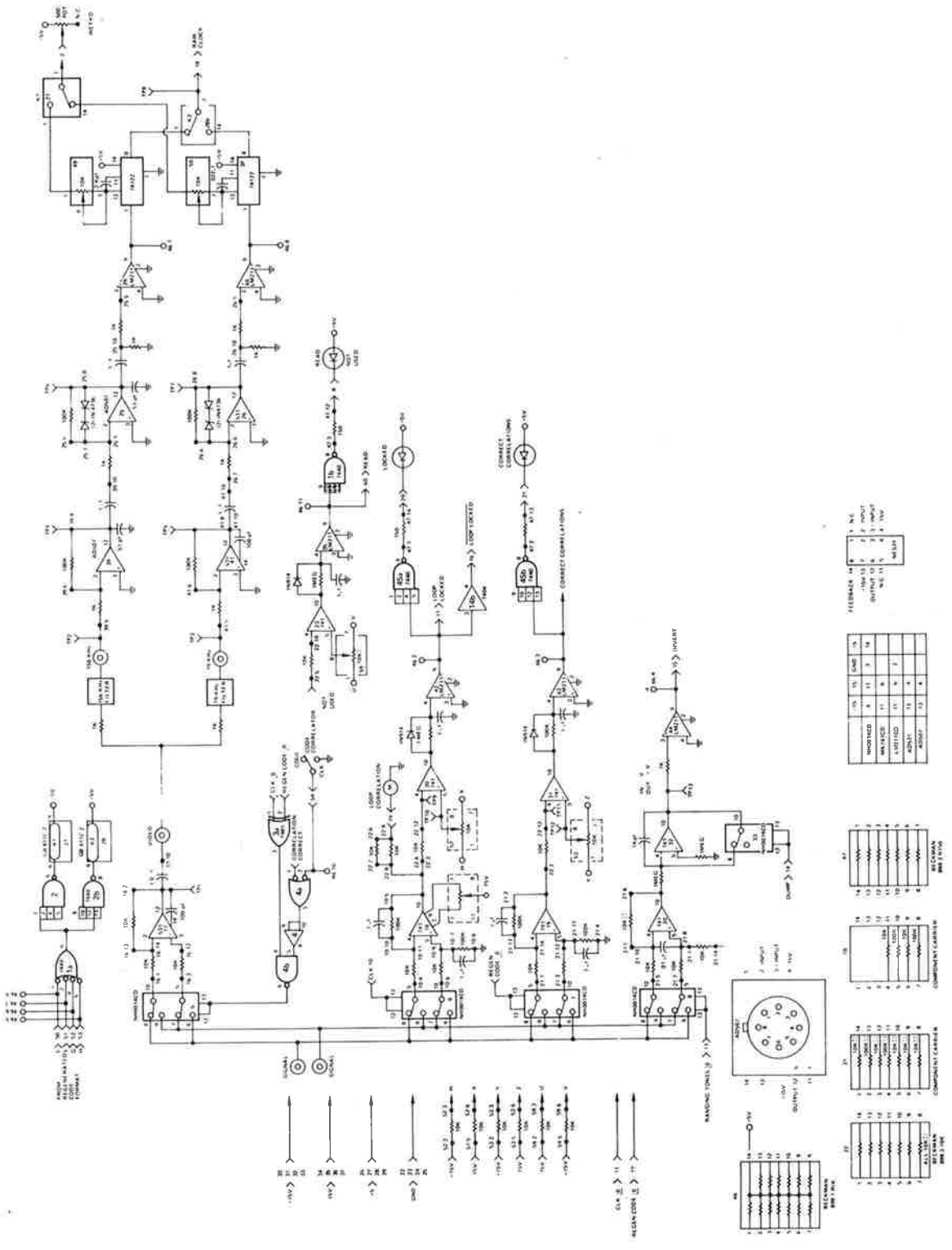


Figure 3-1. ATS-6 Ranging Modem MOS Switching Correlators - Board 1

mode of operation vs the mode where switch 5 is disabled. This problem will be investigated further.

The loop status indicator begins with switch 6 which multiplies incoming video with acquired clock in phase with the incoming clock, therefore, the output of this phase detector followed by a differential amplifier will be a high positive voltage proportional to the signal strength of the incoming video. This is threshold detected by an operational amplifier (package 30) whose saturated output is $\pm$ 15 volts providing a large charging voltage for the following RC network. The capacitor is charged through the 100 K resistor and discharged quickly through the diode, insuring the charging time is much longer than the discharge time and allows time delay sufficient to give the loop adequate time to lock. Therefore, it the clock loop were to slip one cycle, the status indicator would respond very quickly and force the modem to reacquire the incoming code, hence the indicator represents the true condition of the loop.

The correlations status indicator begins by multiplying incoming signal with the regenerated code in switch 7. The output of differential amplifier 19 is threshold detected by amplifier 31 and the operation is identical to the above circuit with the exception that now the threshold is set higher since we are multiplying identical signals and expect higher correlation.

The ranging tones correlator begins with switch 8 multiplying the incoming signal with each of the ranging tones sequentially. The multiplication takes place over 1, 2, 4 or 8 code periods, the output of the multiplier switch 8 is differentially amplified and converted to single end and integrated in package 32. The capacitor of this integrator is dumped through switch 33 at the end of each integrating cycle. The output of the integrator is threshold detected by package 44. Just before dump time, the output of this comparator is interrogated to determine if the correlation has been positive or negative and this information is fed to the program control board. All analog multipliers on this board are implemented with the exclusive-Or function.

3.2 DIGITAL PHASE LOCK LOOP BOARDS 2 AND 3 (FIGURES 3-2 AND 3-3)

Boards 2 and 3 contain the digital Phase Lock Loop which acquires and tracks the incoming clock tone. The loop is completely digital, utilizing digital logic to simulate traditional analog circuit functions such as the VCO, loop filter and phase detector; integration is performed by digital accumulation and multiplication is done by shifting.

Figure 3-2 shows the digital PLL block diagram consisting of six major elements: the input filter, limiter, readout buffer, loop filter, digital accumlator, counter control logic and variable counter.

The variable counter in conjunction with the digital accumulator and counter control logic is the loop VCO. The readout buffer, the phase detector and the digital loop filter provide the appropriate transfer function for the second order loop. The variable counter is a seven stage binary counter. If no special control is applied, the counter divides a 40 MHz reference frequency by 128. Two special modes allow the counter to drop one count, or add one count. By controlling the counter mode, the output phase of the counter may be advanced by adding a count, retarded by dropping a count, or left unchanged.

The state of this counter is the instantaneous phase of the clock in twos complement arithmetic. This phase is read into the buffer at zero crossings of the input clock, so the value in the buffer is the phase difference between the local clock and the incoming clock, in two compliment format. Therefore, the readout buffer performs the phase detector function. The combined gain of the variable counter is one, that is, an advance or retard of one count causes the phase read into the buffer to be advanced or retarded by one count, respectively.

The digital loop filter is implemented as shown in Figure 3-3. In particular, the integration is performed by the digital accumulator where the sampling rate is 156.25 thousand samples per second. This accumulator contains the loop frequency command word for the

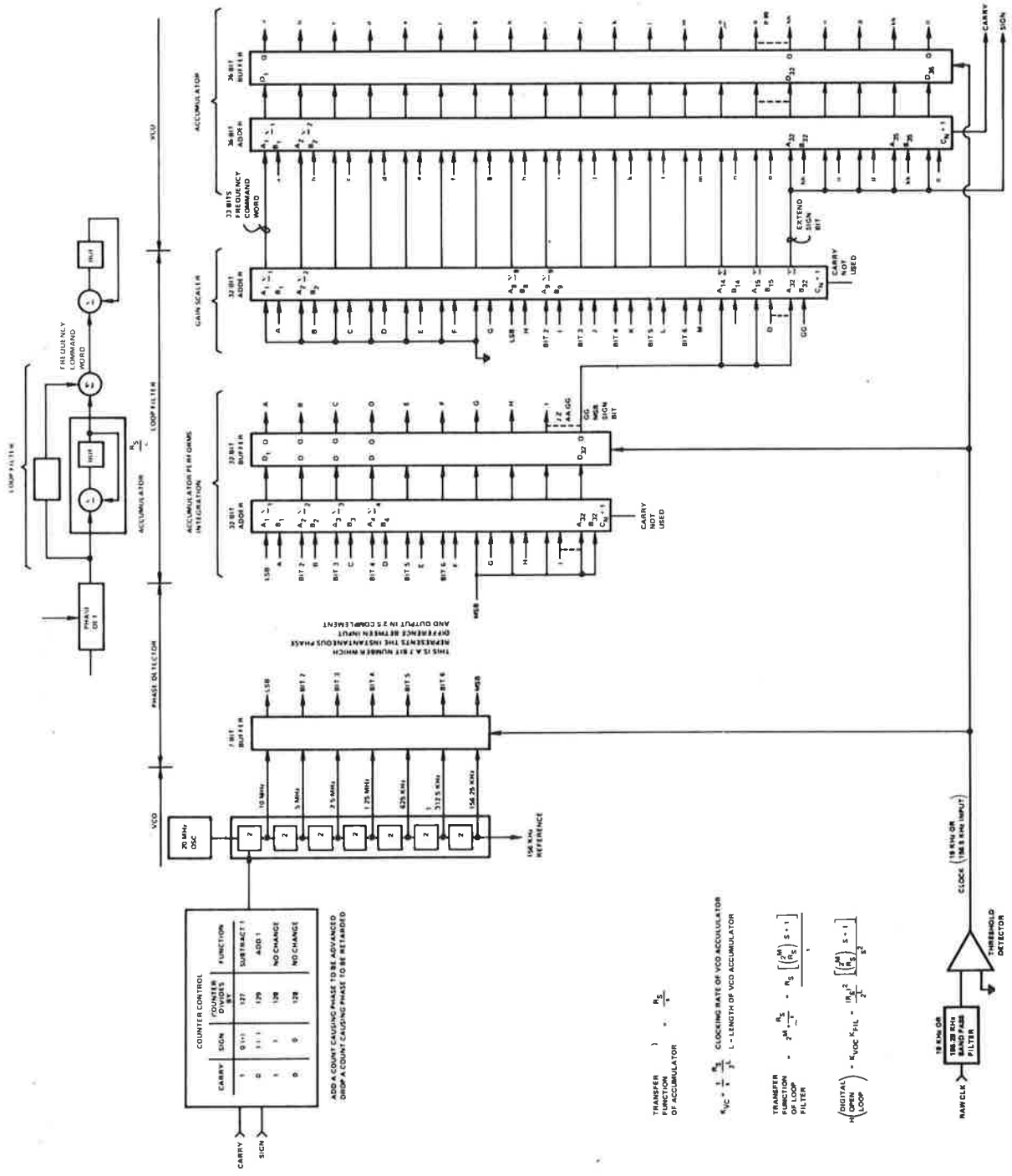


Figure 3-2. ATS-6 Ranging Modem Digital Loop Block Diagram

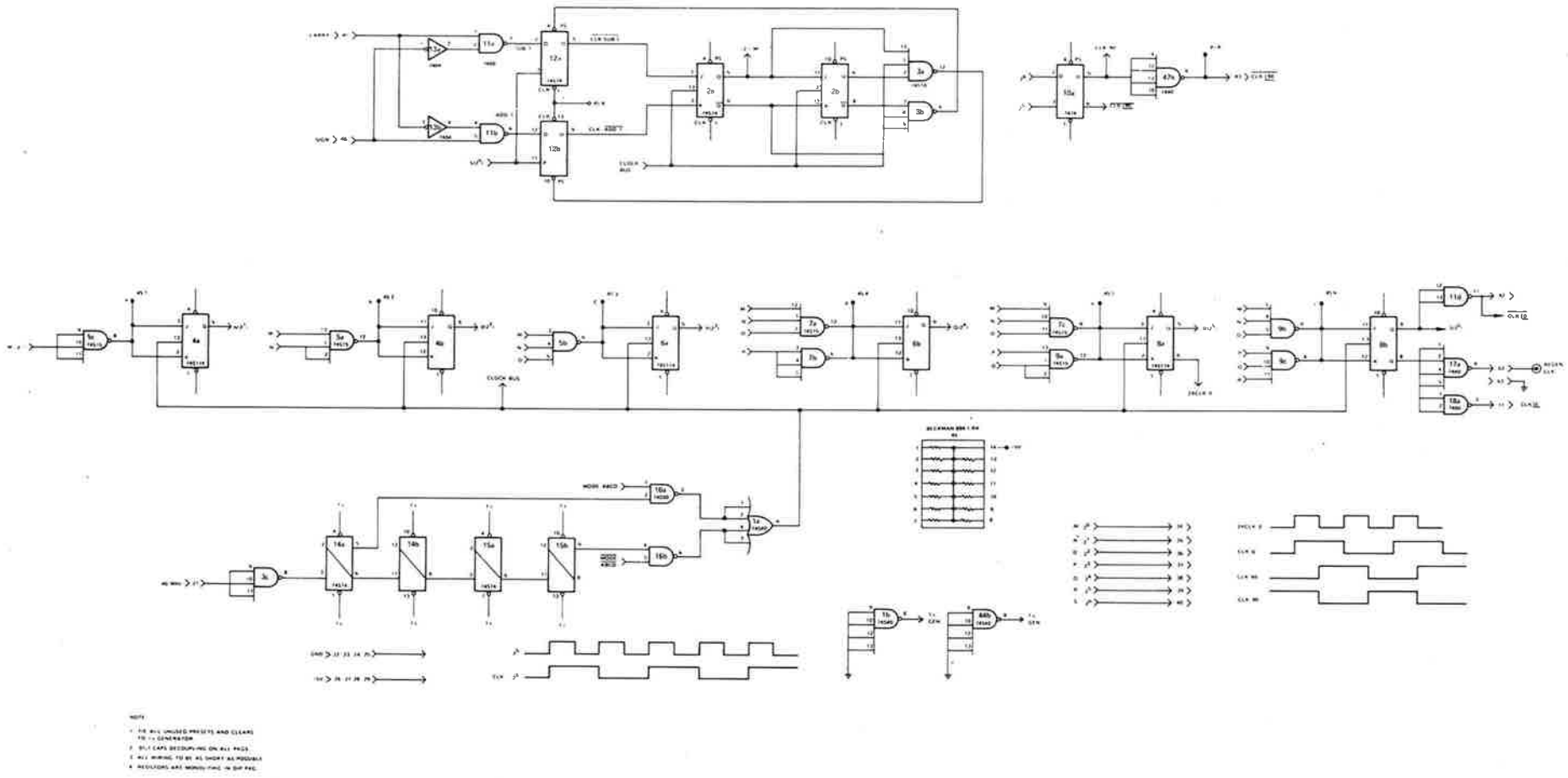


Figure 3-3a. ATS-6 Ranging Modem Digital Loop - Board 2

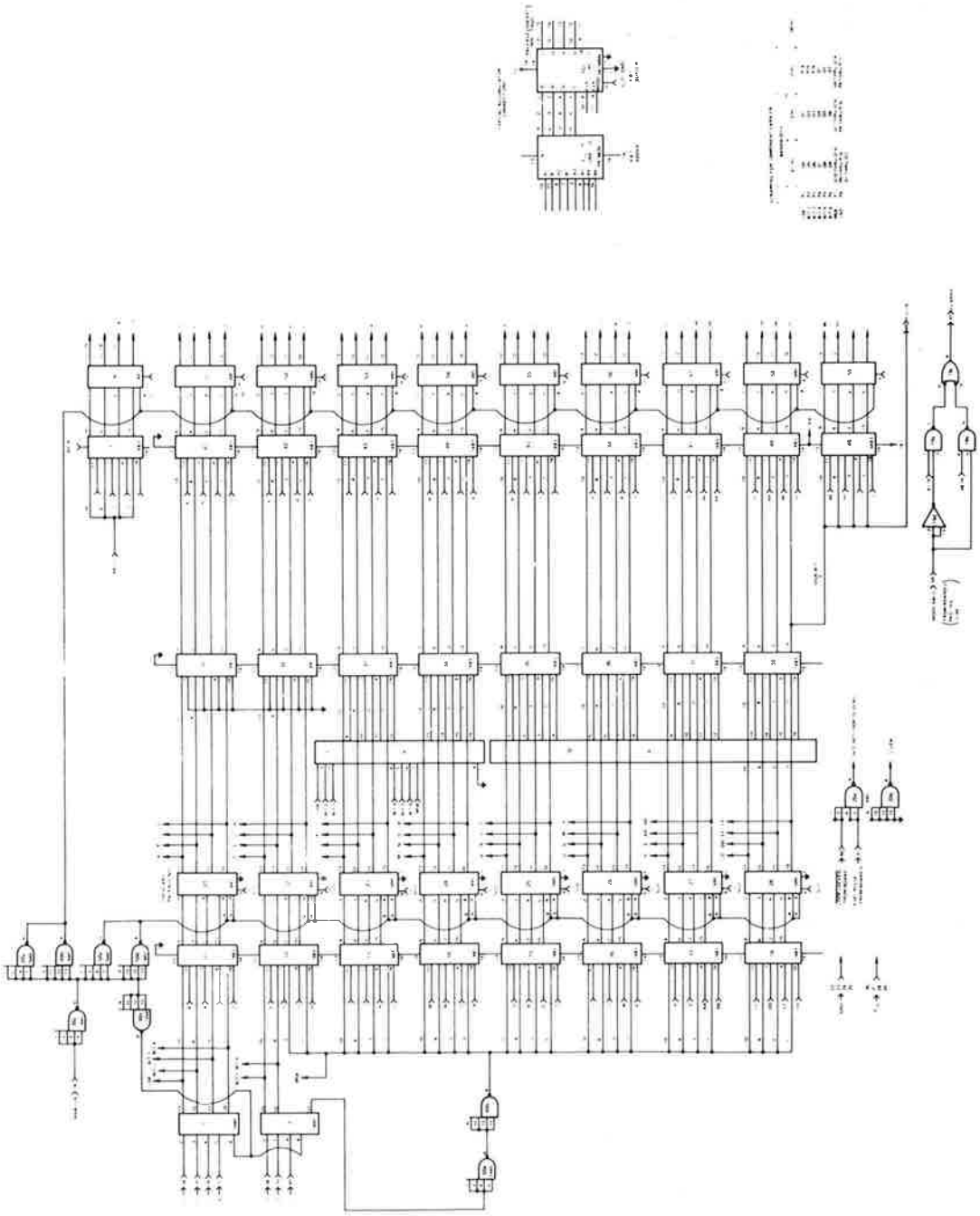


Figure 3-3b. ATS-6 Ranging Modem Digital Loop - Board 3

VCO. It must have enough dynamic range, i.e., enough bits to handle the full expected doppler excursions. In this design, a 32 bit accumulator is required. Packages 11-18 are 4 bit adders and packages 21-28 are 4 bit buffers. The output of each buffer is fed back to the input of the adder and this combination accumulates in a digital fashion. The phase error word from the buffer register packages 1 and 2 is wired to the low order 7 bits of the first accumulator. The most significant bit (sign bit) from the buffer is extended to the remaining n-7 bits of the accumulator, consistent with twos complement arithmetic. The output of the accumulator is added to a scaled version of the buffer output in adders 31-38. The low order "n" bits of these adders are wired to zeros. The next seven bits are added to the buffer output and the remaining n-m-7 bits are added to the extended sign bit from the first accumulator. Carries are propagated between all segments of the adders. The output of adders 31 through 38 forms the loop frequency command word into the VCO. This is the equivalent of an analog VCO control voltage expressed in binary.

The digital accumulator and counter control logic in combination with the variable counter act as the loop VCO. The frequency command word, the output of adders 31-38, is applied the input of the VCO accumulator packages 41-49. The output of this accumulator will be a positive or negative ramp, depending on whether the sign of the frequency command is positive or negative, respectively. Eventually, the accumulator will generate a carry or a borrow. The counter control logic accepts the carry output from package 49 or 48 depending on which clock tone is selected, and the sign of the frequency command word, with the sign and the carry, it generates, either an instruction to add one or subtract one according to the truth table shown.

The add one condition causes the variable counter to be advanced one count which causes it to enter the divide by 127 mode for one count. The subtract one conditions causes the variable counter to be retarded one count by entering the divide by 129 mode for one count. The rate at which ones are added or subtracted depends on three factors: The clock rate, frequency command word

value, and the digital accumulator length. Assume that the frequency command is one and the clock rate is 1 sample per second, if the digital accumulator has ten bits, it will take 1024 seconds between each carry from the accumulator. On the other hand, if the accumulator has five bits, it will only take 32 seconds between each carry. Thus, the equivalent gain for the VCO is $R_s \times 2^{-L}$, where L is the length of the accumulator in number of bits, since the length of the loop filter is not equal to the length of the VCO accumulator. It's necessary to extend the sign bit out of the loop filter to the remaining accumulator bits. A detailed mathematical derivation of the equations describing digital loop behavior is given in Appendix A.

BOARD 2 - HIGH SPEED COUNTER (FIGURE 3-3)

Board 2 contains the high speed counter and the counter control logic, packages 2, 4, 6 and 8 are the high speed synchronous flops used in the counter. Packages 3, 5, 7 and 9 are the high speed gates used in the counter. The counter is straightforward synchronous design, except for the first stage which has the controlling feature of adding or subtracting a count. The output of the counter is either 156 kHz or 19 kHz, depending on which clock tone is being used. Reference for the counter is always 40 MHz and is either divided by 2 or 16 to obtain the appropriate division frequencies.

BOARD 2 - CODE REGENERATOR (FIGURE 3-4)

Also located on Board 2 is the code regenerator used in the correlator functions. If all of the ranging tones generated on Board 4 has been acquired correctly, such that each has the proper phase with respect to each other. It is simply required therefore, to combine all the tones in gating identical to that which generated the code initially. This is accomplished on Board 2. Four bit adders 33-42 perform the majority logic functions which generates the code according to the procedures described in paragraph 2.1. All the gating represented by packages 18, 19, 20, 21, 22

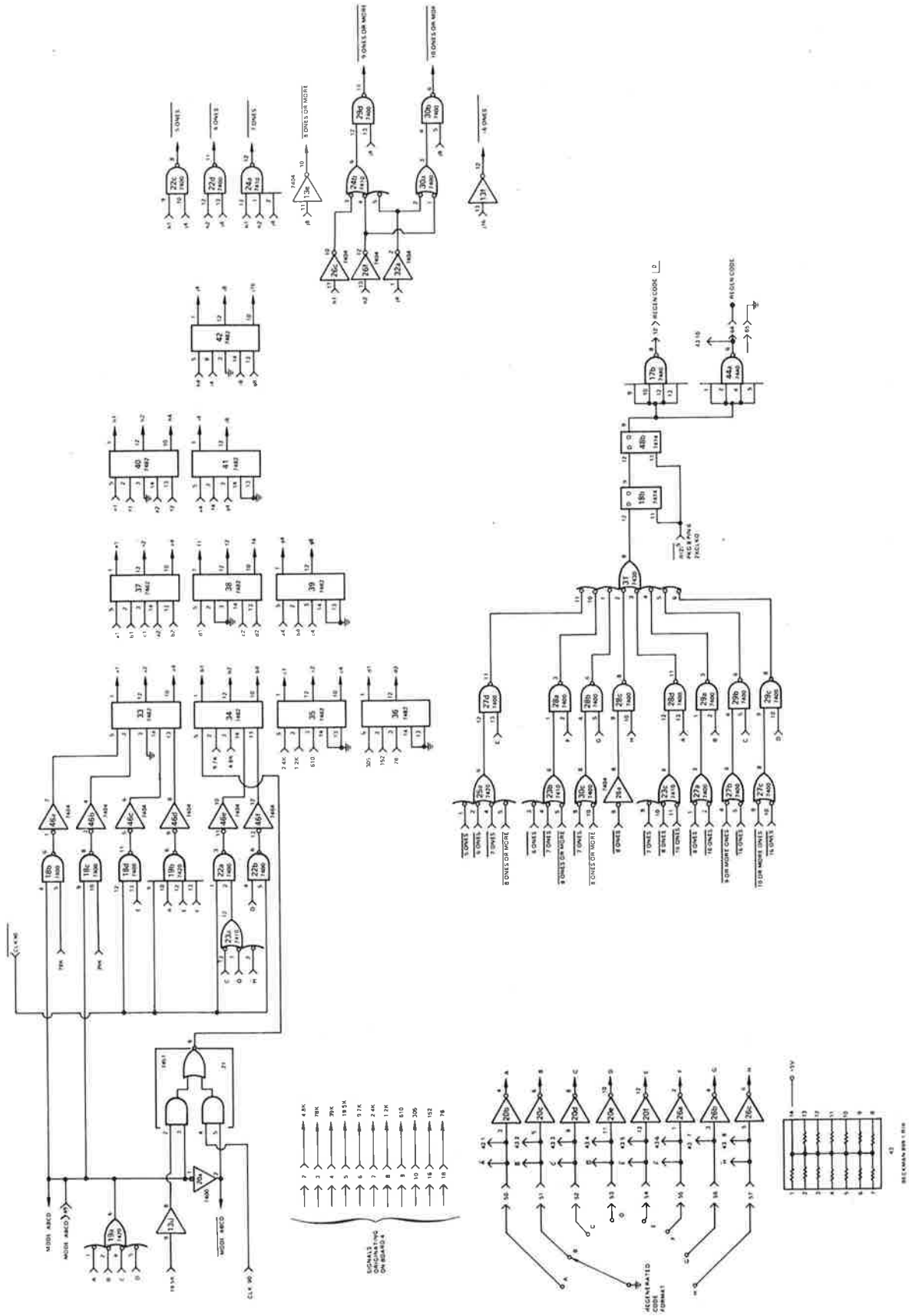


Figure 3-4. ATS-6 Ranging Modem Code Regenerator - Board 2

and 46 simply determine which clock tone is selected, and gate through the proper clock plus the two additional ranging tones required for the higher clock, all with the correct phase. According to the procedure described in Section 1.1, Code Properties, the code is generated by outputing a one, when the majority of the tones are one, hence gates 22, 24, 29 and 40 detect the presence of the necessary quantity of ones for each of the eight codes selectable.

Because each of the eight codes requires a different quantity of ones, gates 27d, 28 and 29 a, b and c are enabled by the regenerated code format switch, i.e., for code format A which is a 156 kHz clock tone weighted twice, with 11 additional ranging tones for total of 13 components, the majority logic would output a one if 7 or more components were high, therefore, gate 23c ORs together 7 ones or 8 ones or 16 ones, since the presence of any one of these would require a one output. In similar fashion, code format E is a 19 kHz clock tone weighted once, with eight additional ranging components for a total of nine component code, hence a majority of five or more ones would require a one output, gate 25a ORs together 5 ones or 6 ones or 7 ones or 8 ones. The possibility of having all components high, i.e., having 9 ones, is covered by the fact that 8 ones could also be high in this case. This code format is gated through OR gate 31 and then to flop 10b which removes glitches in the regenerated code.

3.3 PROGRAM CONTROL AND CORRELATION TONES GENERATOR BOARD 4 (FIGURES 3-5 AND 3-6)

Board 4 contains the program control which provides proper sequencing of events throughout the model. Packages 13a and 41-46 represents a 12 stage shift register, each shift causes different events during the acquisition process. Initially, all stages reset until the loop has locked, which is indicated by the input to package 38 going high. This forces flop 13a to be set to one, and that one is progressively shifted down the chain by a shift pulse generated by the integration cycles counter.

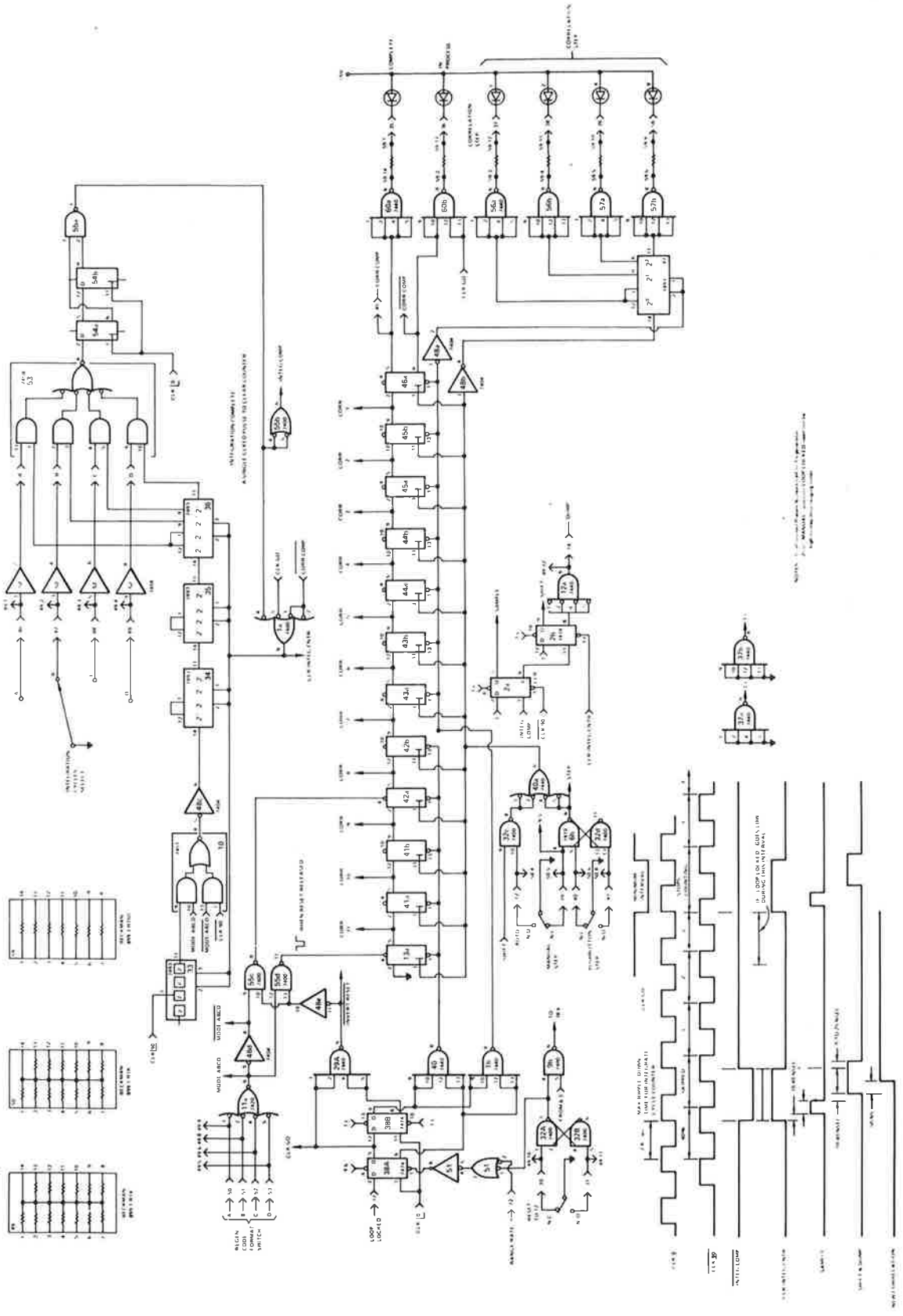


Figure 3-5. ATS-6 Ranging Modem Program Control - Board 4

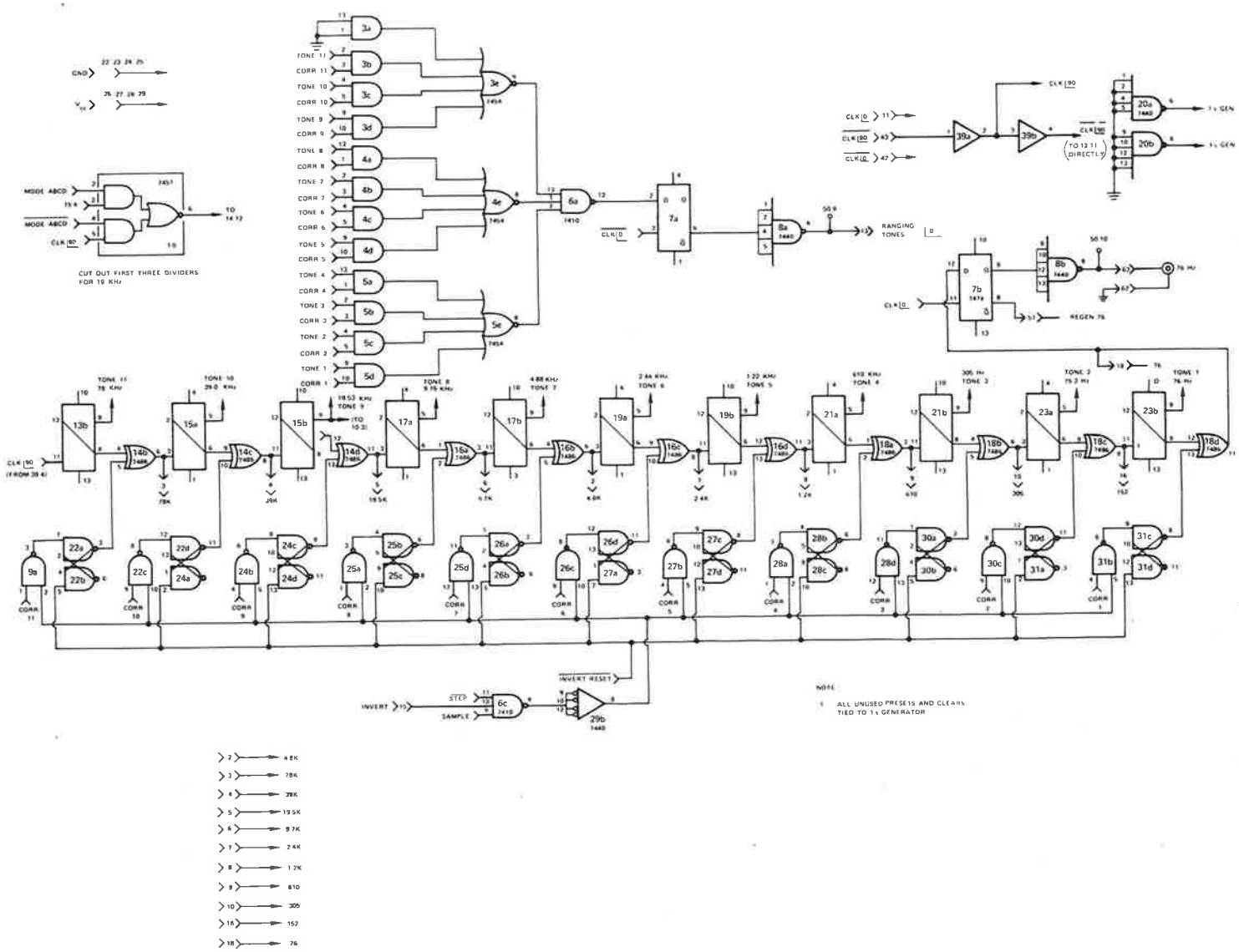


Figure 3-6. ATS-6 Ranging Modem Correlation Tones Generator - Board 4

At each shift a lower range tone correlation is made with the incoming code. These tones are generated in packages 13, 15, 17, 19, 21, 23 and are successively switched into sub-frequency correlator. Integration is then performed over the selected number of integration cycles, counted by packages 34, 35 and 36. A sample of pulse to interrogate the integration comparator then causes a dump pulse to discharge the integrator, causing a shift right in the program control which finally directs the next lower range tone to repeat the process. After the last range tone is correlated, a final shift right causes the complete lamp to illuminate. The particular correlation being performed is indicated by front panel lamps in a binary sequence.

3.4 RANGE MEASUREMENT, DISPLAY, AND ENCODER BOARD 5 (FIGURES 3-7 AND 3-8)

The lowest frequency ranging tone (76 Hz) from both the local code generator and the processor are fed through edge pulse generators, packages 7-9, which generate a START and STOP pulse 25 nanoseconds wide, at the leading edge of each. The time between START and STOP represents the range interval measurement which is gated out at a selectable rate through packages 5 and 6. A COUNT pulse is generated using START and STOP pulses and measured with both a high and low resolution time interval counter. The low resolution counter, packages 12-17, counting a 10 MHz square-wave is displayed on the front panel digital readout. Packages 18-27 and 30-33 perform the sole function of suppressing leading zeros in the digital display. The high resolution counter, counting a 40 MHz square-wave, provide precision data output for recording.

The count interval is selected to be either 4 per second, once per 2 seconds, or once per 4 seconds or a single count upon acquisition. At the once per 2 second or once per 4 second rate, the processor is forced to reacquire all ranging tones. At the 4 counts per second rate, reacquisition is not required provided the loop never loses lock. At the single count position, one range measurement is made upon acquisition of the tones and it is not repeated until reacquisition is required by losing lock.

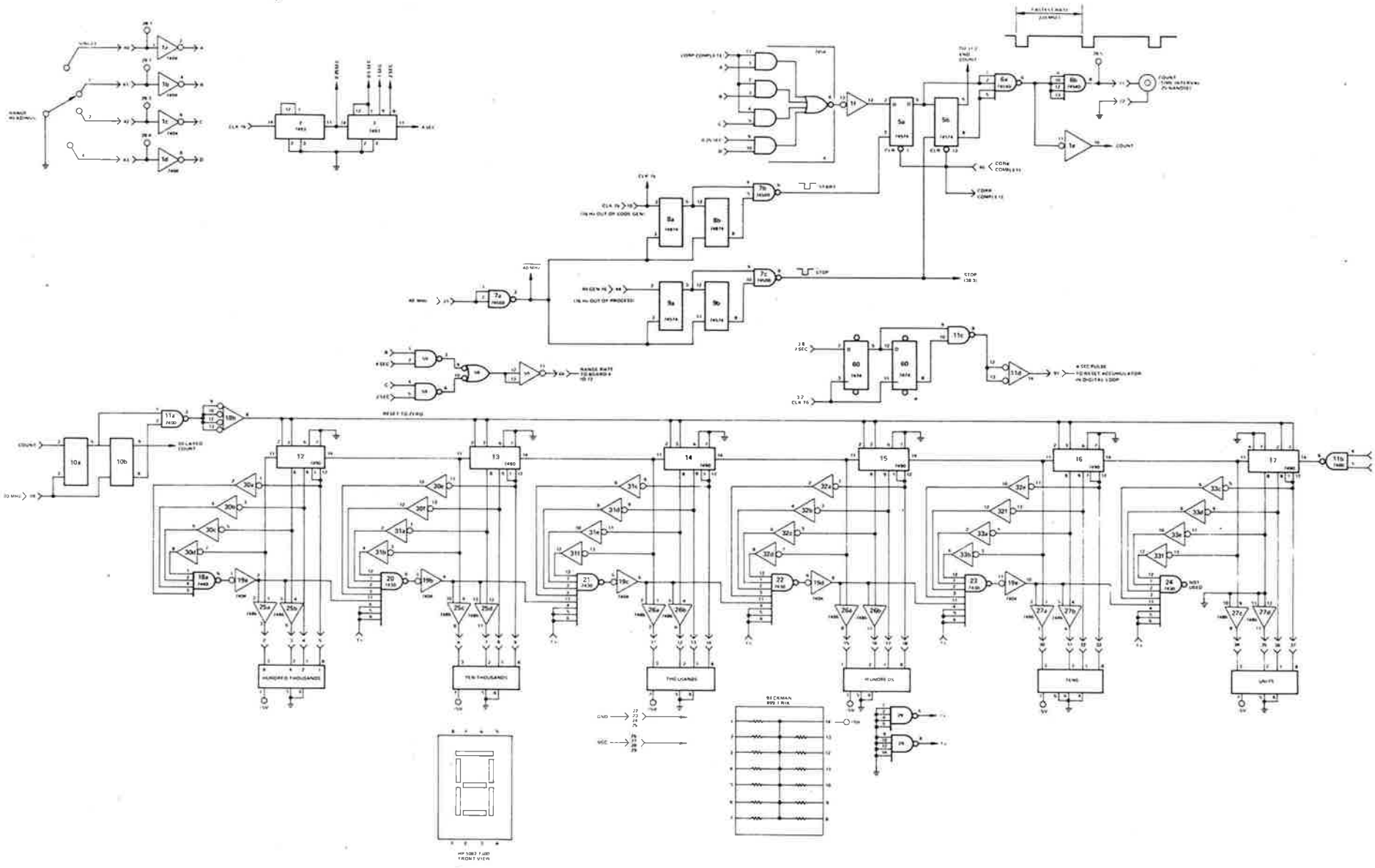


Figure 3-7. ATS-6 Ranging Modem Range Measurement and Display - Board 5

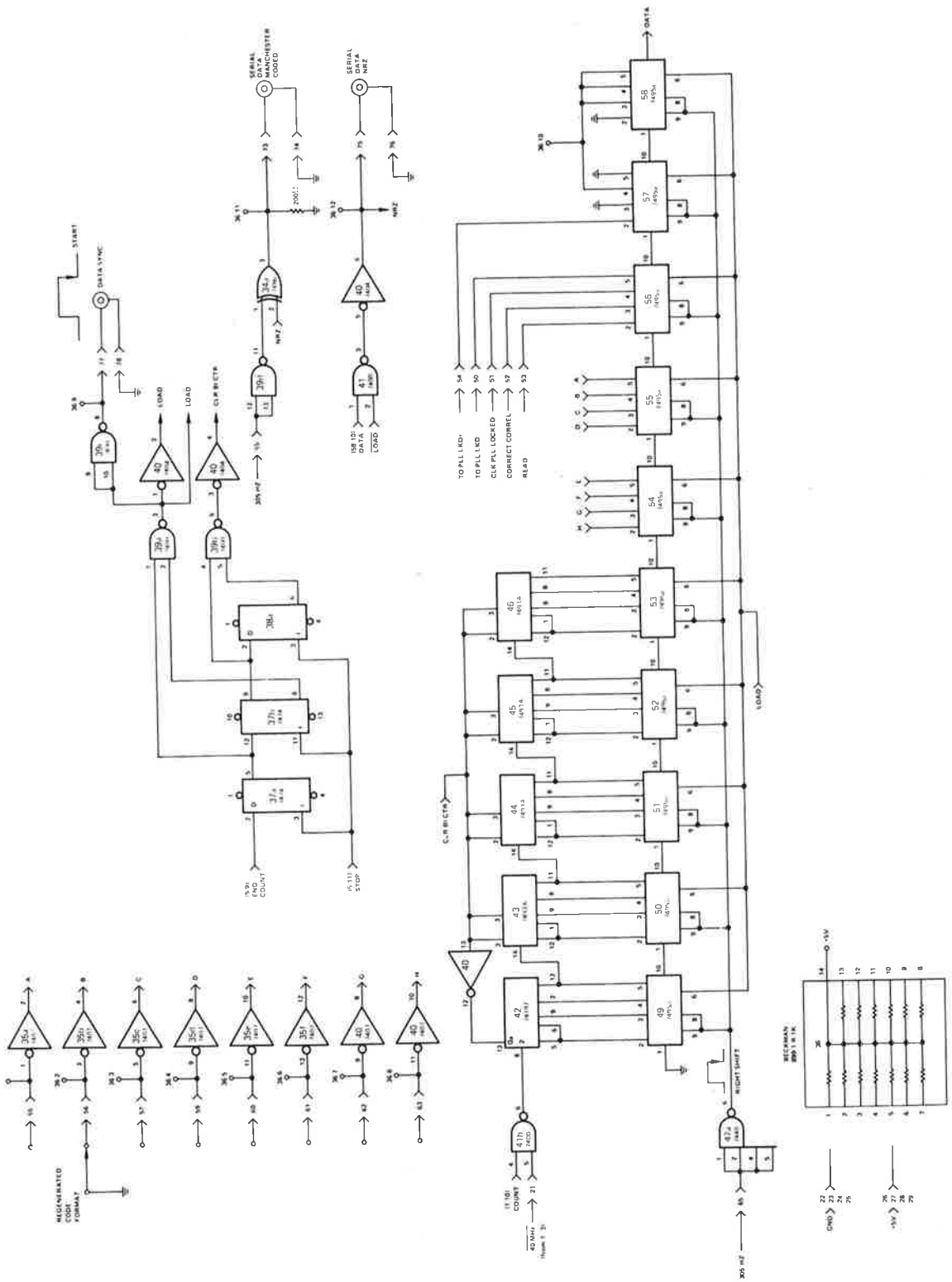


Figure 3-8. ATS-6 Ranging Modem Output Data Encoder - Board 5

3.5 CODE GENERATOR BOARD 6 (FIGURES 3-9 and 3-10)

Board 6 contains the code generator and control circuits. 5 MHz derived from either an internal or external reference is divided down to 76 Hz in divider chain 13-16 which generates all of the ranging tones. Tones 19.5 kHz through 76 Hz are fed directly to the logic circuits packages 36-45. The other ranging tones 39 kHz, 78 kHz and 156 kHz are gated through the appropriate selection of code format, therefore, inputs to adders 36 and 37 are either ranging tones or zeros. The code format selector enables one of the signals A through H in packages 19 and 20, which are used to control the gating in packages 18, 19, 21, 22 and 23 for selecting the proper weighting of the code format as follows: 2, 4, 6 or 8 times in the case of 156 kHz clock or once, 3, 5 or 7 times as in the case of the 19 kHz clock. The output of the majority logic packages 36-45 determines the number of ones in the total code components summed together. Then, for any particular code format selected, it is simply required to OR together the possible combinations of ones. This accomplished in packages 28a, 23b and 25. Packages 30a provides a means of inverting the code to account for an odd number of inversions between the modulator and demodulator. Packages 24b removes glitches and the local code is available at the front panel BNC connector and werever required in the processor.

3.6 RF MODULATOR AND REFERENCE FREQUENCY GENERATORS BOARD 7 (FIGURES 3-11 and 3-12)

Board 7 contains the RF modulators and the reference frequency generators. A reference phase lock loop, consisting of an exclusive OR mixer package 3a, followed by a loop filter, package 4, driving a vectron VCXO of 80 MHz can be phase locked to either an internal or external 5 MHz. This loop then generates all of the subsequent reference frequencies used throughout the ranging modem. The 80 MHz is divided in half by flop 6a to generate a symetrical 40 MHz squarewave which is then synchronously divided in package 7 to obtain 40,20,10 and 5 MHz. To indicate that the 5 MHz loop is

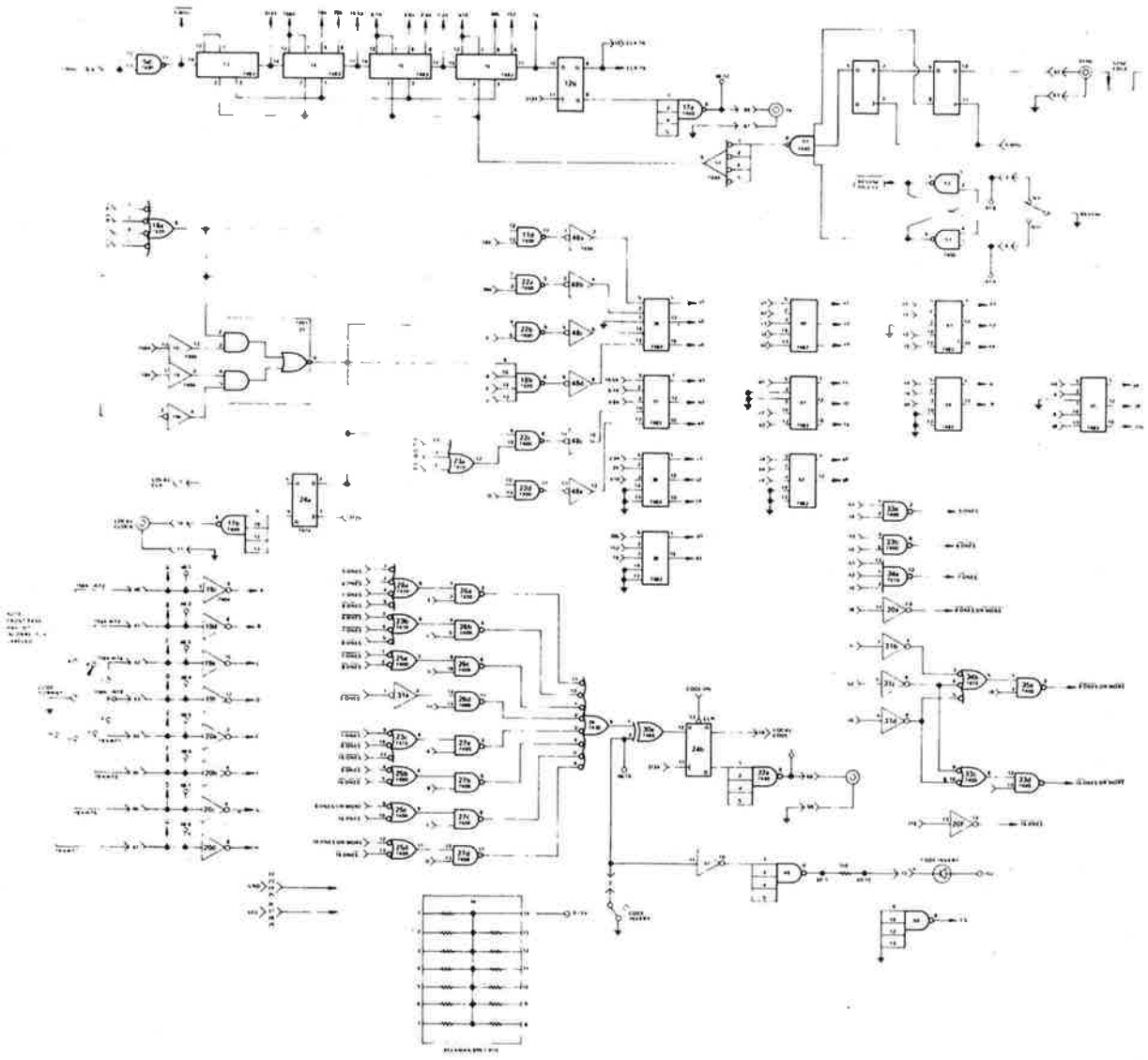


Figure 3-9. ATS-6 Ranging Modem Range Code Generator - Board 6

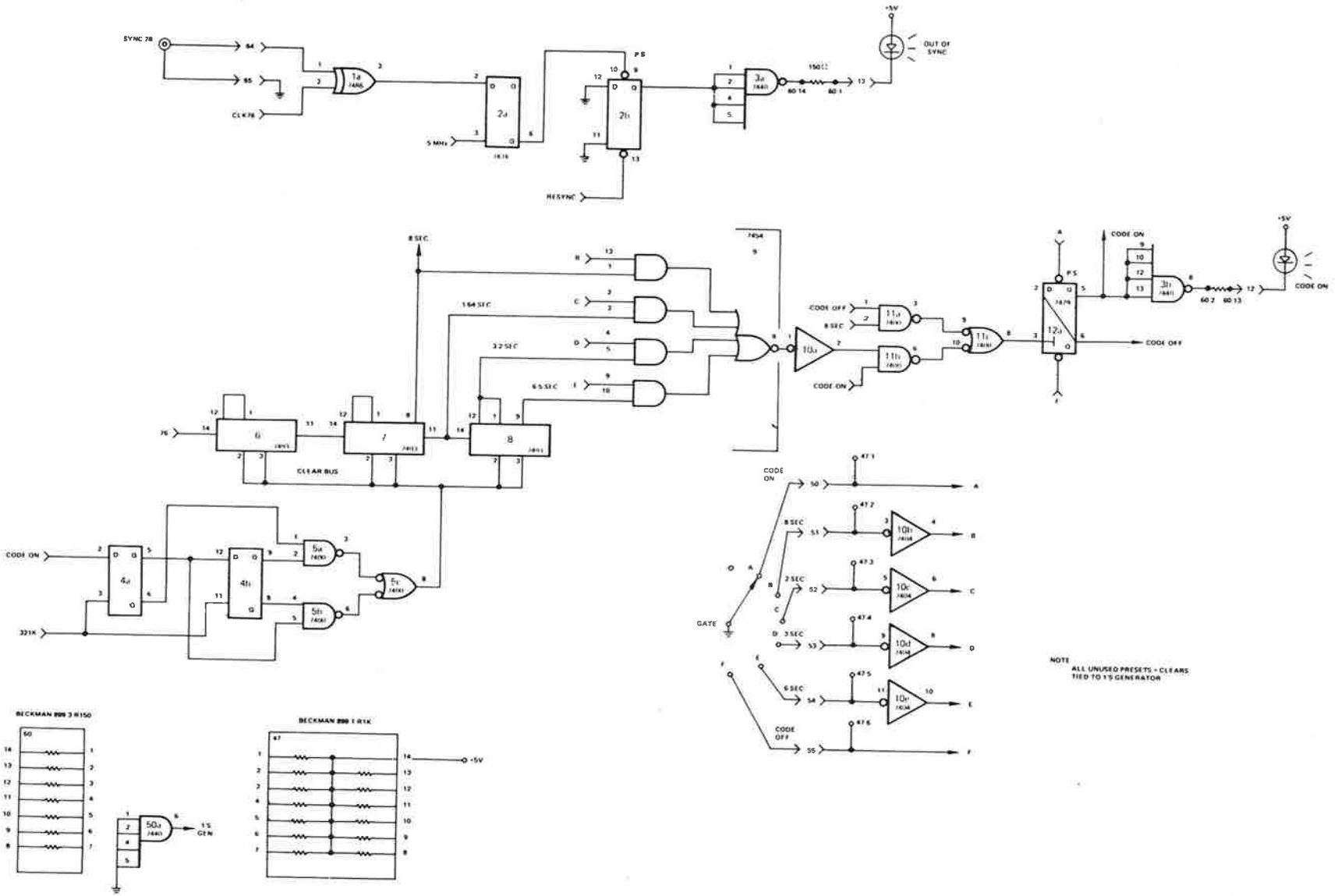


Figure 3-10. ATS-6 Ranging Modem Code Generator Controls - Board 6

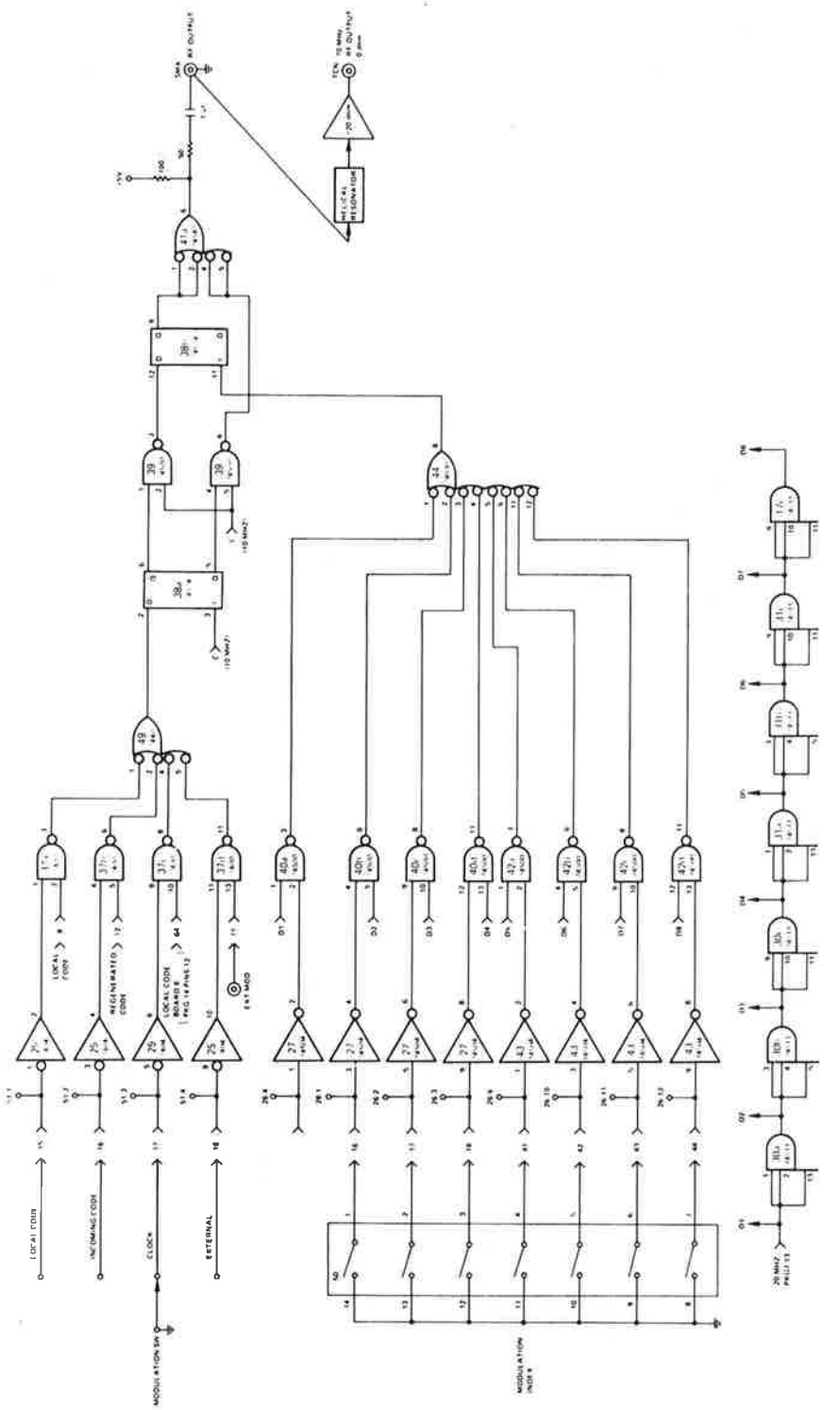


Figure 3-11. ATS-6 Ranging Modem RF Modulator - Board 7

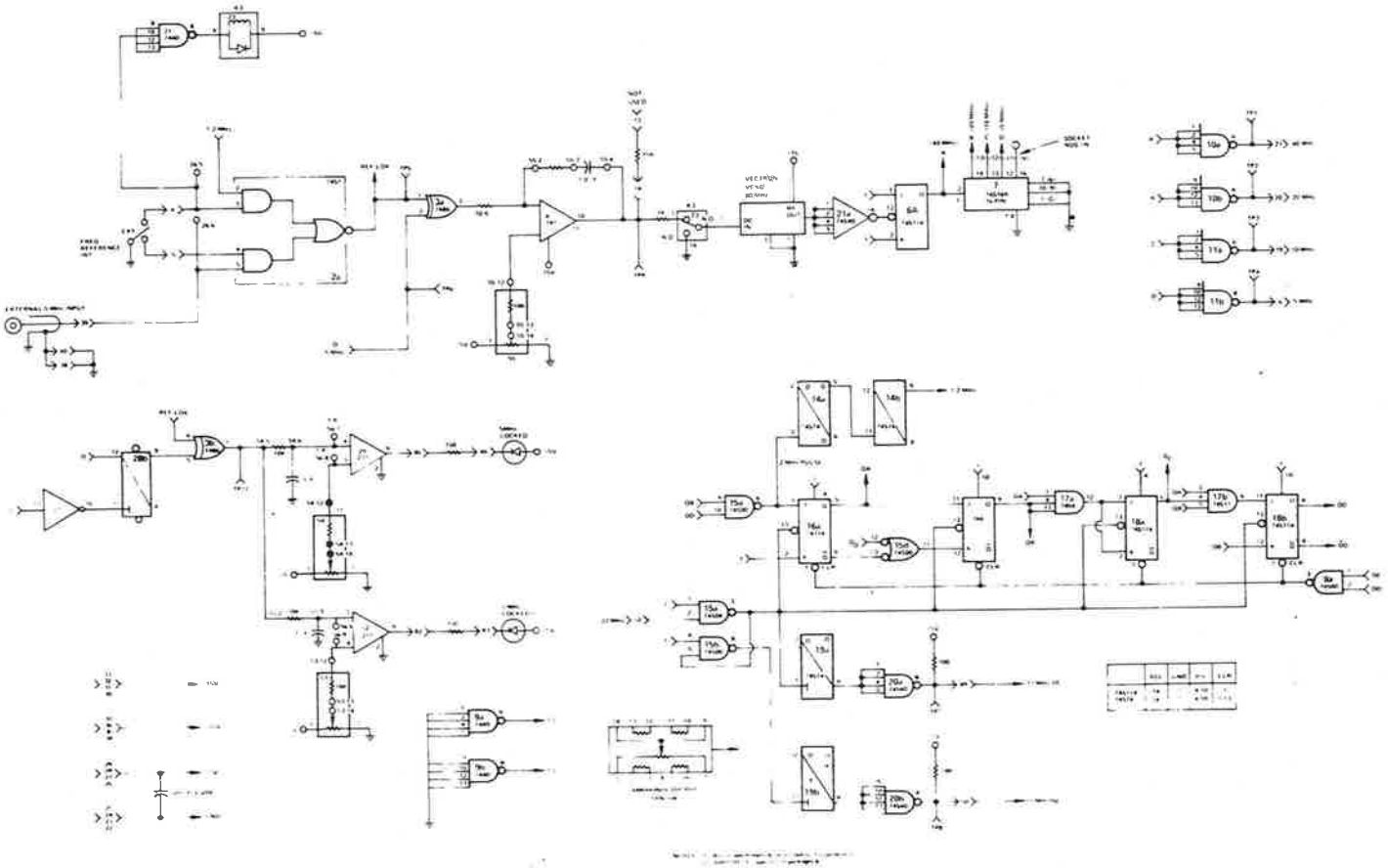


Figure 3-12. ATS-6 Ranging Modem Reference Frequencies - Board 7

locked to either internal or external references. A coherent detector is provided, beginning with the exclusive OR mixer in package 3b, followed by threshold detector, package 29 for lock-up in negative phase and another threshold detector, package 52, for lock-up in a position phase. Because the 5 MHz loop is able to lock-up in either phase, both indicators are required. A 22 MHz reference signal also comes into this board; is divided in half and the phase changed to obtain 11 MHz at 0° phase and 11 MHz at 90° for use in the RF card.

Packages 15, 16, 17 and 18 are part of a divide by 11 circuit which is no longer used, but included in the drawings.

The RF modulator function is performed by packages 38 and 39. Packages 25, 37 and 49 select which of four signals will be modulated onto the RF carrier. They are: the local code, incoming code, the clock, or an external input. The modulation index is selected by the switches in package 50. The 20 MHz modulating frequency is delayed through gates, packages 30 and 31, and gated into a matrix which determines the final modulation index, in packages 27, 40, 42, 43 and 44.

The modulation is performed on a 10 MHz carrier which is the output of buffer package 41. It is then capacitively coupled into a sharp skirted filter called a helical resonator, which picks out the 7th harmonic. This is then amplified up to 0 dBm, and appears at a front panel output BNC.

3.7 70 MHz LOOP BOARDS 8 AND 9 (FIGURES 3-13 AND 3-14)

The 70 MHz IF frequency from the satellite down-converter is accepted by a front panel BNC connector and fed to Board 9, which contains all the 70 MHz circuitry.

The input hybrid H1 provides a convenient method of injecting noise for testing the system through the 70 MHz noise input jack. Input 70 MHz is mixed in Mixer M1 with 81 MHz VCO frequency to produce at 11 MHx IF which is split two ways; one to the video demodulator and the other way through a crystal filter F1 for the

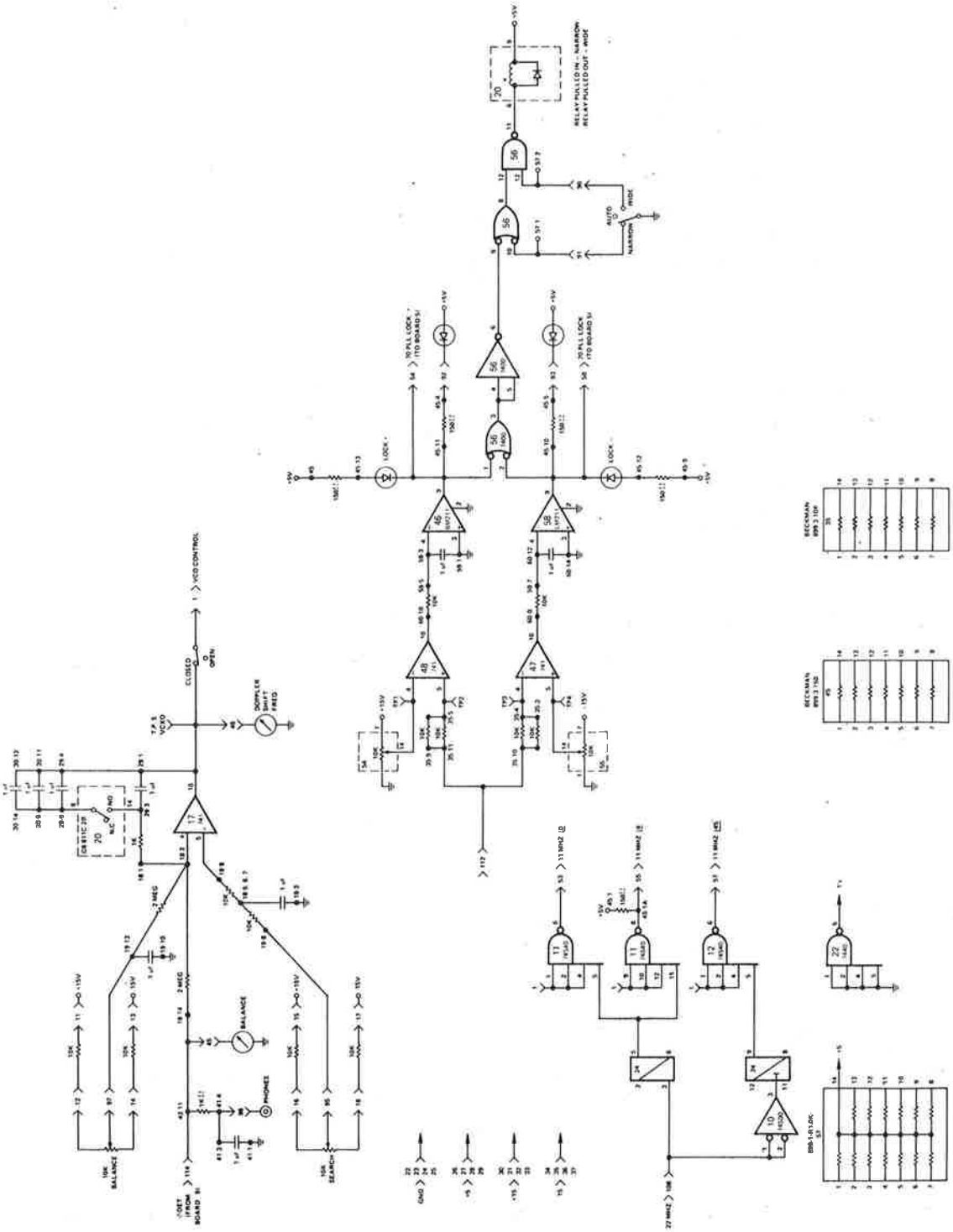


Figure 3-13. ATS-6 Ranging Modem RF Loop Filter - Board 8

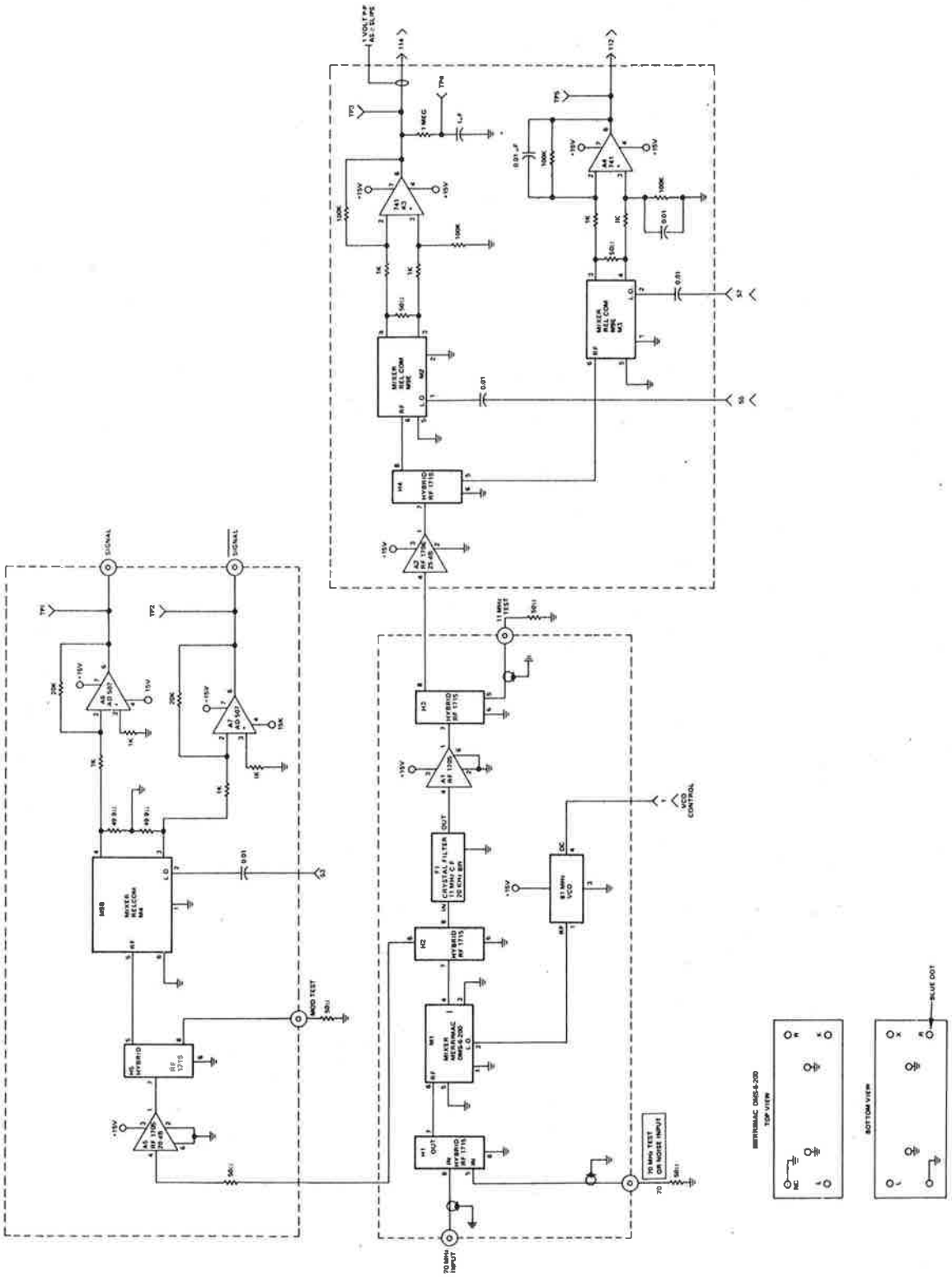


Figure 3-14. ATS-6 Ranging Modem RF Phase Lock Loop - Board 9

locking circuits. Amplifiers A1 and A2 amplify the 11 MHz IF. Hybrid H4 splits the IF frequency to three phase detectors. The first one beginning with Mixer M2 is a conventional double balanced mixer followed by a differential amplifier and loop filter for narrowband loop locking. The second phase detector beginning with mixer M3 is also a conventional doubled balanced mixer followed by loop filter, this detects a coherent signal for driving the lock indicator. A third phase detector located on Board 8 has a wide bandwidth for rapid acquisition and is implemented using a combination of digital and analog components. Board 9 also contains the video demodulator beginning with mixer M4. The differential signal out of this mixer is amplified by a special wideband operational amplifier, analog devices type 507. These amplifiers provide both the high gain wide bandwidth required by the video signal and the high capacitance drive required by the cable carrying the video signal to Board 1.

Board 8 contains the wideband phase detector, packages 10, 23, 24.

Operation is as follows:

The 11 MHz IF frequency out of the first mixer is threshold detected and squared up in high speed comparator, package 21 (Fairchild uA760) then drives flop 23b. 11 MHz reference frequency drives flop 23a. The setting of these two flops and feedback gate 10d generate a signal proportional to the phase difference at the input to the differential amplifier, package 34. Here either the wideband or narrowband phase detector is selected by read relay package 20 and supplied to the loop filter, package 17. The loop may be opened at the output of package 7 for testing purposes. Packages 46, 47, 48, 59 provide the circuitry for driving the loop lock indicators.

Additional gating provides automatic transferal from the wideband to the narrowband phase detector. When automatic is selected, the wideband phase detector operates until the loop has locked up; at that time there is automatic switching to the narrowband phase detector via read relay 20.

Also located on Board 8 are the flops that divide the internal 22 MHz reference oscillator down to 11 MHz to provide the reference IF frequency for the RF loop. Packages 11 and 12 are buffers to provide the mixer drive levels required. In addition, Board 8 contains the plus and minus 6 volt power supplies required by the search and balance potentiometers and the high speed comparator.

3.8 MODEM MOTHER BOARD INTERCONNECTIONS (SEE FIGURE 3-15)

Each of the functional boards 1 through 9 plug in to a mother board which makes all of the interconnections between each of the above boards.

Figure 3-15 shows these interconnections.

3.9 FRONT PANEL CONTROLS

Beginning with the left hand side controls for the code generator; CODE FORMAT - This eight position rotary switch selects which ranging code is to be phased modulated for the outgoing 70 MHz carrier to the satellite up-converter. Four of the codes have a clock tone of 156 kHz which may be weighted 1, 3, 5, or 7 times and another four have a clock tone of 19 kHz which may be weighted 2, 4, 6, or 8 times.

GATE - This five position rotary switch selects the interval during which code is applied to the 70 MHz carrier. The code may be on continuously or on for 1, 2, or 4 second invervals and off for one second intervals, or switches the code off all together leaving an unmodulated 70 MHz carrier.

MODULATION - This four position rotary switch selects the modulation source for the 70 MHz carrier. The choices are:

1) internal code for one way ranging where the code generated locally is used.

2) incoming code for round trip ranging where the regenerated code in the demodulator section is used to modulate the 70 MHz carrier essentially taking the incoming code and turning it around and sending it right back out.

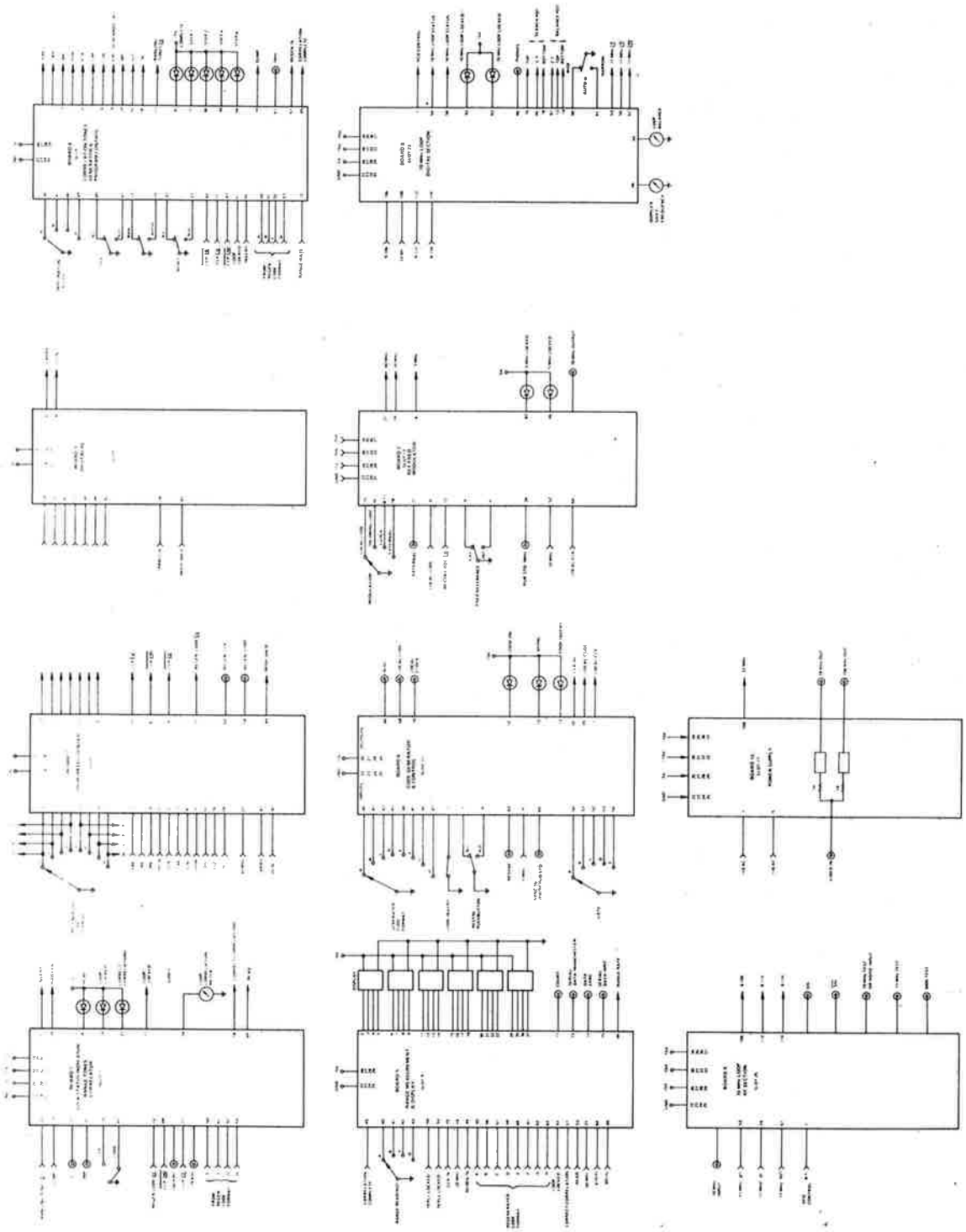


Figure 3-15. ATS-6 Ranging Modem Mother Board Interconnections

3) external modulation at the external BNC connector in the outgoing box.

4) clock generated in the code generator locally, either 156 kHz or 19 kHz depending on which code format is selected.

The lighting emitting diodes (LED) located on the code generator left hand side from left to right are as follows: 5 MHz LOOP LOCKED PLUS AND MINUS indicate which phase of the external 5 MHz reference frequency coming from the Rubidium standard has been selected as the lock point for the internal 80 MHz VCO. It is not important which of these lights is luminated, just as long as either one is illuminated when the external reference frequency is selected.

CODE ON illuminates during the true gate interval.

76 Hz ASYNC. illuminates if the interval 76 Hz is out of phase with a reference 76 Hz, coming in through BNC labeled SYNCH 76 in the outgoing reference frequency box.

INVERT is illuminated when the code is inverted when compared with the regenerated code from the domodulator. This switch allows for an odd number of inversions in transponding the ranging signals through ATS-F satellite.

The SYNC RESET push button engages the local code generator at the leading edge of the square wave applied to the BNC connector labeled RESYNC in the external reference frequencies box.

Switch labeled WETYO is for future use.

FREQUENCY REFERENCE switch selected either an external 5 MHz or the Internal stability of a 80 MHz VCO.

OUTGOING CONNECTORS

CODE - locally generated code is available at this connector.

CLOCK - the clock component of the locally generated code is available at this connector.

76 Hz - the 76 Hz component of the locally generated code is available at this connector.

70 MHz - this is the carrier frequency to the satellite up-converter.

FREQUENCY REFERENCE

5 MHz - this is the 5 MHz coming in from the Rubidium standard.

SYNC 76 - this connector accepts a 76 Hz squared wave for comparison against the local generated 76 component of the code and will illuminate the ASYC light if these are out of phase by more than 200 nanoseconds.

RESYNC - this connector accepts a waveform which can be used to synch the local internal regenerated code.

MODULATION - this connector accepts external modulation to be phase modulated onto the 70 MHz carrier.

The following controls apply to the demodulator portion of the ATS-F ranging modem.

CODE FORMAT - this eight position rotary switch selects the format of the incoming code. It is possible to be receiving and transmitting different code formats if modems on each end of the link are operating in one direction only.

RANGE READINGS -

Position one selects a single range measurement upon acquisition and correlation of the incoming code, which remains displayed indefinitely on the front panel and is clocked out only once in the data output connectors.

In position 2, the processor will track the clock of the incoming clock and reacquire the ranging tones once every 2 seconds. At the completion of this acquisition, a new range measurement will be made and displayed on the front panel indicator and clocked out at the data outputs.

In position 3, the processor will repeat the above at a once per 2 second interval.

In position 4, the processor will remain locked to the incoming clock, acquire the ranging tones once, and then proceed to make four range measurements per second, displayed on the front panel and clocked out at the data outputs. It will continue to do this as long as the modulator remains locked.

INTEGRATION CYCLES - this four position rotary switch selectes the number of code word lengths that integration of each ranging ton occurs over.

Under the box labeled CORRELATIONS, the following functions apply:

CLOCK - illuminates when the clock tracking loop acquires.

COMPLETE - illuminates when all range tone correlations are completed.

CORRECT - illuminates when all of the range tone correlations have been done correctly.

READ - this lamp is for future use.

LAMPS 1, 2, 4 and 8 - indicate which of the range tones are presently being correlated.

AUTO - this switch selects either AUTOMATIC or MANUAL sequencing through the range tone correlations.

STEP - this push button sequences through range tone correlations in the MANUAL position.

RESET - this push button resets range tone correlations back to zero in either the MANUAL or AUTOMATIC position.

CODE/CLOCK - this switch selects the special correlations mode at the completion of all range tone correlations. See paragraph 2.3 for further explanations.

The following functions apply for the box entitled 70 MHz.

LOOP LOCK PLUS AND MINUS - one of these lamps will illuminate to indicate which phase of the 70 MHz incoming carrier the loop has locked to.

WIDEBAND/AUTO/NARROWBAND - this three position switch selects the RF loop phase detector during the 70 MHz acquisition process. In the wideband position, rapid acquisition is possible regardless of the doppler shift frequency. In the narrowband position, searching with the potentiometer is required for lock. In the automatic

position, the wideband phase detector operates until lock is found, then the loop automatically transfers to the narrowband phase detector.

INCOMING CONNECTORS

CODE - The reconstructed code based on the incoming signal is available at this connector. It will always be the correct code but it will only have the correct phasing when the loop is locked, and correlations made correctly.

CLOCK - This is the clock tone of whichever code is selected by the code format switch.

76 Hz - This is the 76 Hz component of the reconstructed code.

70 MHz - This connector accepts the 70 MHz IF frequency from the satellite down-converter.

DATA OUTPUT CONNECTORS

NRZ - Range data is available at this connector, coded in non-return to zero format at a rate selected by the range readings switch.

MANCHESTER - Same as above except Manchester encoded.

SYNCH - A pulse in phase with the start of data available at this connector.

COUNT - This is a pulse whose width corresponds to the time interval between the incoming 76 Hz component and the locally generated 76 component.

PANEL METERS

76 Hz Doppler Shift - This meter represents the doppler shift in kHz that the incoming 70 MHz frequency has experienced.

70 MHz Loop Balance - This meter should be set to zero with the WETYO potentiometer after the 70 MHz loop has locked. It indicates loop filter offset voltage. Optimum performance of the loop will occur when this voltage is near zero, since that allows equal excursions of noise spikes without amplifier saturating or clipping.

Clock Loop Correlation - This meter is a relative indication of the coherent phase detector output of the clock loop. It provides a visual indication of the performance of the clook loop. Jitter and cycle slipping are easily observable. Use the BALANCE potentiometer to adjust this meter for maximum positive deflection.

3.10 ALIGNMENT PROCEDURES

The modem should not require alignment, but a change in the operating input levels would require certain threshold points to be readjusted.

To perform an alignment, proceed as follows:

3.10.1 Alignment - RF Loop Board 8

STEP 1: Turn modem on, select code format A, in both the code generator and demodulator, connect 70 MHz carrier out to 70 MHz carrier in.

STEP 2: Connect a scope to the 11 MHz test output jack on Board 9. Connect the second channel of the scope to the test point 14 on Board 8. These are the 11 MHz RF frequency of the RF loop and the 11 MHz internal reference, respectively. The signals will be locked in phase when the loop is locked.

STEP 3: The potentiometers 54 and 55 on Board 8 adjust the threshold point that indicates lock of the 70 MHz loop on either the plus or minus phase. The loop will randomly select either plus or minus lock points.

STEP 4: While the loop is in lock, adjust the corresponding potentiometer to illuminate the front panel display.

3.10.2 Alignment Procedure/Board 7/Reference Frequencies

Board 7 contains the reference frequencies generators which can be locked to an internal or external frequence source as described in paragraph 8. The adjustments in the loop that locked

to the 5 MHz external signal are phase offset adjusted by potentiometer 55, and loop lock indicators plus and minus adjusted by potentiometers 53 and 54.

STEP 1: Connect scope to test point 1 and adjust potentiometer 55 from a symmetrical square-wave.

STEP 2: Connect the scope to test point 2 and adjust potentiometer 54 for the lock light to illuminate.

STEP 3: Repeat the above procedure for potentiometer 52 when the loop is locked to the opposite phase.

3.10.3 Alignment Procedure/Board 1/Video Correlators

Insure that the RF loop is locked and display the clock out of the code generator and the clock out of the code processor. Clock loop should also be locked.

STEP 1: With mode format A selected on both code generator and processor, adjust potentiometer 49 for maximum position deflection on the loop correlation meter.

STEP 2: Adjust potentiometer 52 for the loop locked light to come on.

STEP 3: Force the modem to reacquire the ranging tones until front panel display is reading 1.7 microseconds, then adjust potentiometer 34 for correlations correct lamp to illuminate.

STEP 4: Switch to code format F in both generator and processor.

STEP 5: Adjust potentiometer 50 for maximum positive deflection on the loop correlation meter. Potentiometer 59 is for future use.

4. LABORATORY TESTS

The ATS-6 Ranging Modem was tested in the laboratory under various conditions of input signal-to-noise ratio, clock tracking loop bandwidth and code structure. The system performance variables of primary interest are sub-frequency correlation error and phase jitter, which represents ranging accuracy.

5. TEST RESULTS AND RECOMMENDATIONS

A comprehensive testing program was performed for the ATS-6 ranging modem. We had an opportunity to test the modem both in the laboratory and under actual field operation conditions. Data on the performance of the modem has been collected during a series of flight experiments conducted from September, 1974 through April, 1975 operating through the ATS-6 satellite. Three identical ranging modems were built and installed: (1) on board an aircraft; (2) on a Coast Guard cutter; (3) at the ground station at Rosman, which will allow comparison of data collected to two mobile locations. Testing performed to date has given assurance that the unit performs reasonably well in the laboratory but field data is considered primary criteria. As data reduction progresses throughout the following year, the major design goals of correlation error and ranging accuracy will all be investigated further. The results of the test program will guide recommendations for design changes to improve the performance.

We have experimented with the ratio of clock tone power to ranging tone power since the loop fails to lock long before correlation errors are made. Different clock weightings at both 156 kHz and 19 kHz clock frequencies are provided.

Multipath effects have been investigated under actual field conditions. Because the existing laboratory simulator does not have the necessary bandwidth, the ATS-6 experiments have provided the first opportunity to test this approach to ranging under real-time multipath conditions.

6. SUMMARY AND CONCLUSIONS

The primary feature of the ATS-6 ranging modem is its ability to function with weak input signals in high noise environments. The modem was designed with a maximum of flexibility to allow various combinations of experiments to be performed. Each modem is completely self-contained having an internal code generator plus internal 70 MHz modulator and demodulator, along with a built in front panel display of range measurement, allows ranging modem to be both versatile and independent for easy implementation in an AEROSAT ranging experiment. Preliminary test data demonstrates satisfactory performance at carrier-to-noise density ratios as low as 39 dB-Hz, in laboratory conducted noise measurement tests. This modem demonstrates the successful implementation of a completely digital phase lock loop which makes possible extremely narrow loop bandwidths, exactly duplicated in each modem. The bandwidths may be changed easily and the performance duplicated at any location repeatedly.

7. MODEM SPECIFICATIONS

7.1 PROCESSOR INPUTS

The processor will function correctly with an input signal level of -18 ±2 dBm, with noise of up to 0 dBm. In the 500 kHz input bandwidth, this is equivalent to a carrier-to-noise density ratio of 39 dB-Hz. At input signals lower than this, the modem will fail to lock. At input signals greater than this, the RF amplifiers will begin to saturate.

7.2 IMPEDANCE

The input impedance to the processor is 50 ohms.

7.3 BANDWIDTH

The processor bandwidth is 1/2 MHz centered about 70 MHz. This is satisfactory for the wide bandwidth code format, with its clock tone frequency at 156 kHz.

7.4 POWER

The model accepts standard 115 volt ac 60 to 400 cycle power.

7.5 OUTPUTS

All of the following outputs are TTL levels.

76 Hz - lowest component of the code, both from the generator and processor. This square-wave is quantized by the digital loop only, not by the internal count frequency generator, and therefore, should be used in making all jitter measurements.

7.6 70 MHz PHASE LOCK LOOP

The RF loop in the modem was designed to have a loop natural frequency of 7 Hz, and damping factor of 1/2. The loop will track a doppler shift of ±4 kHz from 70 MHz, and will pull in with a doppler shift of ±2.5 kHz from 70 MHz.

7.7 DIGITAL PHASE LOCK LOOP

The digital loop is designed to have a bandwidth of 1 cycle and a damping factor of 1/2.