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ANALOG RANGING MODEM CODE PROCESSOR AND GENERATOR

P.G. Mauro

MAY 1974

FINAL REPORT

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16. Abstract

This report details technical development efforts to implement an analog ranging modem using recently developed linear integrated circuits where possible. The breadboard hardware is capable of acquiring frequency and phase of a weak signal in a high noise environment, i.e., a C/No ratio of 37 dB-Hz, as verified in laboratory noise tests.

The report includes a description of the system and of the hardware implementation. The ranging technique implemented and tested here has direct application to the AEROSAT system. It represents one possible approach to sidetone ranging. The test setup and test results are given along with a summary, recommendations and conclusions. Schematics of the circuitry, test data and analyses are included.

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PREFACE

The work described in this report was performed in the context of an overall program at the Transportation Systems Center supporting system design and development, avionics design, and test evaluation programs that influence the overall design of an aeronautical satellite system for an en-route-over-ocean-traffic, advanced air traffic control system. This program is sponsored by the Department of Transportation through the Federal Aviation Administration, Systems Research and Development Service. The program supports government activities designed to promote Air Traffic Safety through improving the integrity of the Air Traffic Control System.

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1. ANALOG RANGING MODEM PRINCIPLES

The analog ranging modem was designed to experimentally verify a ranging technique originally analyzed by J.J. Stiffler[1], and later extensively investigated by Thompson, Ramo and Woolridge (TRW) on a National Aeronautics and Space Administration - Electronic Research Center contract[2]. Stiffler showed that in a tone ranging system, the optimum rate of information transfer would be achieved if a 2:1 tone ratio was used. TRW pointed out that this led to a particularly simple implementation scheme, referred to as BINOR for Binary Optimum Ranging. In essence, it is a simple way of generating and detecting signals used for sidetone ranging.

1.1 CODE PROPERTIES

The code sequence chosen is generated from a series of coherent square waves which are harmonically related by multiples of two. These are referred to as the "components" of the code, or "ranging tones." The binary code is generated from the square waves by the following rule. During each bit time of the highest frequency square wave or "top tone," the number of square waves in binary state "zero" are subtracted from the number of square waves in binary state "one." If the result of this subtraction is negative, the code is put in the binary state "zero," and if the result is positive, the code is put in the binary state "one." The total number of square waves can be kept odd to avoid a "zero" or an indeterminate subtraction result. This code generating process has a bit rate equal to twice the highest square wave frequency, and a code period equal to the period of the lowest frequency. The code displays mirror symmetry about the center of its period.

Of great importance is that the code contains elements of each of the input frequencies and, in the most straightforward system, each component represents $\frac{1}{n}$ of the signal power, where n is the number of components. This makes it possible to correlate the code against any of its components. The limiting action, which was needed to produce a binary output, introduces other elements into the code so that correlation with the original components is reduced

somewhat. The reduction, however, is only about 2 dB, which for this design is not considered significant.

The code used in the model implementation encompasses thirteen components (n = 13) ranging from 312.5 kHz to 76.5 Hz. Thus, the bit rate is 625 kilo bits/sec and the ambiguity range is in excess of 2100 nmi. The 312.5 KHz tone is derived form a stable 5 MHz source by digital division.

1.2 SYSTEM PRINCIPLES

For any application, a system built to utilize the code as described above will embody the principles of operation discussed briefly here. The processor will acquire the transmitted code and output its lowest frequency component. This square wave is then compared in phase with the locally generated square wave, and the relative phase is known. A time interval meter providing the necessary resolution is a convenient means of measuring the relative phase. This phase represents both the absolute time difference between the clocks and the propagation time.

From the foregoing description, it is clear that the basic system principles are no different from those of any ranging system. The important area of difference is in the process referred to as "acquiring the transmitted code." In this system, the acquisition is accomplished in sequential steps or stages starting with the top frequency or clock component. A phase-lock loop tracks this component, filtering out the rest of the code and the additive noise. When lock is achieved, the phase of the transmitted signal is known to be one of the 2^{n-1} possible phases of the top frequency component that occur within one cycle of the lowest frequency component.

The received code is now correlated with the first subfrequency (second highest frequency) and this subfrequency is derived from the phase-locked oscillator. Accordingly, it is coherent with the incoming code with a phase ambiguity of 180 degrees and will correlate to a maximum value over one code period. The correlation will be either positive or negative in sign and, if it is the latter, the derived subfrequency is inverted in sign (shifted 180 degrees)

and the number of possible phases is now reduced to 2^{n-2}. By performing a sequence of n-1 similar subfrequency correlations, all phase uncertainties are removed and the lowest frequency tone counted down from the locked oscillator will be in phase with the received code. It can then be compared to the local clock for a relative-phase measurement, or retransmitted to the source for a round-trip measurement.

The important feature of this system is that acquisition consists of locking to the clock tone and then making n-1 binary decisions in sequence. With a pseudo-random (PRN) code of the same length, and with no a priori knowledge of phase, it is possible that 2^{n-1} decisions would have been necessary for acquisition. Thus under the same set of conditions, the acquisition time of the modem is considerably shorter than its PRN counterpart.

Another feature of equal significance is that although the phase measurement is made at the lowest subfrequency, the phase resolution is derived from the clock tone. This implies that phase differences will be measured with a precision equivalent to the phase jitter on the clock tone, but with a range ambiguity equal to the wavelength of the lowest frequency tone.

2. BREADBOARD DESCRIPTION

2.1 PROCESSOR BASELINE SPECIFICATIONS

2.1.1 Inputs (From Receiver)

2.1.2 Ranging Code

Rate - 625 kilo bits/sec., 13 component code 312.5 KHz clock frequency component (commensurate with 5 MHz)

Input SNR (Noise BW = 2.0 MHz)	-26 dB minimum
Input $\frac{C}{No}$ = 37 dB-Hz	
Signal Plus Noise Level	1.0 Volt RMS (Clipped)

Impedance - The receiver shall be capable of providing the above levels into a modem input impedance of 50 ohms.

2.1.3 Power

Standard 60 cycle 115 volt AC.

2.1.4 Outputs

312.5 kHz - TTL in phase with 312.5 kHz component of code.

76 Hz - TTL in phase with 76 Hz component of code.

READ - TTL inverted pulse. 3.2 usec. wide occuring when subfrequency correlations are completed. This pulse is repeated at about a one second rate when MULTIPLE READ is selected.

2.1.5 Performance Characteristics

With the modem input signal described previously, the following performance parameters shall apply.

2.1.6 Code Acquisition Time

"READ" output available in less than 1.0 second after code voltage is applied to modem.

2.1.7 Range Error Contribution by Modem

With the input signal as defined above: ($\frac{C}{No}$ = 37 dB-Hz) Approximately plus or minus 100 feet (plus or minus 0.1 usec)

2.1.8 Loop Noise Bandwidth, Phase Lock Loop: 15 Hz

2.1.9 Loop Natural Frequency: 4.5 Hz

2.2 SUMMARY OF CIRCUIT DESIGN

The Analog Ranging Modem Processor shown in block diagram form in Figure 1, consists of a phase lock loop circuit which locks onto and tracks the highest frequency tone of the code, a correlation detector which indicates when the phase lock loop is locked to the code, and a correlation circuit which sequentially correlates on each of the subfrequencies of the code. From this, the binary sequence which generates the code is reconstructed in the logic circuits. The reconstructed bottom tone is then compared to an externally generated reference to determine the range. A detailed description of the individual circuits as well as the schematic diagrams follows.

2.3 INPUT AMPLIFIER

The input amplifier shown on Figure 2 is a three-stage, discrete component, differential amplifier. It provides a differential voltage gain of ten and a differential output from a single-ended input to drive the phase-detection circuits.

A 1.5K resistor between the Q1 emitters sets the input clipping level to ±1 volt, while the 2.2 milliamp 2N2219 current source affords common mode rejection (since the input is actually single-ended, the input common mode voltage is one-half of the noisy input signal). Q1 is a low capacitance, monolithic NPN differential pair 2N2920 which provides low input offset and wide bandwidth capability.

Q2 and Q3 are 2N3906 PNP transistors, selected for nominal V_{BE} match at the 2ma operating current. Their high beta and low capacitance offset the need for matching in view of the present

lack of suitable PNP monolithic pairs.

Q6 is nominally biased at 2ma, allowing considerable latitude for output common-mode voltage correction. The A1-Q6 circuit primarily corrects for power supply and component changes, since the first stage current source provides a first order correction of input common mode voltage (CMV).

The differential emitter follower output drives four metal oxide semi-conductor (MOS) integrated analog switches (National NH0014CD) which comprise the double balanced switching phase detectors for the following analog circuits:

a. Phase Lock Loop - Incoming signal multiplied by advanced code and,
Incoming signal multiplied by retarded code

b. Lock indication - Incoming signal multiplied by top tone of code

c. Subfrequency correlator - Incoming signal multiplied by each subfrequency of code.

The output of each MOS switch is summed in differential operational amplifiers A17 through A20. The MOS switch used in a double balanced configuration provides excellent phase detection characteristics; differences of "on" resistance between each switch closure are balanced out in the differential amplifier. The switch accepts a ±10 volt signal range with switching times of about 100 nsec. If it is driven with a low impedance level, the capacitive spike across an opening switch is negligible. The phase detector is, of course, the most critical component in the modem. The test results show that the integrated circuit approach is successful with a -26 dB code to noise ratio, which is at least as good as the results obtained using discrete components.

2.4 PHASE LOCK LOOP

During acquisition of the code analog Switches 5 and 6 are driven with the same quadrature phase of the clock tone performing redundant phase detection. The outputs are summed through two 20K

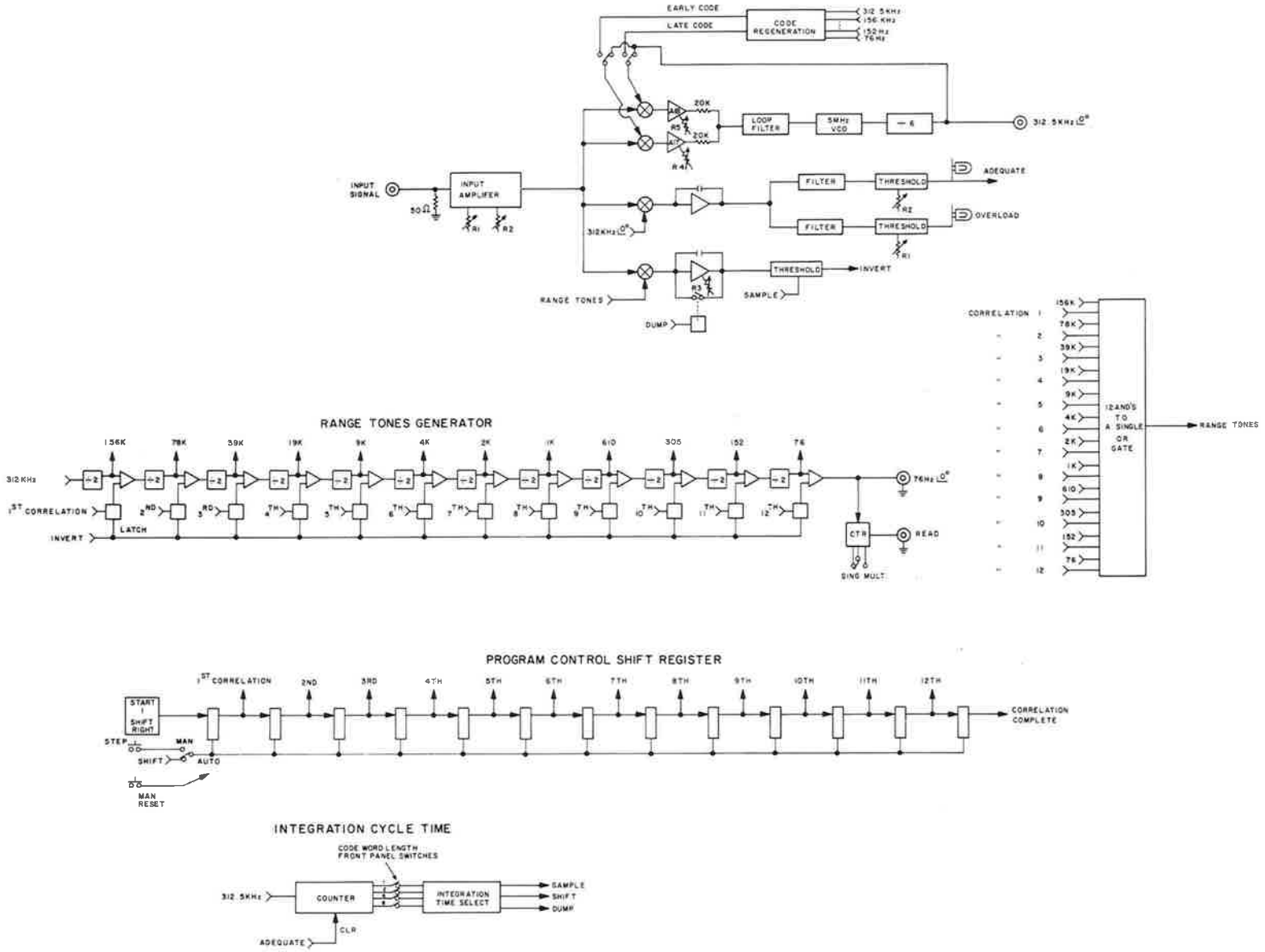


Figure 1. Analog Ranging Modem Processor

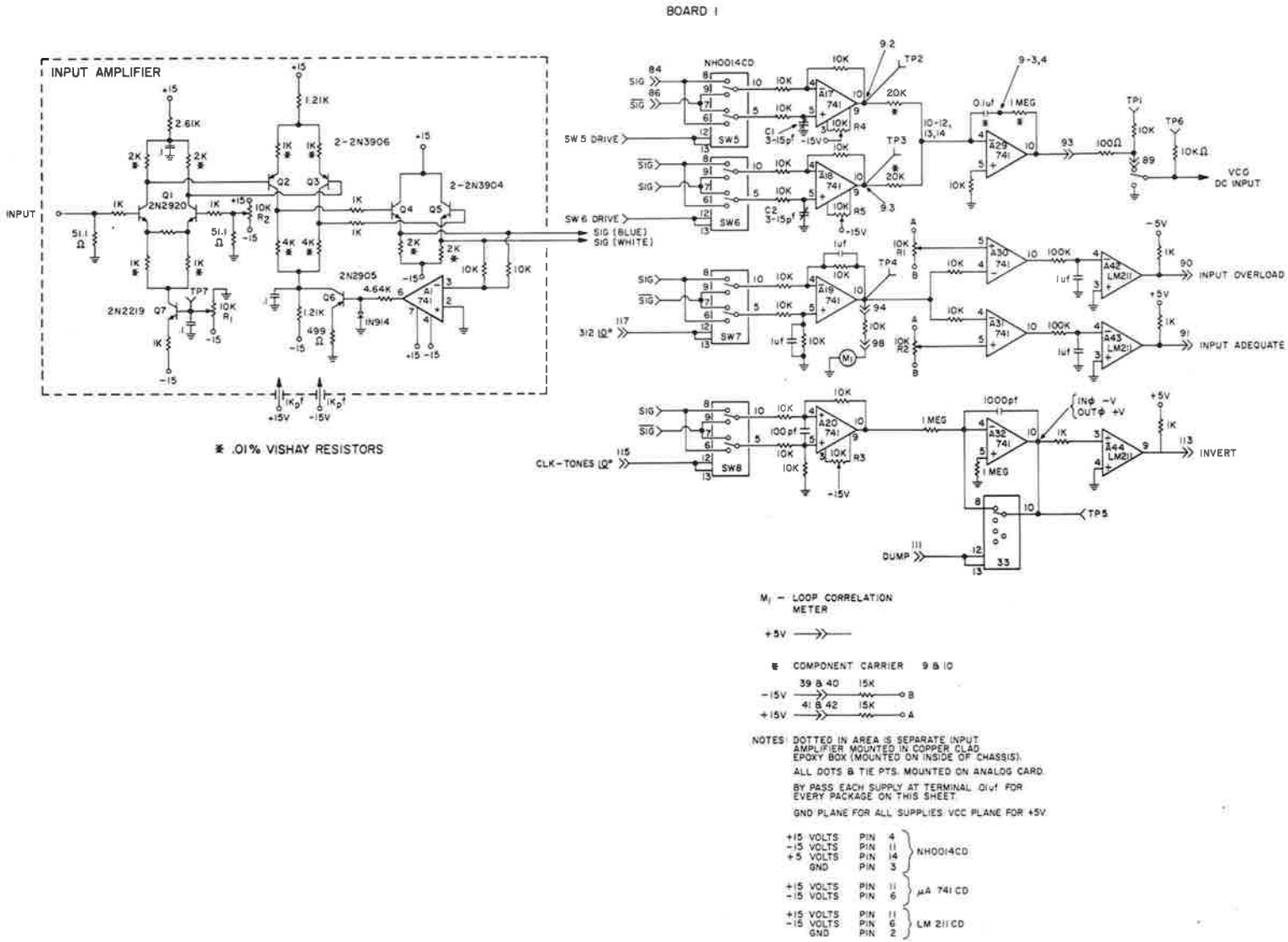


Figure 2. Phase Lock Loop, Range Tones Correlator and Lock Status Indicator

resistors and fed to the loop filter A29. The component values selected provide a loop noise bandwidth of 15 Hz with a damping factor of 0.5 (see Appendix A). The resistive divider at the output of A29 allows a modulating sine wave to be inserted in the loop for bandwidth testing, and Switch 1 enables the loop to be opened conveniently for gain measurements. Once the loop has locked to the clock tone and the subfrequency correlations are complete, the drive to Switch 5 and Switch 6 is changed to a reconstructed ranging code one-half bit advanced and one-half bit retarded respectively. This generates a positive and negative voltage which when summed will be an average of zero for clock loop tracking. This is shown on Figure 3.

2.5 LOCK STATUS CIRCUIT

This circuit consists of a multiplier (MOS Switch 7), differential amplifier and low pass filter A19 followed by two threshold detectors A30 and A31. The code is multiplied by in-phase clock tone which generates a positive voltage proportional to signal amplitude. This represents correlation of input signal and reference. This filtered correlation voltage level is detected by amplifier A30 and A31 with the threshold set so that the code will cause the threshold to be exceeded for an in-lock condition. This output is again filtered by the RC combination and sign detected by A42 and A43 which drive the lamps to indicate whether the input signal is sufficient to make correct range measurements or too strong such that it would saturate the input circuits. Threshold levels are adjustable by R30 and R31.

2.6 SUBFREQUENCY CORRELATION

This consists of a multiplier (Switch 8) followed by a differential amplifier A20. A32 integrates over an integral number of code word lengths, selectable from one to fifteen. At the end of an integration cycle, the charge on the integration capacitor is dumped by Switch 33. Comparator 44 outputs a "1" at the end of the correlation process if the incoming range tone is in phase with the reference range tone and "0" if not. Potentiometer R3 is used to

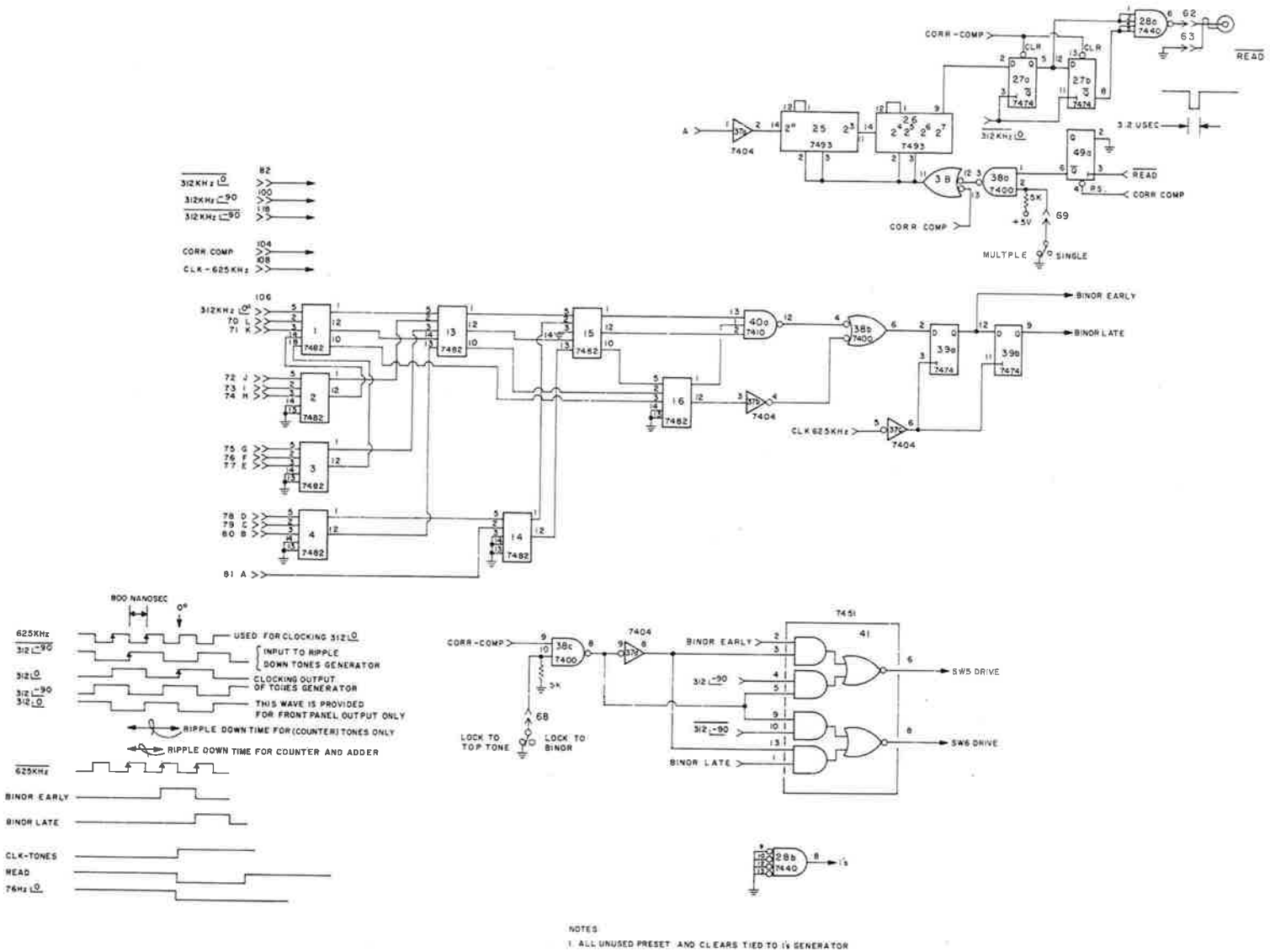


Figure 3. Code Regeneration

adjust the output of amplifier A20 such that under the condition of signal and reference tone in quadrature, the integrator output is zero. Therefore, it will integrate to a positive voltage if in phase and negative if 180 degrees out. The next ranging tone to be correlated with the incoming signal is switched in by the Program Control Logic at "dump" time.

2.7 PROGRAM CONTROL LOGIC (Figures 4 and 5)

When the input signal exceeds the minimum threshold set by comparator A43 "INPUT ADEQUATE" goes high generating the "CLK-GO" pulse which shifts the program control register one stage right. This advances the program control one step (Packages 41 through 46). Range tones generated internally in Packages 13, 15, 17, 19, 21, and 23, are successively switched into the subfrequency correlator and integration performed over the selected number of integration cycles counted by Packages 33, 34, 35, 36. A "SAMPLE" pulse to interrogate the integration comparator then causes a "DUMP" pulse to discharge the integrator and finally causes a shift right in the program control directing the next lower range tone to repeat the process. After the last range tone is correlated a final shift right causes the "IN PROCESS" lamp to extinguish and the complete lamp to illuminate. The particular correlation being performed is indicated by front panel lamps in a binary sequence.

2.8 RANGE TONES GENERATOR

Each range tone is derived from the clock tone by successively dividing by two in Packages 13, 15, 17, 19, 21, and 23. The tones are all gated out to the subfrequency correlator through Packages 3, 4, 5, and 6. Flop 7 reclocks each to be in syncronization with the top tone. Each tone as it exits Flop 7 may either be in or 180 degrees out of phase with the tones contained in the incoming code. The subfrequency correlator determines which is the correct phasing and sets the latch (Package 20) which controls the inverter (Package 14) this process is repeated for each range tone.

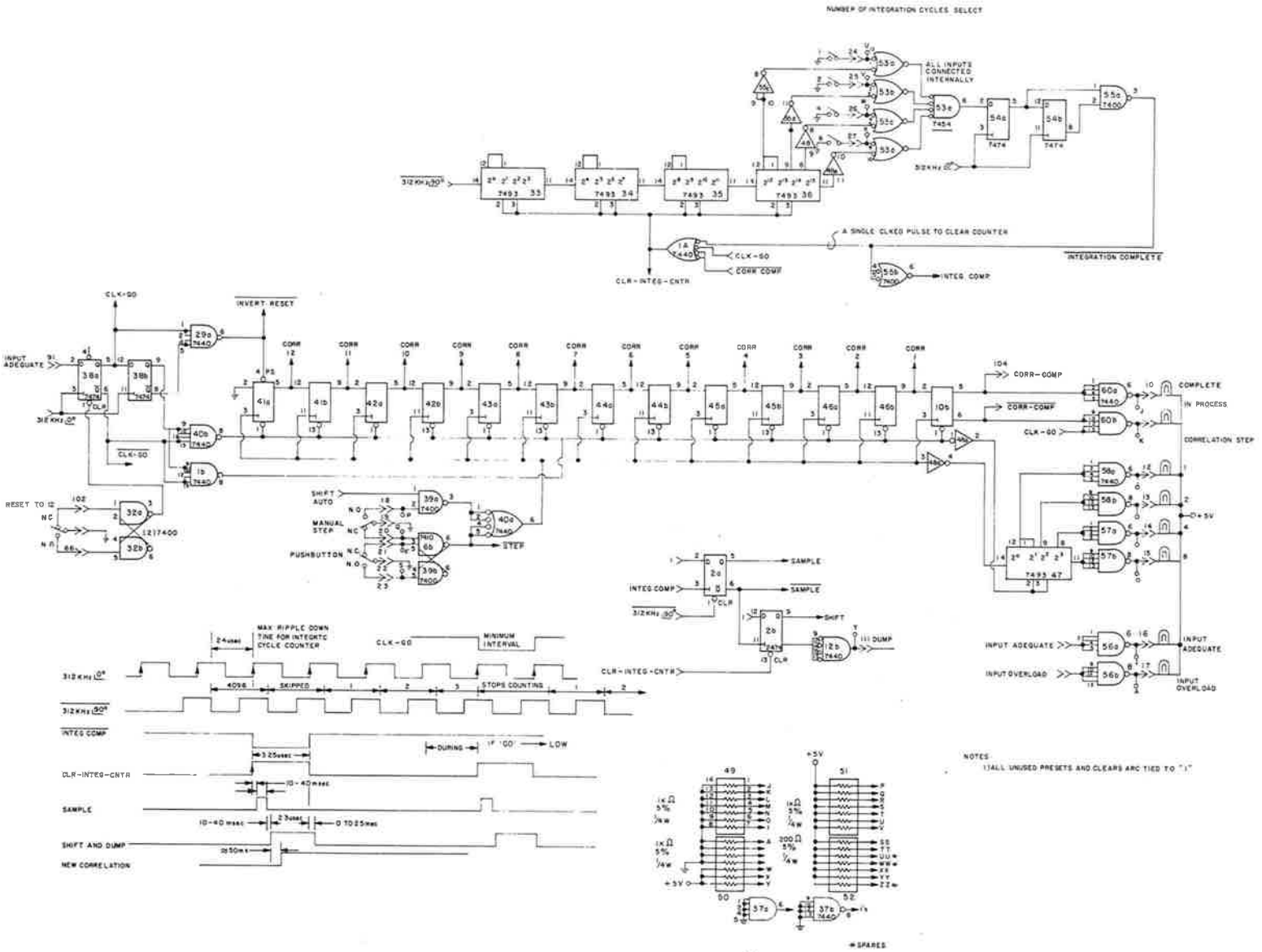


Figure 4. Program Control

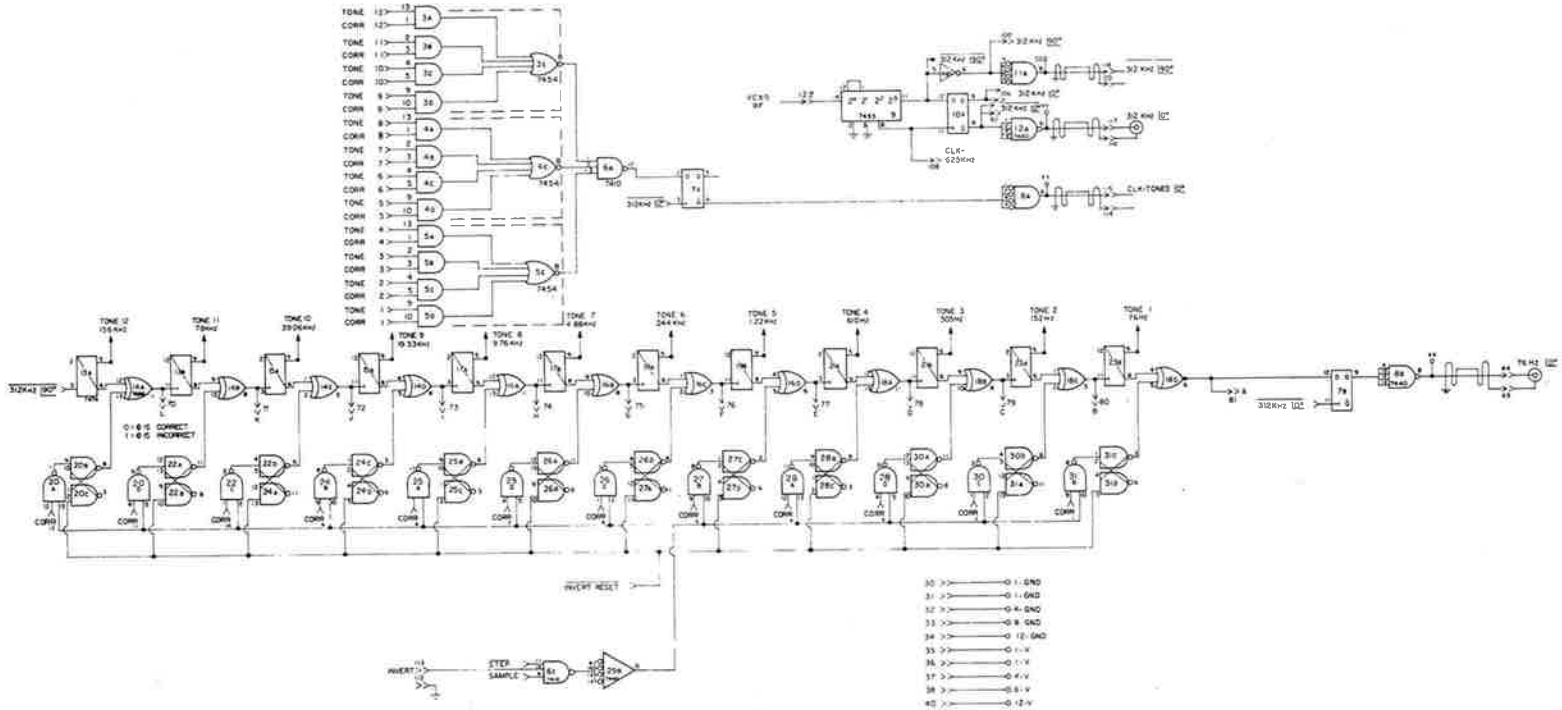


Figure 5. Correlation Tones Generator and Controlled Invert Function

2.9 FRONT PANEL CONTROLS

The input BNC accepts the signal together with additive noise. A minimum of 30 millivolts rms of signal is required to operate the modem, and sufficient to illuminate the "INPUT ADEQUATE" lamp. If the input signal exceeds 60 millivolts rms "INPUT OVERLOAD" illuminates warning of possible saturated condition in the input amplifier. The modem will tolerate white noise 26 dB greater than the signal at the input.

Loop CORRELATION meter is a relative indication of the correlation voltage out of the lock status detector circuit. This meter may be used for setting ADEQUATE and OVERLOAD thresholds.

RANGING TONE CORRELATION lamps illuminate in a binary sequence to indicate which subfrequency is undergoing correlations. IN PROCESS is illuminated while the correlations are being made and COMPLETE illuminates at the termination of the process.

INTEGRATION CYCLES switches select the number of code word lengths to integrate over, adjustable from one to fifteen. The AUTO position automatically cycles the program control logic through each of the subfrequency correlations, MANUAL sequences through each subfrequency singly with depression of STEP push button. RESET push button puts the program control back to the initial state where the first subfrequency is being correlated.

SINGLE RANGE READINGS outputs a single pulse at the BNC connector coincident with the reconstructed (76 Hz) lowest ranging tone upon completion of the subfrequency correlation process.

MULTIPLE RANGE READINGS outputs a pulse as above at one-second intervals. This pulse is used to start a time interval counter, which is stopped by an externally generated reference 76 Hz. The counter reading then represents the propagation delay. Multiple counter readings provide an indication of the phase jitter inherent in the locked loop. TOP TONE switch selects the ganged correlator mode of operation in the CODE position. BNC connectors marked 312 kHz and 76 Hz output those components of the reconstructed code in phase with the incoming code.

2.10 ALIGNMENT PROCEDURE

1. Adjust R1 (input amplifier) for -12.40 volts at TP7 to ground.
2. With loop locked up 30 mv of TOP TONE input, adjust R2 (input amplifier) for minimum amplitude and distortion of the sine wave at TP2 and TP3.
3. Disconnect the 20K resistor at the output of A18. With the loop locked and 30 mv of analog code signal input, adjust R4 for zero phase shift between 312.5 kHz out of the processor and the same tone out of the generator.
4. Mix 600 mv rms of white noise with the input signal and adjust C1 for optimum loop performance as noise is increased from zero to 600 mv.
5. Reconnect the 20K resistor.
6. Repeat steps 3, 4, and 5 for the 20K resistor at A17 and R5. Adjust C2.
7. Lock processor to 30 mv rms of analog code. Adjust R2 such that the green INPUT ADEQUATE lamp illuminates at an input greater than 30 mv and extinguishes at less than 30 mv.
8. Lock processor to 60 mv rms of analog code. Adjust R1 such that the red INPUT OVERLOAD lamp illuminates at an input greater than 60 mv and extinguishes at less than 60 mv.
9. Lock processor to 30 mv of analog code inverted. Switch to MANUAL correlation mode and push RESET, then step to the first correlation. Adjust R3 for an integration to zero volts at TP5.

3. TEST DESCRIPTION AND RESULTS

3.1 INTRODUCTION

The analog ranging modem was tested in the laboratory under various conditions of input signal-to-noise ratio (SNR) loop bandwidths of the phase lock loop, and code structure. The system performance variables of primary interest are loop acquisition time, subfrequency correlation error, and phase jitter which represents ranging accuracy.

3.2 LOOP ACQUISITION TEST (Figures 6 and 7)

Acquisition time is defined here as the time interval from when a code signal appears at the modem input until the time that the subfrequency correlations begin. This time interval consists primarily of the time required for the phase lock loop to lock onto the top tone of the code, which is a function of the loop bandwidth and not dependent on the signal-to-noise ratio directly. However, at extremely small $\frac{C}{No}$ (about -37 to -39 dB-Hz), there is some degradation in the acquisition time. Figure 7 plots a hundred reading average of acquisition time versus $\frac{C}{No}$ for different values of $\frac{C}{No}$. Also plotted is the distribution of acquisition time for 100 readings at a $\frac{C}{No}$ = 43 dB-Hz.

The probability of acquisition is 100 percent at all $\frac{C}{No}$ ratios greater than 37 dB-Hz. At 36 dB-Hz, it drops to 99.5 percent and degrades rapdily from there. Figure 6 is the test setup for acquisition time measurements.

For a given bandwidth acquisition time is fixed and given by

$$TACQ \approx \frac{(\Delta w)^2}{2 \zeta W_m^3}$$

where: Δw is the initial frequency offset

ζ loop damping factor

W_m loop natural frequency

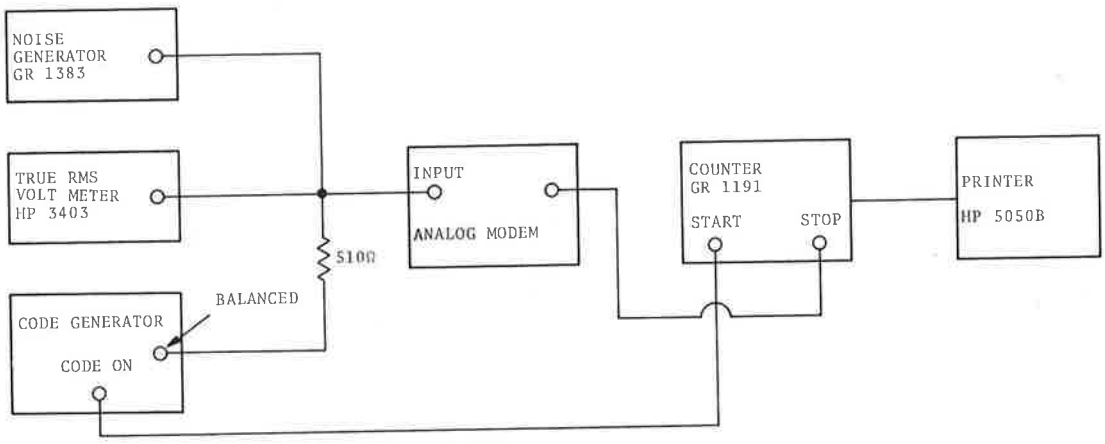


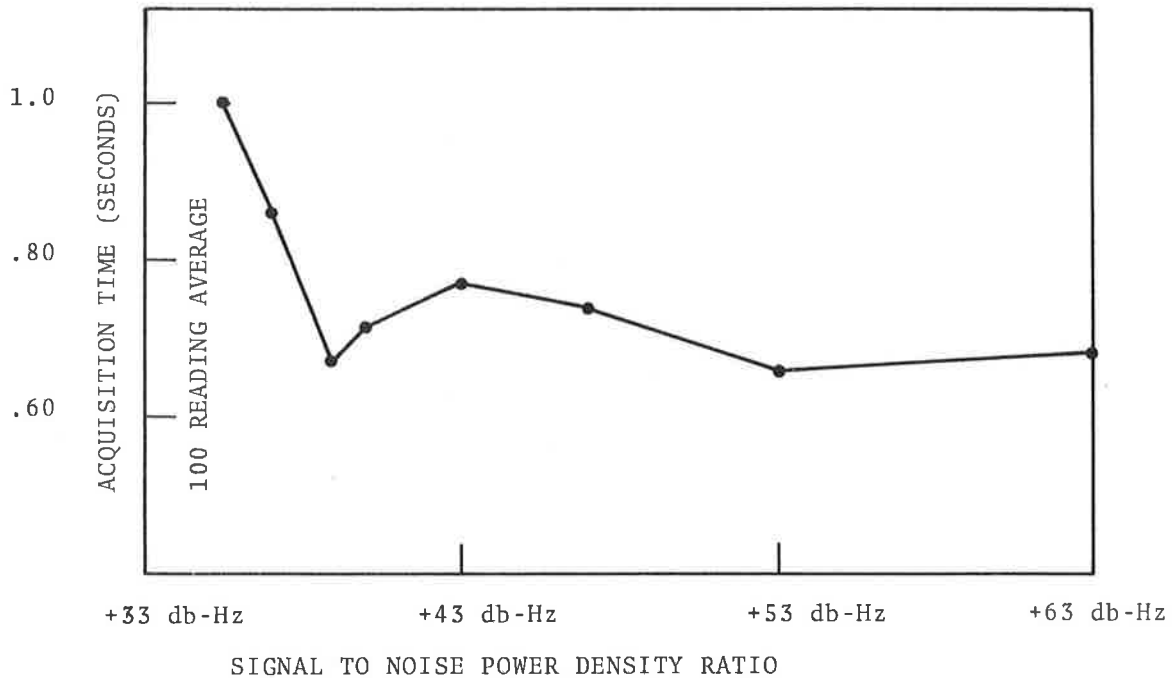
Figure 6. Acquisition Time Measurements

There are two approaches to reducing Acquisition Time; one is to apply a sweep voltage to the VCO and search for the input frequency. If done properly, the loop will lock up as the VCO sweeps into the input frequency. The other is to change the loop bandwidth. Starting with a wider bandwidth for rapid acquisition and switching to a narrow bandwidth for minimum jitter.

Both methods are being considered for the ranging equipment being designed for the ATS-F experiment. The clock tracking loop will be implemented completely with digital integrated circuits. Simulating the analog functions with digital logic enables great flexibility in manipulating loop performance under varying input signal conditions.

3.3 SUBFREQUENCY CORRELATION ERROR TEST

Figure 8 is a block diagram of the test setup used for measuring subfrequency correlation errors as well as the failure to lock condition. A subfrequency correlation error is any condition



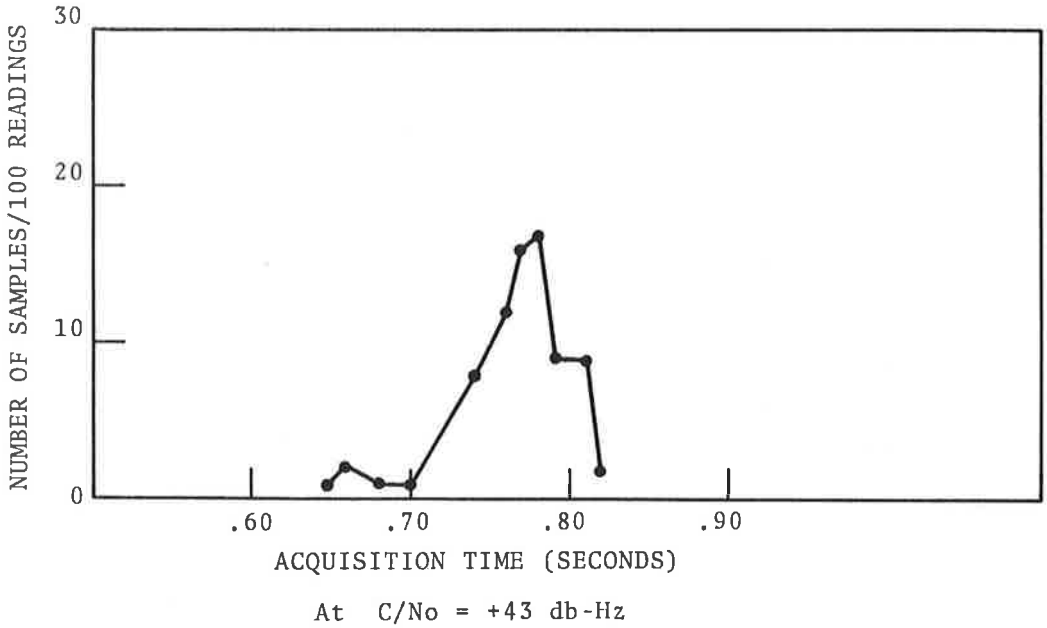


Figure 7. Signal to Noise Power Density Ratio and Acquisition Time

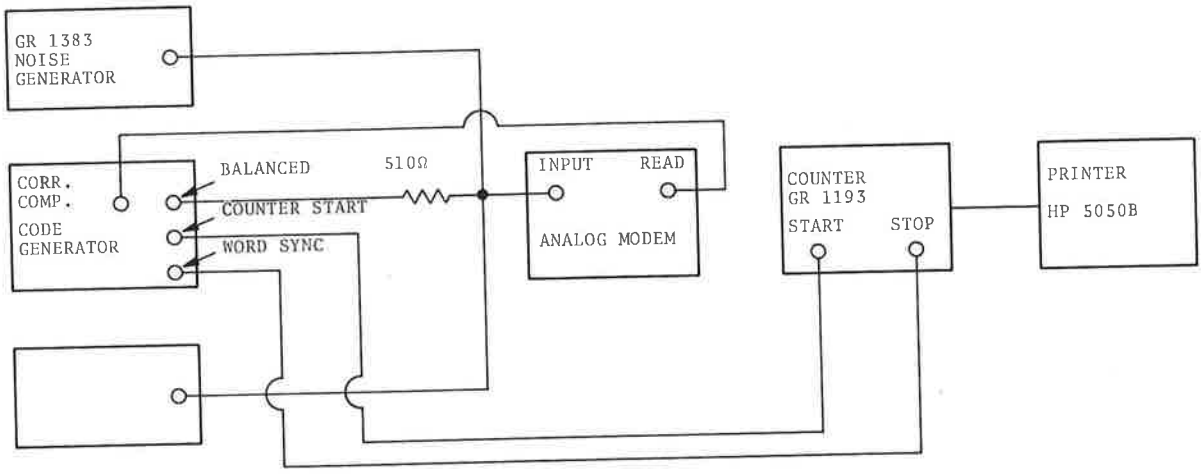


Figure 8. Subfrequency Correlation and Failure to Lock

where a mistake is made in determining the correct phase of any one of the subfrequencies during one acquisition sequence. In evaluating the ranging data, any range time which deviated from the nominal time by more than one cycle time of the top tone (3.2 usec.) was considered to be an error. Any deviations less than this amount were caused by noise producing jitter in the phase lock loop. The failure to lock condition is indicated by the counter measuring half of the code length time which is a 6558.5 milliseconds reading rather than the phase delay which is nominally 1.5 microseconds plus an additional "delay" time if selected or a correlation error. At $\frac{C}{No}$ greater than 37 dB-Hz there were no correlation errors or failure to lock made in ten thousand readings; at 36 dB-Hz $\frac{C}{No}$ ten percent of the readings were in error or failed to lock. It is obvious that the processor exhibits an operating threshold of 37 dB-Hz. At greater $\frac{C}{No}$'s, acquisition and correct correlation is guaranteed. At lower $\frac{C}{No}$'s, the performance degrades severely.

3.4 ACCURACY TEST

The ranging accuracy test uses the test set up shown in Figure 9. Ranging error is the measurement of the RMS jitter in recorded range time. This jitter is primarily due to the effects of noise in the phase lock loop and is a function of the loop bandwidth. The jitter was approximately 300 nsec. at a $\frac{C}{No}$ of 37 dB-Hz and dropped to 100 nsec., at 53 dB-Hz, and was unrecordable at 63 dB-Hz.

A significant improvement was obtained at the lower $\frac{C}{No}$ (37 to 43 dB-Hz) by using the code correlation mode. Jitter dropped to about 200 nsec. (See Appendix B for discussion).

Because these measurements were made with a counter having 100 nsec. resolution, the results of this test are approximate. This test should be repeated with a 10 nsec. time interval counter.

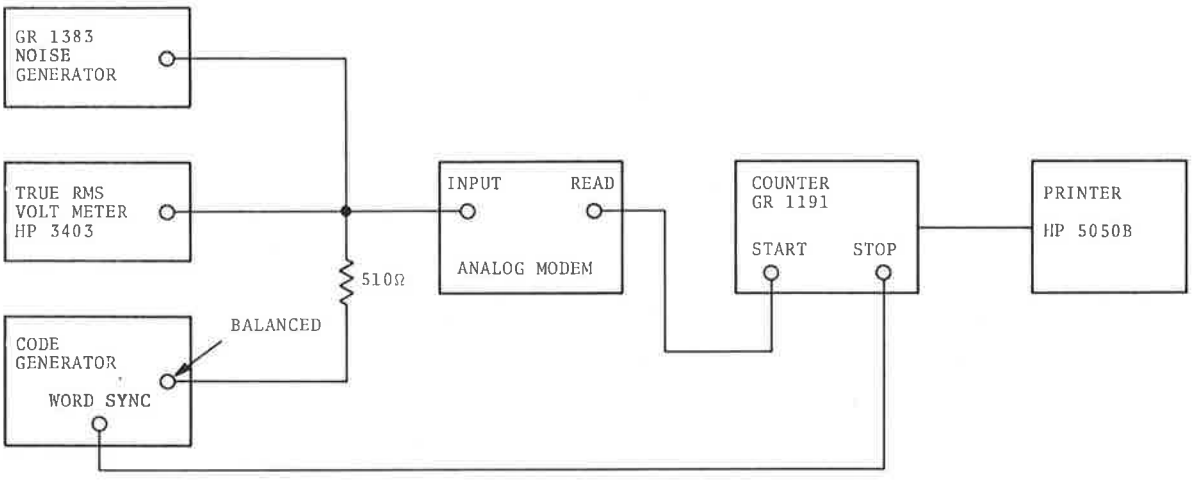


Figure 9. Ranging Accuracy

3.5 TEST RESULTS AND RECOMMENDATIONS

A comprehensive testing program is planned to compare the performance of the analog with the digital ranging modem counterpart. The digital ranging modem is still in the circuit design state. The test program will include environmental testing as well as detailed performance measurements. Much of the experiments will be to assess performance and to discover the failure modes. It is recommended that additional effort be devoted to complete construction of the digital ranging modem and to conduct such a test program. Testing performed to date has given assurance that the unit performs reasonably well. All circuits work within the assumed operating tolerances. The major design issues addressed to date are acquisition, correlation errors, and accuracy. All should be investigated further. The results of the test program will guide recommendations for design changes to improve performance at low $\frac{C}{No}$. Specific areas of design improvements are summarized here.

Some thought might be given to changing the ratio of clock tone power to lower tone power, since the loop fails to lock long before correlation errors are made. Alternately, the failure to lock might be investigated to effect a significant improvement in the weakest link, the phase detector. This is the critical circuit component in determining the lowest SNR of operation. Performance is curtailed from two sides:

1) The DC offset voltage which exists between each pole of the switching multiplier;

2) The noise peaks which exceed the maximum allowable signal excursions, resulting in a DC potential due to unsymmetrical clipping.

A number of different approaches have been tried, including various commercially available analog multipliers, and a design employing all discrete components. The MOS analog switch proved to be greatly superior to all others, and we feel that with more effort, performance could be further improved.

Also planned is testing of the loop to determine if it operates as predicted by classic loop equations given by Gardner and others; in particular, acquisition time, lock-in range, pull-in range, hold-in range and phase jitter. Multipath effects need to be investigated also, although the existing simulator does not have the necessary bandwidth.

4. SUMMARY AND CONCLUSIONS

The primary feature of the Analog Ranging Modem is its ability to function with weak input signals in high noise environments with rapid acquisition. In addition, the implementation and operation of this unit is extremely simple, with a minimum of components and high reliability. A design goal for the breadboard was to acquire and operate at an input signal-noise power density ratio of +43 dB-Hz. Test data demonstrates satisfactory performance for $\frac{C}{No}$ as low as +37 dB-Hz in laboratory conducted noise measurement tests. This ranging modem demonstrates the successful implementation of advanced integrated circuit technology with the attendant qualities of small, simple packaging. Performance is, as indicated by preliminary testing, at least as good or better than equivalent discrete components systems which are far more complex. It is also concluded that this modem is a candidate for an AEROSAT ranging experiment.

5. RANGING CODE GENERATOR

5.1 INTRODUCTION

A generator was designed and constructed to provide both the "sum of twelve tones" ranging code used with the analog modem and the "four phase modulated tones" ranging code used with the digital modem. Also, it was provided with many features which accommodate different test functions for present and future requirements.

5.2 SUM OF TWELVE CODE (ANALOG RANGING MODEM)

This is a binary code which is formed by adding together thirteen square waves, each twice the frequency of the preceding, and hard limiting the sum. This produces a binary code which is almost optimum[1] when the ranging signal acquisition search is performed serially. More information about the code and its acquisition is contained in Section 1.1 of this report.

This code is processed with conventional Analog phase lock loops and correlation circuitry hence it is referred to as the Analog Modem Code although it is a digitally generated binary code.

5.3 ANALOG RANGING MODEM CODE GENERATION

An internal or external source of stable 5 MHz is counted down in a string of binary dividers (Packages 13, 25, 37, 49) down to the lowest ranging tone (76 Hz) required. Each of the thirteen ranging tones are generated and fed to a group of adders (Packages 10, 22, 34, 46, 11, 35, 23, 47) which combine the tones such that a "1" is generated if the majority are high and a "0" if the majority are low. Ripple down time in the binary dividers is small enough so that no resyncronization is required in the tones before entering the adders, but large enough to cause glitches which are removed by Flop 12a from which either true or inverted code is available and selectable.

5.4 FOUR PHASE MODULATED TONES (DIGITAL MODEM) CODE

This is a binary code which is formed by phase modulating a subcarrier with four range tones. The tones have frequency ratios of 8:1, and are selected so that the digital modem is capable of the same phase and ambiguity resolution as the analog modem. The frequencies used are as follows: 76 Hz, 610 Hz, 4.8 kHz, and 39 kHz. The tones are phase modulated at a subcarrier of 312.5 kHz, which also serves as the clock tone for the modem.

5.5 DIGITAL MODEM CODE GENERATION (Figure 10)

Each of the four ranging tones and the subcarrier are resynchronized first, with 625 kHz in Flops 3a, 15a, 27b, 39b, 51b, and second with 5 MHz in Flops 3b, 15, 27b, 39b, 51b. This established both true and inverted ranging tones at precisely zero phase to be used in the phase modulator. Phase modulation is performed in four consecutive circuits. The operation is identical in the four modulators and only the first will be described.

Gate 56b is enabled and passes the subcarrier (clock tone) when the 39 kHz tone is high; when not, gate 56a passes the subcarrier but inserts a variable delay with Flop 55a. This delay causes a phase displacement of the subcarrier at every transition of the 39 kHz ranging tone. The variable delay provides a method of increasing the deviation of phase modulation such that increasing amounts of energy are put into the ranging tones for experiments to determine optimum SNR for the ranging tones and subcarrier independently.

5.6 SPECIAL FEATURES OF THE CODE GENERATOR (Figure 11)

The generator may be driven from an EXTERNAL REFERENCE (5 MHz) or the INTERNAL REFERENCE may be selected which is variable over a 1.0 percent range. The DEVIATION control varies the degree of phase modulation which is imposed on the 312.5 kHz subcarrier by the four range tones of the digital ranging code. It is continuously variable from 11 to 45 degrees deviation. The RANGE TONES selects one of the twelve ranging tones and outputs it at the TONES BNC connector.

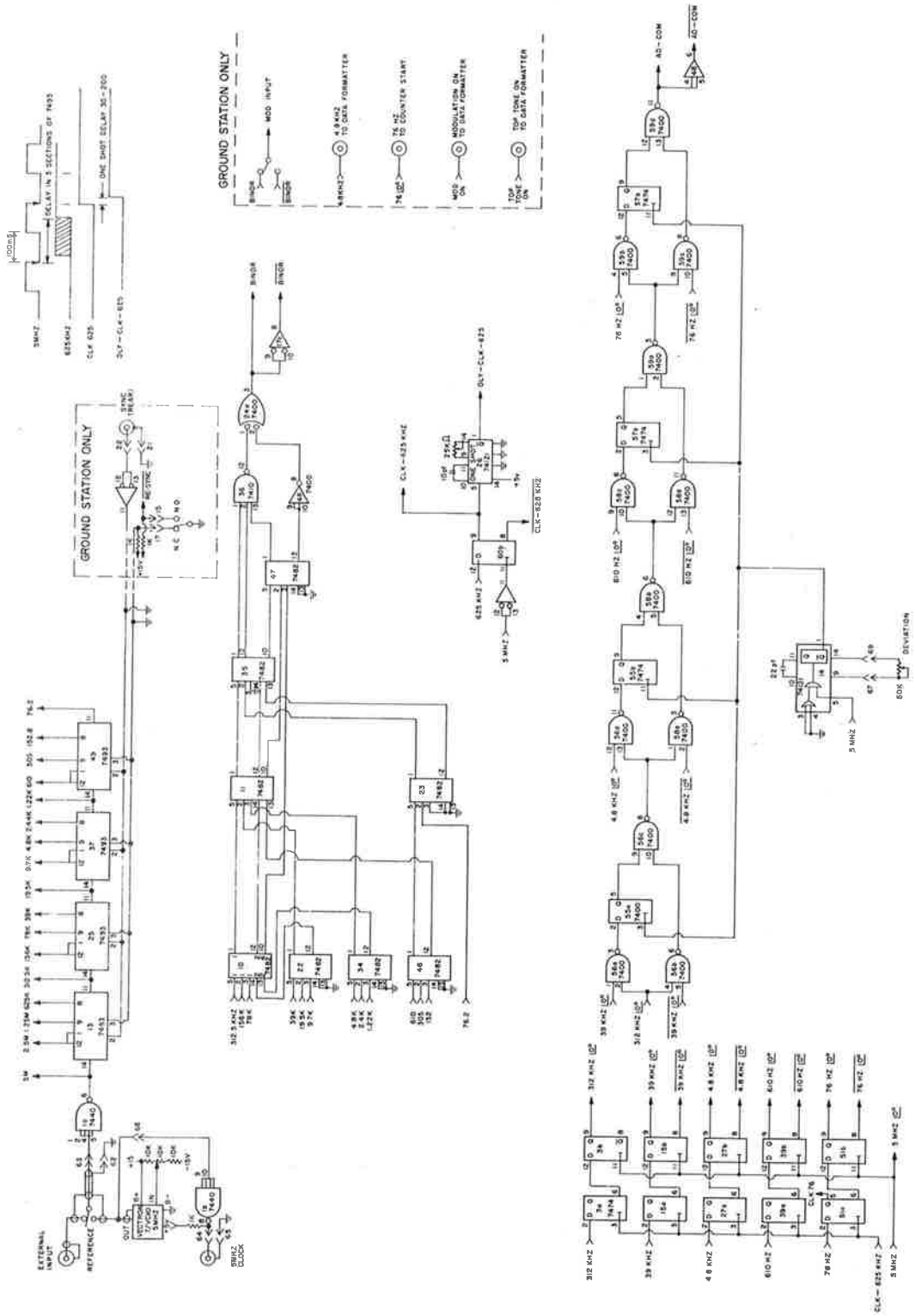


Figure 10. Ranging Code Generator - Code Generation

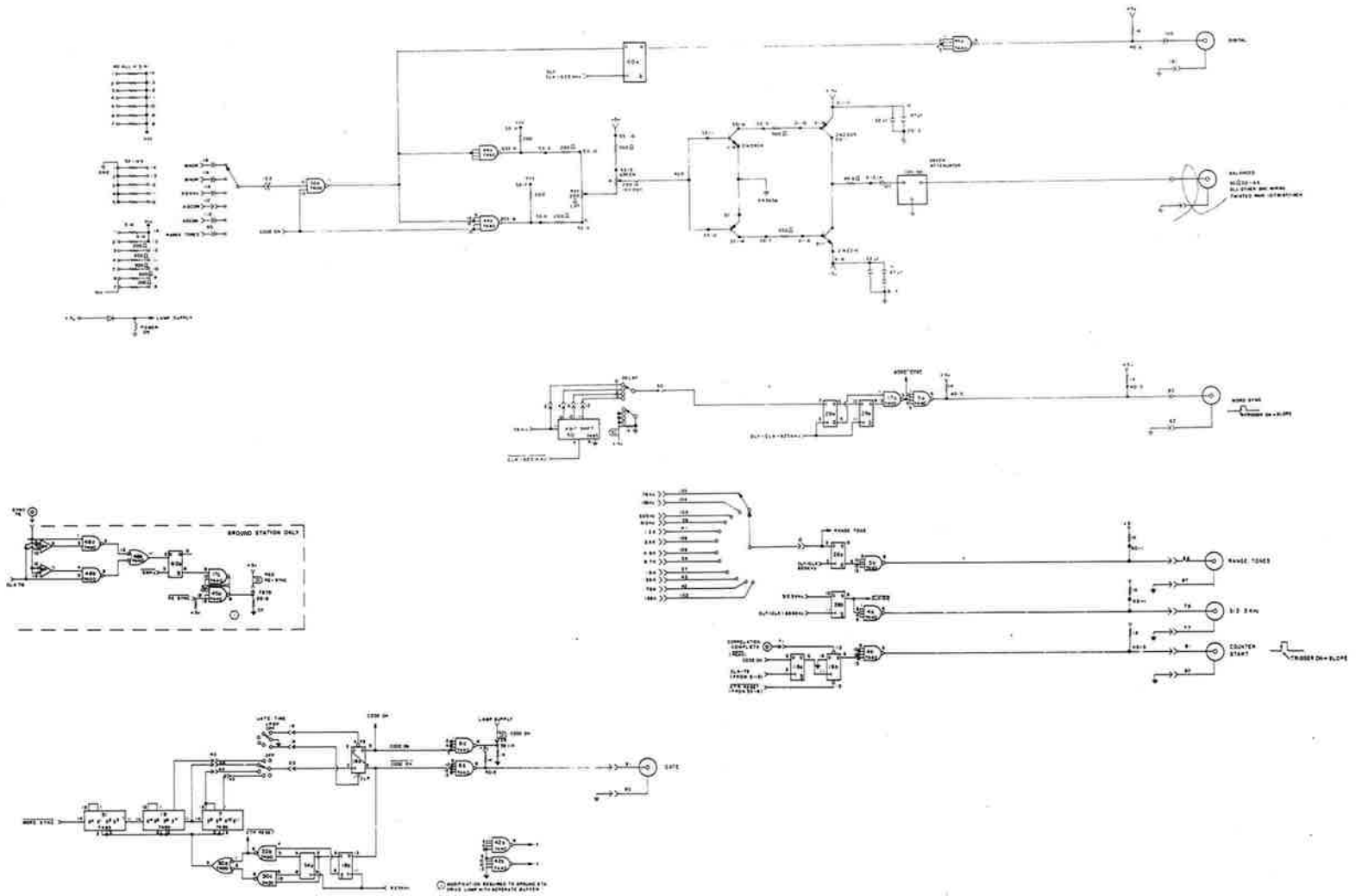


Figure 11. Ranging Code Generator - Peripheral Features

DELAY selects a fixed 1.6 usec. delay multiplied by 0, 1, 2, or 3, inserted in the WORD SYNC output. This allows small adjustments to be made in phasing outputs from the generator and processor for optimum time interval counter measurements.

GATE turns the code on and off with the interval selected. It is available as an output at the GATE BNC.

Five modes are front panel selectable. They are the codes for for:

(1) The digital, or

(2) The analog modem,

(3) The analog code inverted to compensate for an odd number of inversions in the transmeter link,

(4) The range tone which may be fed to the output circuits,

(5) The clock tone.

The output circuits provide both a digital output, directly from a TTL buffer, or a balanced output from a discrete driver which produces a 5 volt peak-to-peak waveform centered about zero volts. An attenuator reduces this in 2 dB steps to 40 dB.

CORRELATION COMPLETE BNC accepts a signal from the processor at the end of the correlation cycle and outputs a pulse in sync with the lowest ranging tone (76 Hz) at the COUNTER START BNC. Then the 76 Hz reconstructed wave out of the processor may be used to stop the counter. WORD SYNC is a 3.2 usec wide pulse at the start of each 76 Hz tone, it may be delayed which proves useful for the counter STOP pulse.

APPENDIX A

PHASE LOCK LOOP (PLL) ANALYSIS

The PLL can be represented by the following block diagram:

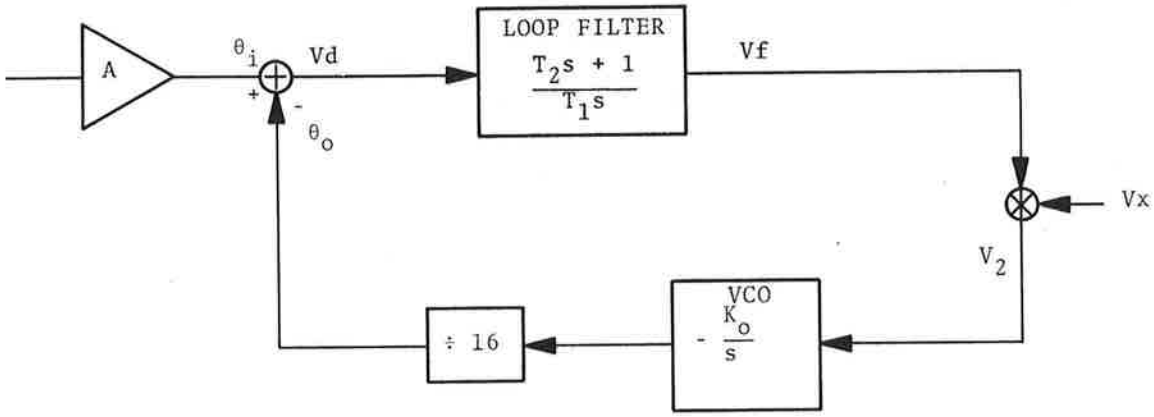


Figure A-1. The Phase Lock Loop

Where θ_i = input phase in radians

θ_o = output phase in radians

KØ = phase detector constant volts/radian

Vd = phase error voltage volts

Ko = oscillator scale factor rad/volt-sec

$Vd(s) = K\emptyset\ \theta(s)$ if $\theta i = 0$

$Vf(s) = Vd\ F(s)$

$V2(s) = Vf(s) + Vx(s)$

$\theta_o(s) = \frac{Ko}{S}\ V2(s)$

Vx is an external modulating voltage inserted in the loop for testing damping and bandwidth. Initially assume Vx = 0 and derive loop equations.

This is a second order loop with the phase transfer function:

$$\frac{\theta o\ (s)}{\theta i\ (s)} = H\ (s) = \frac{2\ \zeta\ \omega ns + \omega n^2}{s^2 + 2\ \zeta\ \omega ns + \omega_n{}^2}$$

where $\omega n = \left(\frac{K_o\ K\phi}{\tau_1}\right)^{\frac{1}{2}}$ is the loop natural frequency, (1)

and $\zeta = \frac{\tau_2}{2}\left(\frac{Ko\ K\phi}{\tau_1}\right)^{\frac{1}{2}}$ is the loop damping factor.

For a damping factor of $\zeta = 1/2$

$$T_2 = \frac{1}{\omega_n} \text{ and } T_1 = \frac{Ko\ K\phi}{\omega_n{}^2}$$

The parameters for this loop are:

$$Kvco = 2.5\ \Pi\ \frac{rad/sec}{Volt}$$

$$K\phi = \frac{340\ mvP\text{-}P}{\Pi\ rads}$$

If the loop natural frequency is chosen to be $\omega n = 10$ rad/sec., and the loop filter capacitor chosen to be 0.1uf then the values for loop filter resistors R1 and R2 may be computed as follows:

$$T_2 = CR_2 = \frac{1}{\omega_n} = .1 \text{ sec}$$

$$R_2 = \frac{.1 \text{ sec}}{10^{-7}\text{uf}} = 1 \text{ Meg } \Omega$$

$$T_1 = R_1C = \frac{Ko\ K\phi}{\omega_n{}^2} \quad \frac{2.5\Pi\ \frac{340}{\Pi}\ x\ 10^{-3}}{10^2} = 850 \times 10^{-5} \text{ sec}$$

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[1] Gardner, op. cit., pg. 9.

$$R_1 = \frac{850 \times 10^{-5}}{10^{-7}\text{uf}} = 85\text{K}\Omega$$

In order to test the loop's performance with the calculated filter values, a test signal is injected into the loop between the filter and VCO. It is simply added as shown below with a resistive mixer which has negligible effect on loop calculations.

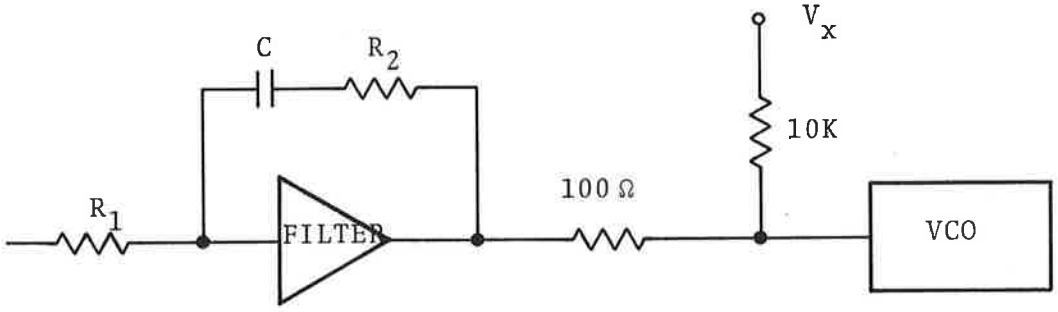

Figure A-2. Block Diagram of Analog Ranging Modem

From the block diagram the following relationships result when $Vx \neq 0$:

$$\theta o\ (s) = \frac{Ko}{S}\ (Vf + Vx) = \frac{Ko}{S}\ (Vd\ F(s) + Vx)$$

$$\theta o\ (s) = \frac{Ko}{S}\ [Kd\ \theta o\ (s)\ F(s) + Vx]$$

$$\theta o\ (s) = \left[\frac{Ko\ Kd}{S}\ F(s)\ \theta o\ (s)\right] + \left[\frac{Ko}{S}\ Vx\right]$$

$$\theta_o\ (s)\left(1 + \frac{Ko\ Kd}{S}\ F(s)\right) = \frac{Ko}{S}\ Vx$$

$$\frac{\theta_o\ (s)}{Vx\ (s)} = \frac{\frac{Ko}{S}}{1 + \frac{Ko\ Kd}{S}\ F(s)}$$

$$\frac{\theta o\ (s)}{Vx} = \frac{s\ Ko}{s^2 + Ko\ Kd\ F(s)\ s} = \frac{Ko\ s}{s^2 + Ko\ Kd\ s\left(\frac{T_2 s + 1}{sT_1}\right)}$$

$$= \frac{Ko\ s}{s^2 + \underbrace{\left(\frac{Ko\ Kd\ T_2}{T_1}\right)}_{2\zeta\omega_n} s + \underbrace{\left(\frac{Ko\ Kd}{T_1}\right)}_{\omega_n^2}} = \frac{Ko\ s}{s^2 + 2\zeta\omega s + \omega_n^2}$$

$H(s) = \frac{\theta o\ (s)}{Vx}$ is the transfer function of phase error due to

1) input FM

or 2) Vx mixed in after F(s). (1)

if the magnitude of the amplitude of H(s) is plotted versus frequency of Vx, a bell-shaped curve of Figure A results. To find the 3 dB points on the curve set:

$$H\ (j\omega)^2 = \tfrac{1}{2} H\ (j\omega_n)^2$$

two values of ω should result ω_L & ω_H

$$\left|\frac{\theta o\ (s)}{}\right| = \left|\frac{Ko\ s}{s^2 + 2\zeta\omega_n s + \omega_n^2}\right|$$

$$\left|\frac{\theta o\ (j\omega)}{Vx}\right| = \left|\frac{Ko\ j\omega}{\underbrace{\left(2\zeta\omega_n j\omega\right)}_{\text{imag.}} + \underbrace{\left(\omega_n^2 - \omega^2\right)}_{\text{real}}}\right|$$

$$H(j\omega) = \frac{Ko\ \omega}{\left[(2\zeta\omega_n\ \omega)^2 + (\omega_n^2 - \omega^2)^2\right]^{\frac{1}{2}}}$$

if $\omega = \omega_n$

$$H(j\omega_n) = \frac{Ko\ \omega n}{[(2\zeta\omega^2) + 0]^{\frac{1}{2}}} - \frac{Ko}{2\zeta\omega_n}$$

$$|H(j\omega)|^2 = 1/2\ |Hj\omega|^2$$

$$\frac{K^2\omega^2}{(\omega^2_n - \omega^2)^2 + (2\zeta\omega_n\omega)^2} = \frac{1/2K^2\omega n^2}{(\omega_n^2 - \omega_n^2) + (2\zeta\omega_n^2)^2}$$

which reduces to:

$$\omega^2 \pm 2\zeta\omega_n\omega - \omega_n^2 = 0$$

$$\omega = \omega_n\left[\pm\zeta \pm \sqrt{\zeta^2 + 1}\right]$$

Since ζ is always positive and ω must be positive the negative radical can be discarded.

$$\omega\ \text{High} = \omega_n\left[+\zeta + \sqrt{\zeta^2 + 1}\right]$$

$$\omega\ \text{Low} = \omega_n\left[-\zeta + \sqrt{\zeta^2 + 1}\right]$$

$\omega H - \omega L = \omega n 2\zeta$

OR

$$\text{damping factor}\ \zeta = \frac{\omega H - \omega L}{2\omega n}$$

This expression provided a laboratory procedure for determining damping factor from the measurable parameters.

The data of this test is tabulated and plotted in Table A and graphed in Figure A-3.

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(1) Gardner, op. cit., pg. 126

TABLE A-1. TEST DATA USED TO DETERMINE DAMPING FACTOR AND LOOP NATURAL FREQUENCY

MODULATING FREQUENCY IN Hz	$\lvert H(jw) \rvert$ P-P EXCURSION CM	$\lvert H(jw) \rvert^2$
.1	.3	.09
.3	.4	.16
.5	.4	.16
1.0	1.0	1.0
1.5	1.6	2.56
2.0	2.2	4.84
2.5	2.7	7.3
3.0	3.1	9.6
3.5	3.5	12.2
4.0	3.6	13.0
4.5	3.7	13.7
5.0	3.6	13.0
5.8	3.5	12.2
6.8	3.2	10.2
8.0	2.8	7.85
9.8	2.4	6.5
14.1	1.6	2.56
18.5	1.2	1.44
24.2	1.0	1.0
31	0.8	.64
43	0.6	.36
64	0.4	.16

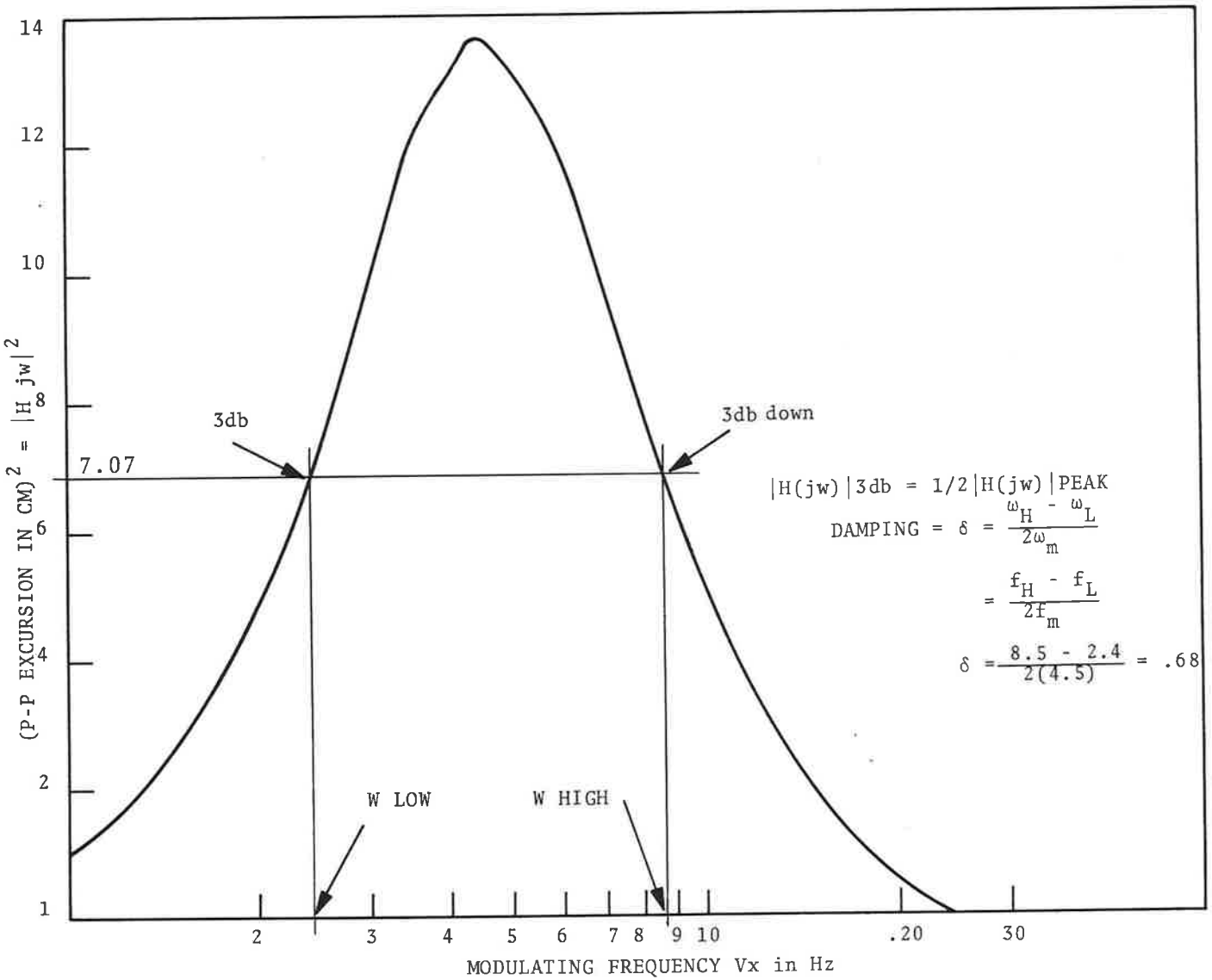

Figure A-3. Closed Loop Phase Response

APPENDIX B

CODE CORRELATOR

The code correlator is designed to reduce the effect of multipath on range tracking. This is accomplished by having the tracking loop track the entire code rather than the clock tone only. The phase lock loop of the code processor locks onto the clock tone component and the subfrequency correlation process is sequenced. When the phase of the lowest subfrequency has been acquired, the ranging code is reconstructed. The phase lock loop then correlates the total received signal with the reconstructed code so as to suppress the interference due to multipath. The auto-correlation function of the code is shown in Figure B-2. The correlation does not equal zero beyond ±T (where T is the period of the clock, which equals 3.2 usec. in this design). In the clock tone mode, the autocorrelation function of the clock component is a periodic triangular shape so that distant multipath signals (where the relative delay with respect to the signal exceeds the reciprocal of the code bit rate) cannot effect the clock tracking point.

The complete code auto-correlation function has a major correlation peak at zero time displacement and only minor correlation peaks over the remaining code repetition period. Consequently, the effect of multipath signals delayed greater than one code bit time (1.6 usec; 1600 feet) are suppressed by the ratio of major peak to minor peak (approximately 18 dB). This essentially eliminates multipath tracking errors resulting from multipath signals beyond 1600 feet.

The implementation of the code correlator requires the use of an early-late correlation tracking technique to generate a clock loop tracking error signal. The code is reconstructed by the processor and advanced 1/2 clock time "early code" and retarded 1/2 clock time late code. The cross correlations of these codes with the received code are shown in Figure B-2 for a three component code. The early correlation (a) has its peak amplitude 1/2 period leading while the late correlation (b) is 1/2 period lagging behind

the in-phase position. By subtracting the two correlation functions a proper phase discriminator characteristic results, having a null at T = 0 (c). The ganged correlation function G(T) can be written as:

$$G(T) = C(T) \quad XC_E - C(T)\ XC_L \qquad (A)$$

$$= C(T) \quad x(C_E - CL) \qquad (B)$$

implementation of equation (A) requires two multipliers whereas (B) requires only one, but done only with tri level logic. Since B_E and B^L are logic signals and have 1 and 0 states, the subtraction of these two C signals will result in three states. For circuit simplicity the former approach is chosen.

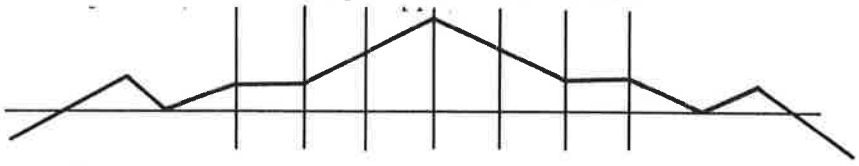

Figure B-1. Auto Correlation of Code

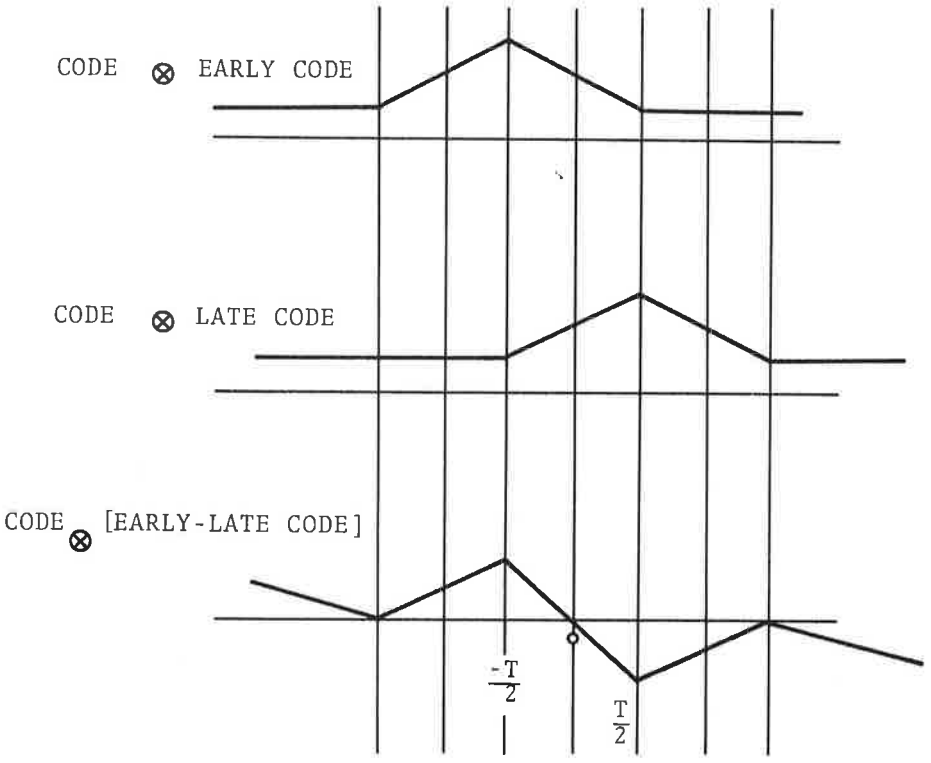

Figure B-2. Cross Correlation of Code

REFERENCES

1. Stiffler, J.J., Block Coding and Synchronization Studies: Rapid Acquisition Sequences, JPL Space Programs Summary 37-42, Vol. IV, p. 191-197, Dec. 1966.

2. TRW, Systems Design Report Binor Code Processor ATS-E L-Band Experiment, NASA-ERC Contract NAS 12-2204, Nov. 1969.