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LETTER REPORT ON A STRAW-MAN MODIFICATION OF AN ATC TRANSPONDER FOR DISCRETE ADDRESS USE

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16. Abstract

An experimental evaluation has been made of an RCA AVQ-65 air-traffic control transponder modified, in Mode D, so as to reply if and only if interrogated with its own preset reply code. Successful operation of the modified transponder was verified, and some key circuit limitations were explored and improved upon.

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PREFACE

This report is concerned with the experimental evaluation of an RCA transponder modified so as to reply, in Mode D, if and only if interrogated with its own preset reply code.

The evaluation consisted of determining the degree of conformance to modification design specifications, such as non-interference with transponder operation in Modes A, B and C and isolation of digitally adjacent discrete address codes. In addition, timing diagrams were developed for the various digital operations to determine the tolerances allowed on interrogation pulse spacing.

The results indicate satisfactory adherence to the design specifications. However, logic timing studies indicate that the spacing tolerances on interrogating pulses in Mode D are greater than can be justified on the basis of the slow logic family used. In addition, the design did not incorporate any circuitry to inhibit narrow noise pulses from being decoded as valid members of an interrogating pulse train. To overcome these problems, certain changes were incorporated into the circuitry and those resulted in the expected improvements.

It is a pleasure to acknowledge the helpful comments, suggestions, and constructive criticism offered by Dr. Bernhard Kulke.

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1. INTRODUCTION

During the latter part of 1971, some work was begun at the Transportation Systems Center (TSC) that was aimed at the development of a discrete address Air-Traffic Control Transponder, in connection with the Discrete-Address Beacon System (DABS) that is being considered as a potential successor to the currently used, non-discrete address radar beacon system (ATCRBS). It was recognized at the time that in the absence of a firm decision on the planned modulation and coding format, any experimental transponder design would be highly conjectural. However, it was felt that measured data from a simple and easily realized modification of an existing device could provide a useful input to the thoroughgoing systems engineering analyses that would be required to produce a final design.

Consequently, a contract was placed with RCA in early 1972 to design and build such a modification for a TSC-owned Model AVQ-65 transponder. This modification was delivered in September 1972. The purpose of this report is to describe the modification, to give data on its performance, and to define problem areas and suggest solutions on the basis of the observed performance. While the scope of the beacon radar effort at TSC has meanwhile been narrowed down towards developing engineering improvements of the existing ATCRBS system, it is hoped that the results of the earlier work presented here will be useful to those working groups that are currently engaged in DABS design.

2. FUNCTIONAL DESCRIPTION OF THE AVQ-65 MODIFICATION

An RCA AVQ-65 Transponder was modified by RCA under contract to TSC, such that in Mode D operation, the transponder will reply if and only if the interrogating code is identical to the preset transponder reply code. The operation of the transponder in Mode A or Mode C remains unaffected, and a reply will be obtained upon selection of either mode when interrogated with the standard code. A summary of the interrogating codes, including the code modification for Mode D operation, is given in Figure 1, and it is seen that Modes A, B, and C have their usual format. More detailed information relative to the interrogate/reply Mode D code formulation is given in Figure 2.

It will be noted that successive pulses are spaced a minimum of 2.9 μsec apart, and this is to prevent triggering of the SLS circuitry that is designed to respond to a 2 μsec pulse spacing. Figure 2 also gives a list of the digit values that are assigned to different combinations of code pulses.

The circuitry for the Mode D modification was mounted on a separate PC board. The interconnection consisted of four wires between the discrete address board and the main transponder control unit, and of seven wires between the discrete address board and the control box. A photograph of the modified transponder and of the discrete address board is shown in Figure 3, and a schematic circuit diagram of the modification is given in Figure 4.

Referring back to Figure 2, the decoding process basically consists of comparing the received pulse train with whatever pulse pattern has been selected at the transponder control head. This decoding process is initiated as follows.

Referring to Figure 4a, the normal decoding circuitry is disabled when Mode D is selected, grounding Pin 9 of Z2(A) and forcing the transponder suppression circuit transistor into saturation. To avoid damage to the transmitting tube the transponder operation is inhibited for one minute after turn-on by

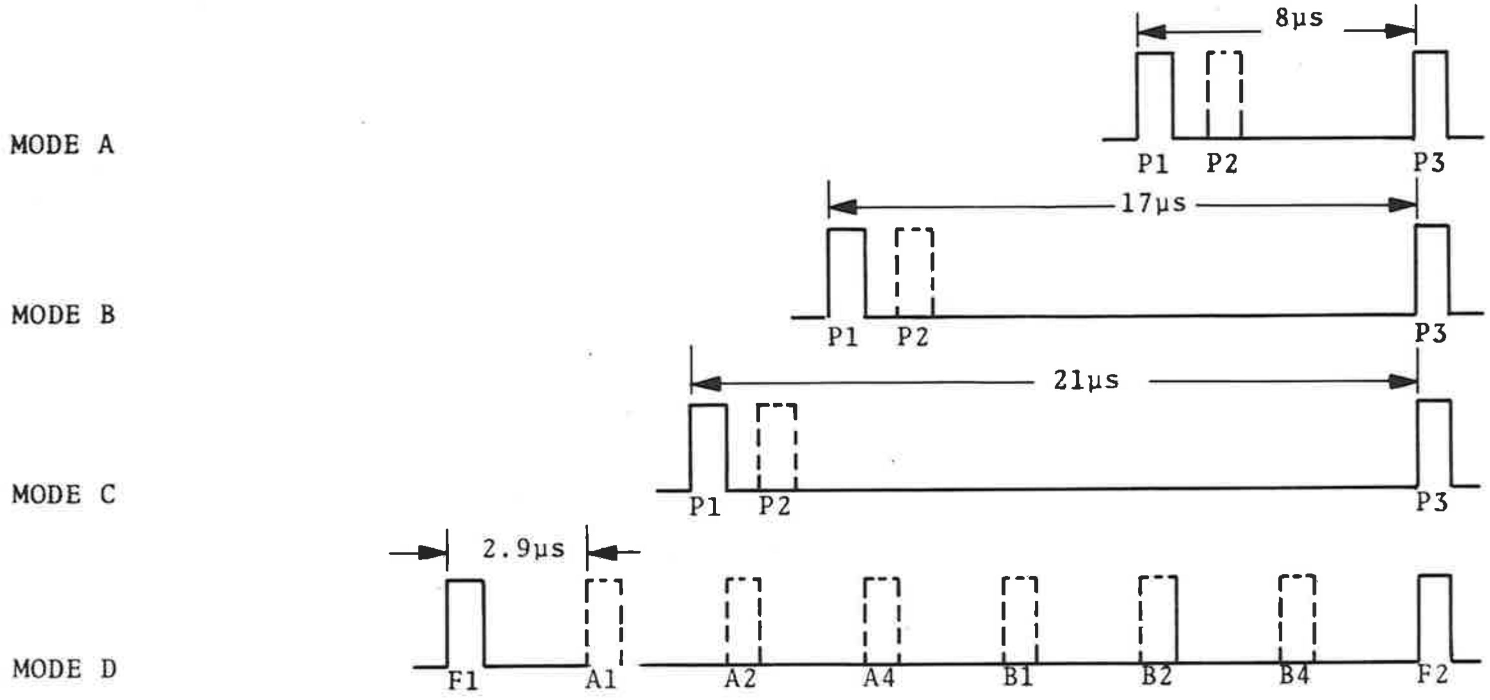
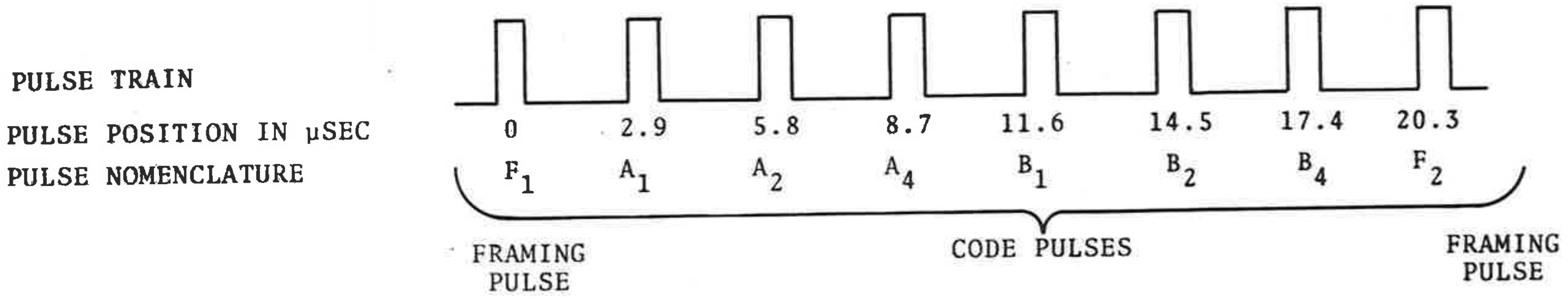


Figure 1. Interrogation Codes Used with the Modified Transponder



CODE TABLE

CODE DIGIT	THOUSANDS	HUNDREDS
0	NONE	NONE
1	A_1	B_1
2	A_2	B_2
3	A_1A_2	B_1B_2
4	A	B_4
5	A_1A_4	B_1B_4
6	A_2A_4	B_2B_4
7	$A_1A_2A_4$	$B_1B_2B_4$

Figure 2. Reply Mode D Code Formulation for Use with the Modified Transponder

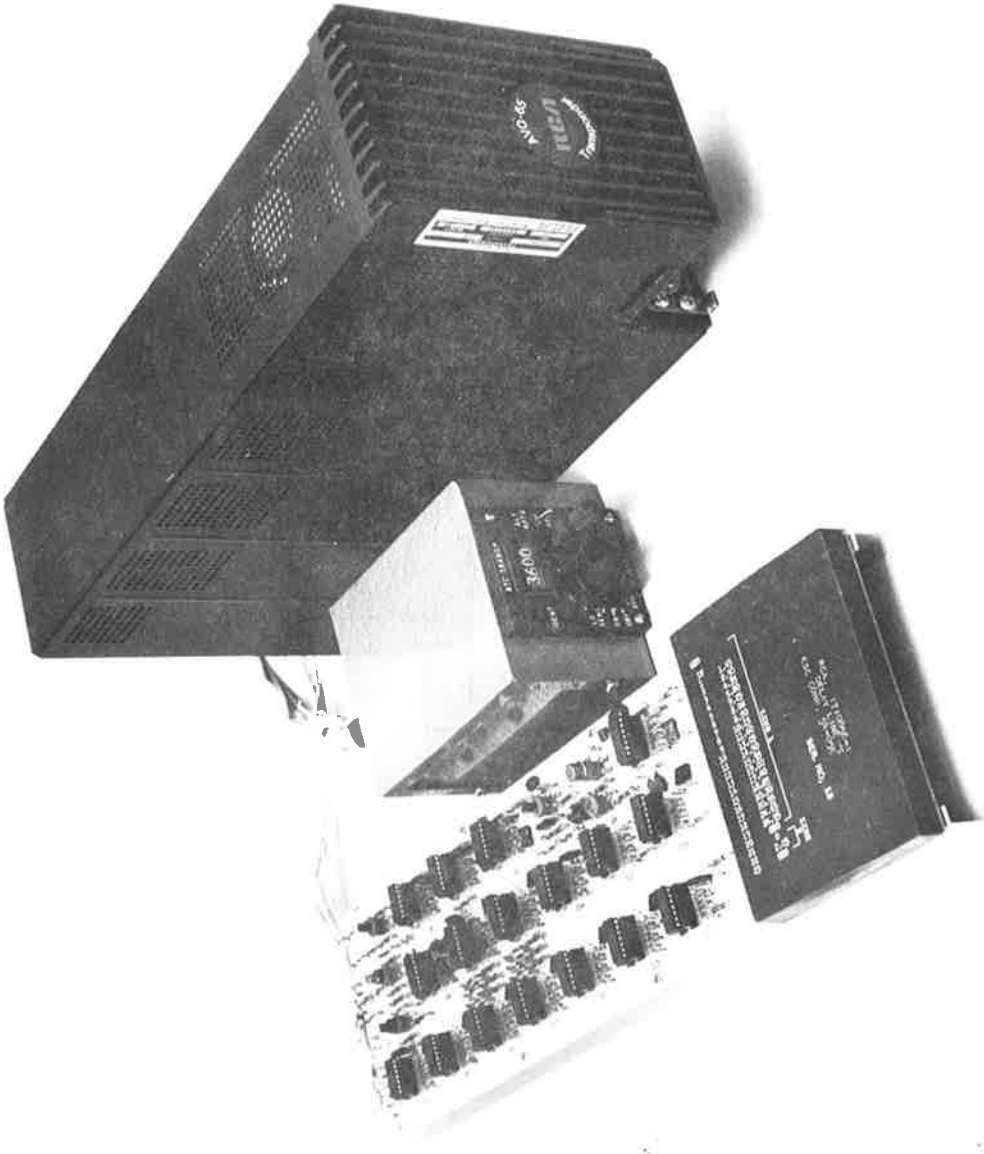


Figure 3. Modified Transponder

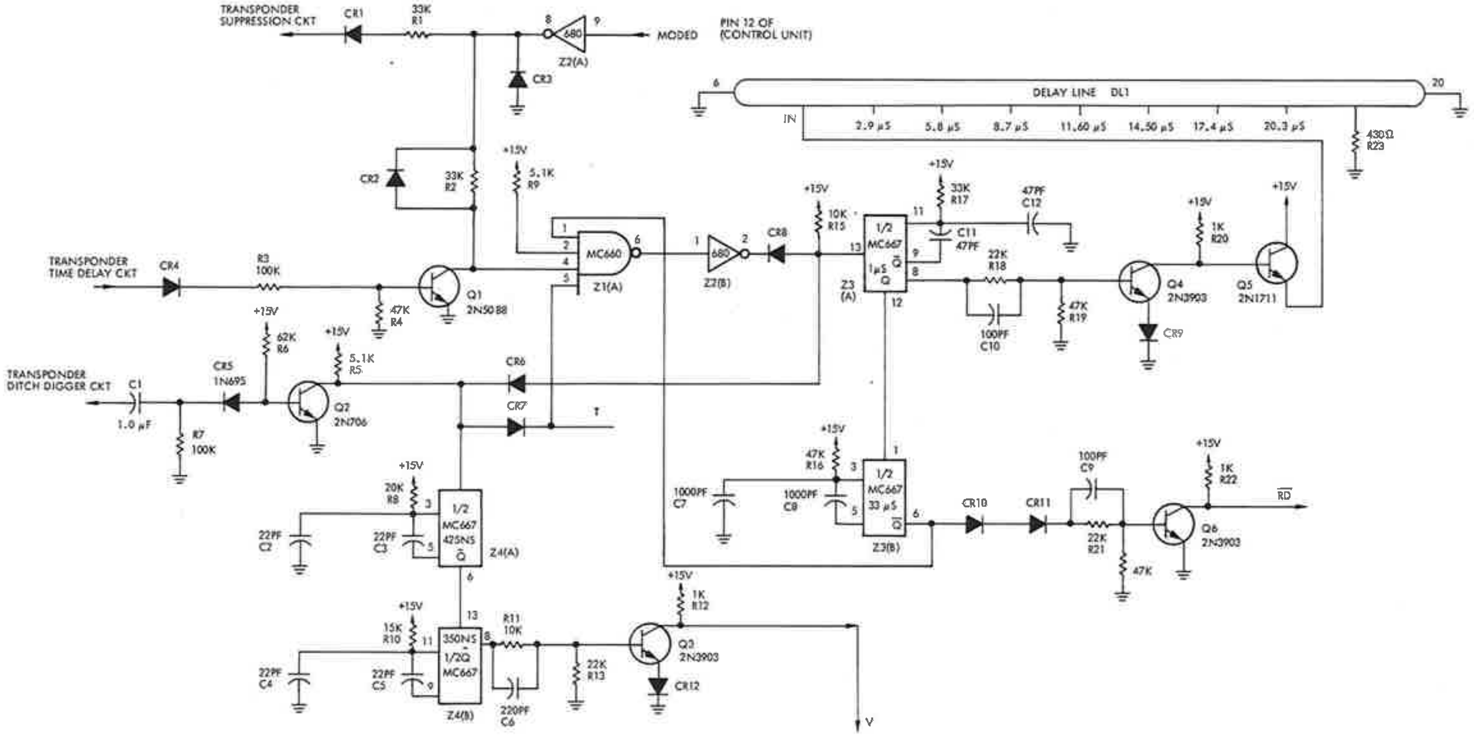


Figure 4a. Initialization Circuit

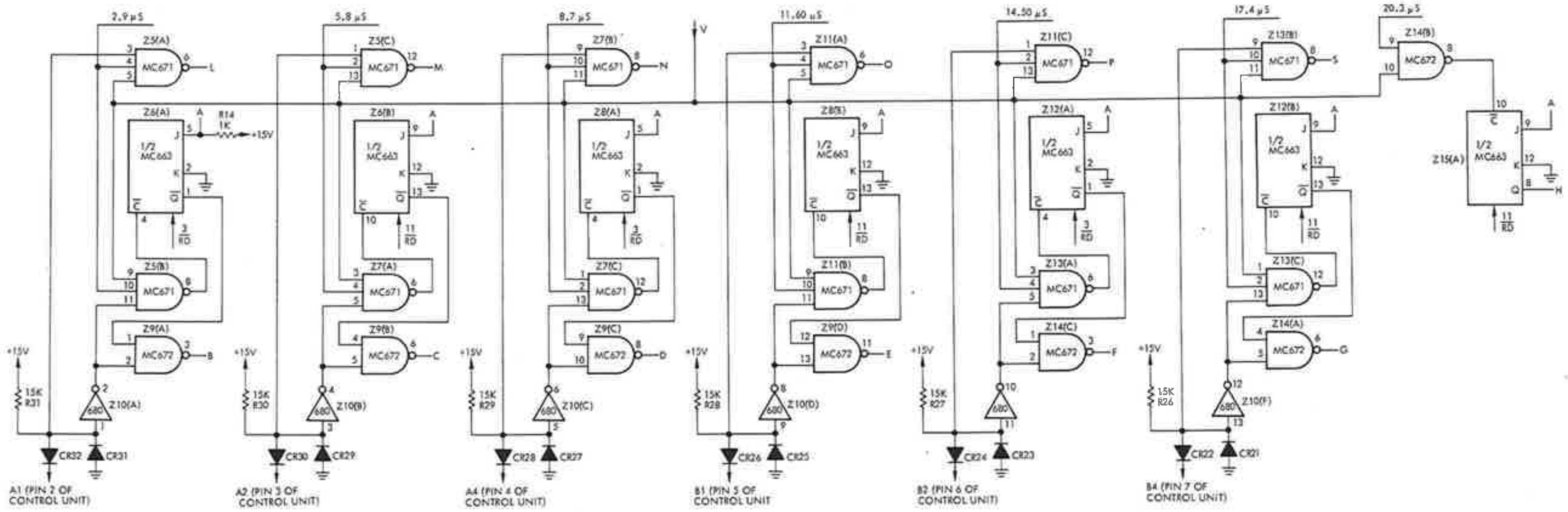


Figure 4b. Coincidence Circuit

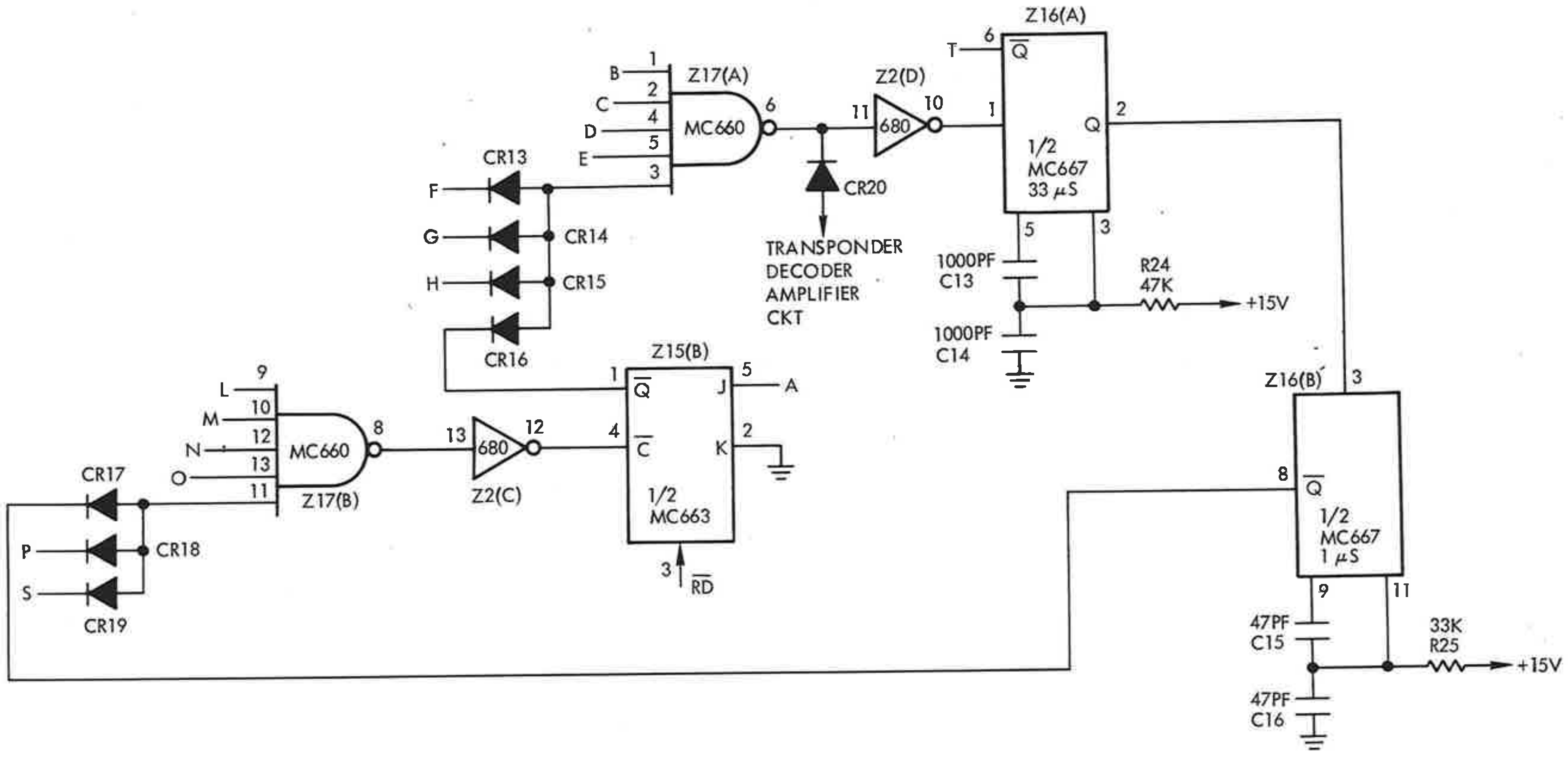


Figure 4c. System Reply and Reset Circuit

saturating Q1 through the transponder time delay transistor and forcing Pin 4 of Z1(A) low.

Only if all inputs to Z1(A) are high does decoding take place. When a pulse is received (generally the F1 framing pulse) of sufficient power, such that Q2 is turned off by the transponder ditch digger circuit, then Pin 1 of Z7(A) goes high generating a 1 μs negative pulse at Pin 8 for input through inverter Q4 and emitter follower Q5 to the delay line. As a result of the pulse appearing at Pin 12 of Z2(A), a 33 μsec pulse is generated by one-shot Z3(B) which through Pin 1 of Z1(A) inhibits further pulses from entering the delay line. When the next pulse arrives at Pin 1 of Z4(A) a 425 nsec system delay pulse is generated at the end of which a 350 nsec wide pulse is developed by one shot Z4(B) which is inverted to +15V at Q3 and applied to Gates Z5(A) and Z5(B). These in turn enable the decoding process which may or may not result in a reply being generated.

For coding, each pulse in the received pulse train is matched with the corresponding position in the preset pattern. Four possible cases arise, and these are illustrated in Table 1.

TABLE 1. TYPICAL OPERATING STATES OF THE MODIFIED TRANSPONDER

Is Pulse A_1 Selected?	Is Pulse A_1 Present?	Reply Enable?
yes	yes	yes
yes	no	no
no	yes	no
no	no	yes

Table 1 holds for all pulse positions. The circuit logic is identical for all pulse positions, so only the logic for pulse position A1 will be analyzed. It should be noted that in the context of individual pulse position analysis, "reply enable" only implies acceptance of the pulse in question. A "system reply enable" is generated later from the combined acceptance signals of all the pulse positions. Figure 4b is a schematic of the coincidence circuitry for all interrogating pulse position.

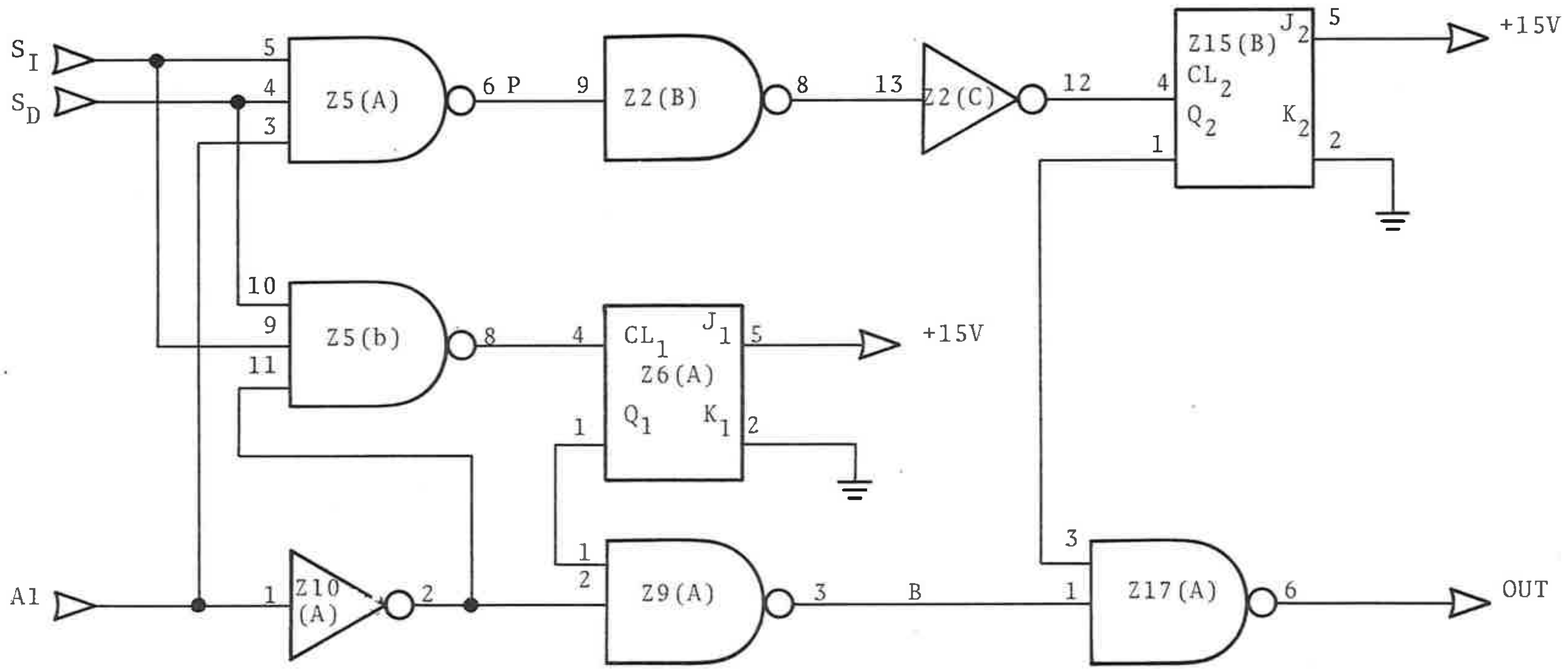
According to Figure 5, which is a schematic of the coincidence circuitry relative to interrogating pulse position A1, the input lines to Gate Z17(A) and Z17(B) must be high for a reply to be generated. As a result, Pin 8 of Z17(B) is low maintaining a high on Pin 3 of Z17(A) through Z2(C) and Z15(B). Pin 6 of Z17(A) goes low triggering the reply circuitry through the transponder decoder amplifier. A low on either input line to Gates Z17(A) and/or Z17(B) inhibits a reply.

If A1 is selected, then Pin 3 of Z5(A) is low and Pin 6 is high, regardless of whether or not a pulse appears at 2.9 µs on Pin 4; however, Pin 11 at Z5(B) and Pin 2 of Z9(A) are high through Z10(A), and Pin 10 is high through the delay line at 2.9 µsec. Therefore, if a pulse is received at 2.9 µs at Pin 9 of Z5(B), Pin 8 goes low, generating a low to Pin 1 of Z9(A) through Flip-Flop Z6(A). As a result, Pin 3 of Z9(A) is high and a reply is thus enabled. On the other hand if no pulse appears at 2.9 µs, the flip-flop Z6(A) is not set, Pin 1 or Z9(A) remains high and the reply is inhibited at Z17(A).

If A1 is not selected, then Pin 2 of Z9(A) is low and Pin 3 is high, regardless of whether or not a pulse appears at 2.9 µs. At Z5(A), however, if a pulse does appear with Pins 3 and 4 high, Pin 6 goes low and the reply is inhibited at Pin 3 of Z17(A) through Z17(B) and Flip-Flop Z15(B). If no pulse arrives at Pin 5 of Z5(A), Pin 6 stays high and a reply is enabled. A summary of gate inputs and outputs leading to a digital reply/no reply decision appears in Figure 6.

This completes the description of the circuit functions that yield Table 1. The truth checks for all individual pulse positions, as illustrated in Table 1, are then combined to enable or inhibit the actual reply generation for the transponder.

It is also necessary to generate appropriate reset pulses to get the system ready for reception of the next pulse train. This is done as follows.

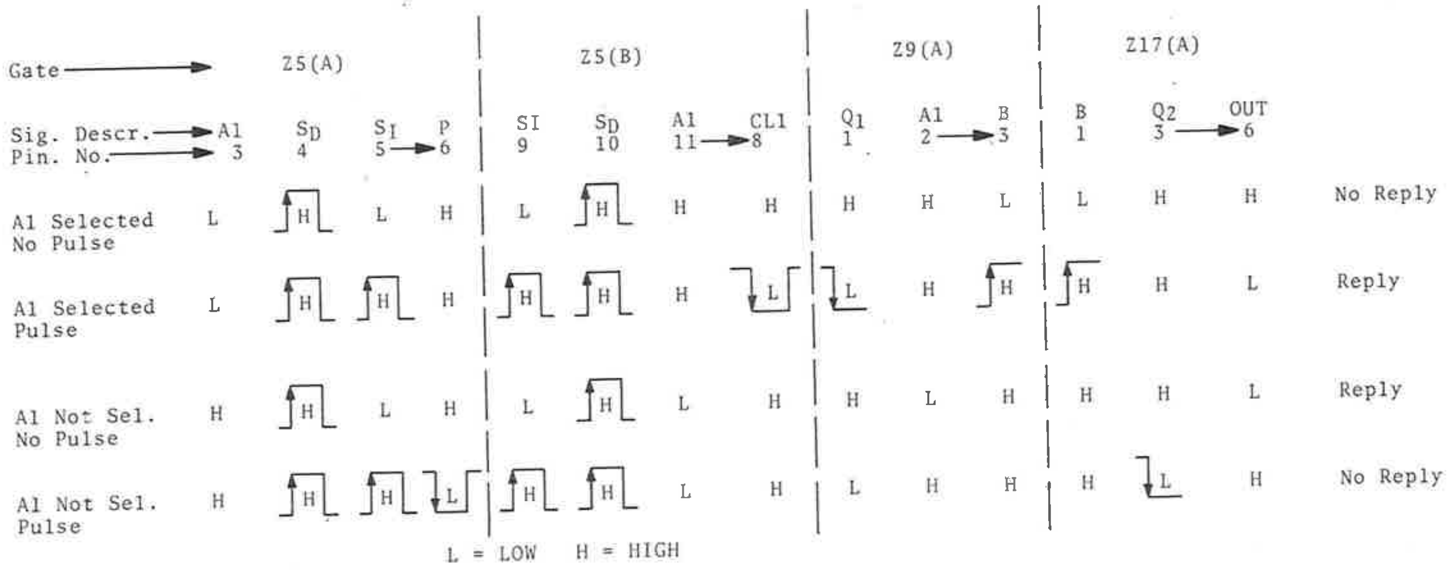


S_I - INCOMING SIGNAL

S_D - DELAY LINE SIGNAL

A1 - PULSE SELECTED - L (LOW)
PULSE NOT SELECTED - H (HIGH)

Figure 5. Condensed Circuit-Interrogate/Reply Code Comparison



Gate →	Z5(A)				Z5(B)				Z9(A)			Z17(A)			
Sig. Descr. → Pin. No. →	A1 3	SD 4	SI 5 →	P 6	SI 9	SD 10	A1 11 →	CL1 8	Q1 1	A1 2 →	B 3	B 1	Q2 3 →	OUT 6	
A1 Selected No Pulse	L	H	L	H	L	H	H	H	H	H	L	L	H	H	No Reply
A1 Selected Pulse	L	H	H	H	H	H	H	L	L	H	H	H	H	L	Reply
A1 Not Sel. No Pulse	H	H	L	H	L	H	L	H	H	L	H	H	H	L	Reply
A1 Not Sel. Pulse	H	H	H	L	H	H	L	H	L	H	H	H	L	H	No Reply

L = LOW H = HIGH

Figure 6. Summary of Digital Reply/No Reply Decision Process

Referring to Figure 4c, Flip-Flop Z16(A) generates a 33 µs pulse when a reply is initiated to inhibit further interrogation pulses during transmission of the coded reply. All Flip/Flops are reset 33 µs after arrival of the F1 framing pulse through Z3(B) and Q6; this gets the system ready for the next cycle. A further remark is in order concerning pulse positions. Given an incoming pulse in the A1 position, it must be remembered that this pulse will appear at the input not only of the A_1 decoding circuit, but simultaneously at the input of all other pulse decoding circuits. This results in four additional possible states of the three variables A1, S_I and S_D (as defined in Figure 5) which deal with the logic of those pulse positions just prior to and those following the position under consideration during one interrogation. The primary characteristic of these states is that the delay line output, S_D, is low indicating no delay line output. Since these states do not change the operating conditions of establishing a valid interrogation they are not considered here in detail.

3. PERFORMANCE EVALUATION MEASUREMENTS AND RESULTS

The operation of the transponder in the discrete-address mode (Mode D) was monitored using the experimental set-up shown in Figure 7. The 1030 MHz signal was modulated by the pulse-train generated by the H.P. 1917A. The H.P. 214A pulse generator was used to provide a gating pulse to obtain a pulse-train repetition frequency of 300. For initial checkout a pulse width of 800 nsec. and a pulse period within the pulse-train of 2.9 μsec were used. For this transponder modification only the six most significant bits of the transponder reply code were used for coding, corresponding to the two most significant digits on the transponder control unit. A scope trace photograph of an interrogation and reply for Code 7700 (bracketed by the two framing pulses) is shown in Figure 8, and for Code 5400 in Figure 9. In each figure the top trace represents the interrogation and the bottom trace represents the generated reply.

As there were 2^{12} possible combinations of interrogation code and transponder control unit setting, but only 2^6 of these would produce a reply, a simple sampling method of checkout was utilized. On the assumption that the most likely combinations to produce an incorrect reply were those for which the interrogating code differed from the preset transponder code by any one bit (all the bits carry the same weight from a circuit point of view), a test was set up for each reply-producing combination whereby the interrogating code was altered by successively adding and then subtracting one bit.

It was found that in all cases when the interrogating code and the transponder control unit code differed, no replies were generated. In addition, beginning with a reply-producing combination of codes and randomly changing the interrogating code by any number of bits, it was found that in all cases where the codes differed, the reply was inhibited. By performing the same tests, but varying the transponder control unit code while keeping the interrogating code fixed, the same results were obtained.

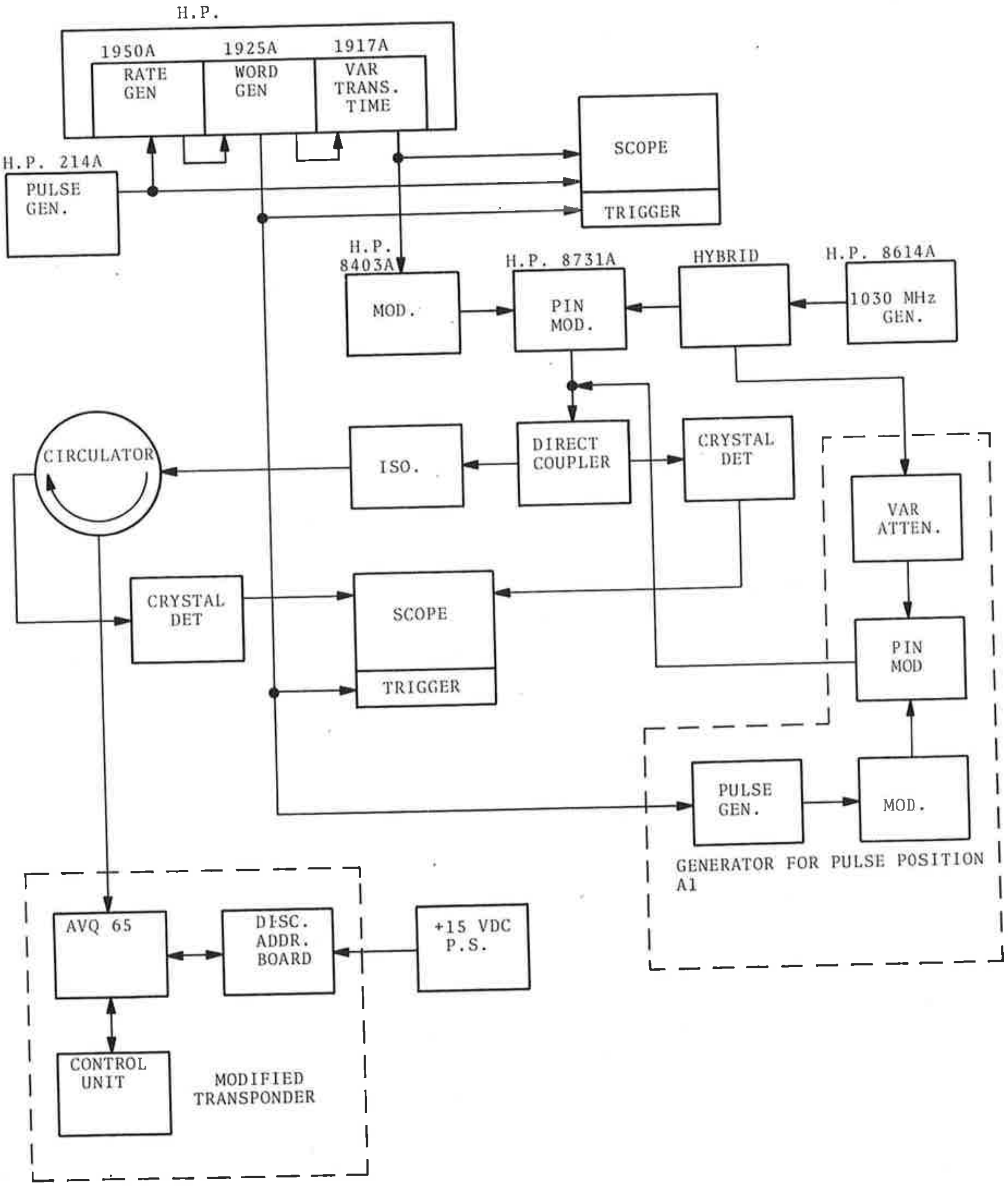


Figure 7. Test Set-Up for Evaluating Transponder Performance

5. SUGGESTED ALTERNATIVE CIRCUITS

The solution to the two problem areas, discussed above requires careful consideration of overall system timing. One possible design alternative, perhaps the simplest, is to shorten the pulse width of the delay line input pulse as generated by one-shot Z3(A). This was done, and as it turned out, replacing R17(33K) with a 10K resistor resulted in an output pulse of approximately 450 nsec wide sufficient to drive the one-shot output circuitry. Any attempt to further narrow the drive pulse by reducing R17 rendered the circuit inoperative. By referring to Figure 11 it can be seen that this change does improve the interrogating pulse-timing tolerance but only to the extent of reducing the latest possible arrival time (L_{PA}) to 2.80 μsec. A more effective change is represented by the circuit shown in Figure 12. As can be seen, in order to improve the earliest possible arrival time, E_{PA}, it is necessary to alter the method of pulse processing as accomplished by Z4(A) and Z4(B).

Thus, one-shot Z4(A) is removed and replaced by a 300 nsec delay-line, a gate Z1(B), and an inverter Z2(E). An interrogating pulse is applied to the delay-line and one input of the NAND gate. At the end of the delay period the output of Z1(B) goes low triggering Z4(B) through the inverter Z2(E). Pulses less than 300 nanoseconds wide (noise spikes) are therefore filtered out. It should also be noted that the Q output of Flip/Flop Z16(A) has been routed to Pin 10 of Z1(B) in order to accommodate the additional circuitry and still perform its function of inhibiting interrogations during transponder transmission, using the same analysis as that used for Figure 11. A new tolerance range of 2.9 ± 0.45 μsec on the position of A1 was calculated, as shown in Figure 13. Finally, Figure 14 shows the measured pulse position tolerance after incorporating the changes shown in Figure 12. Clearly, the measured and the calculated results are in close agreement, and thus a significant improvement of the pulse position tolerance has been achieved. Attempts at still further improvement ran into

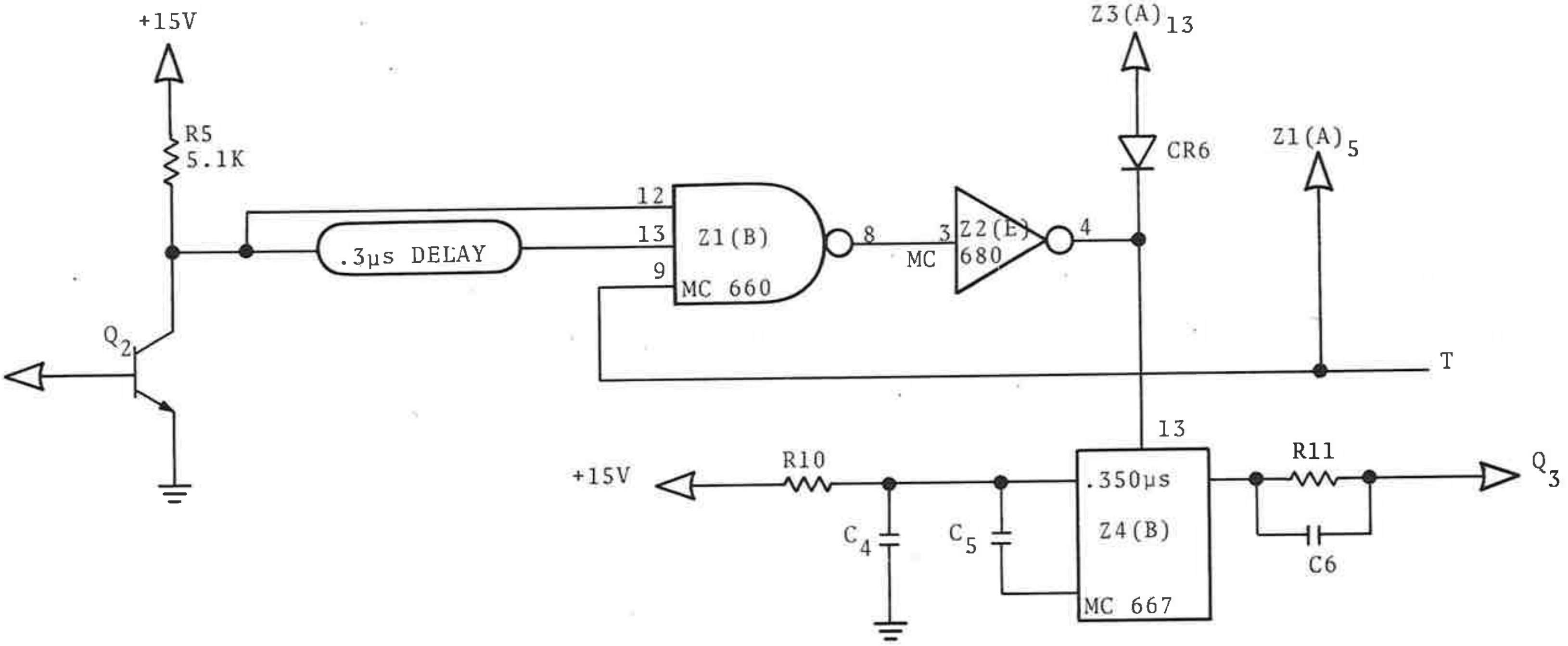
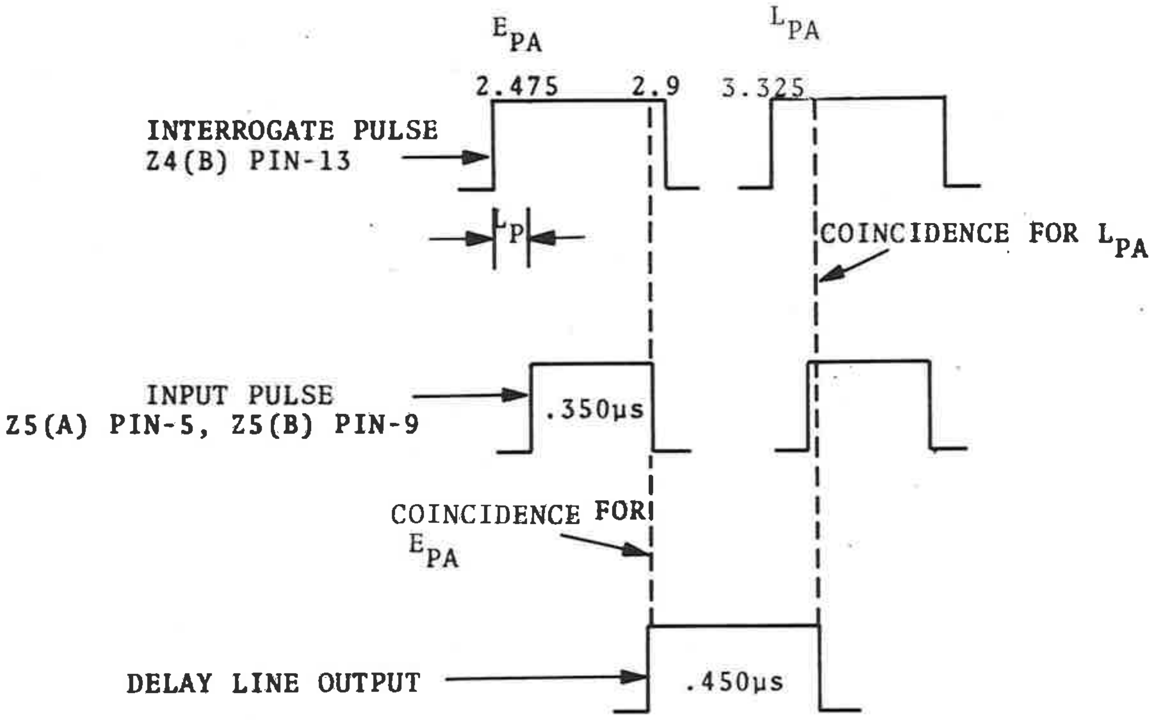


Figure 12. A Circuit Modification to Improve Noise Immunity and Pulse Period Tolerance



E_{PA} - EARLIEST POSSIBLE ARRIVAL FOR VALID INTERROGATION PULSE

L_{PA} - LATEST POSSIBLE ARRIVAL FOR VALID INTERROGATION PULSE

L_P - LOGIC PROPAGATION TIME $(2\ L_P = .125\ \mu SEC)$

Figure 13. Expected Pulse Period Tolerance Improvement as a Result of Suggested Circuit Modifications

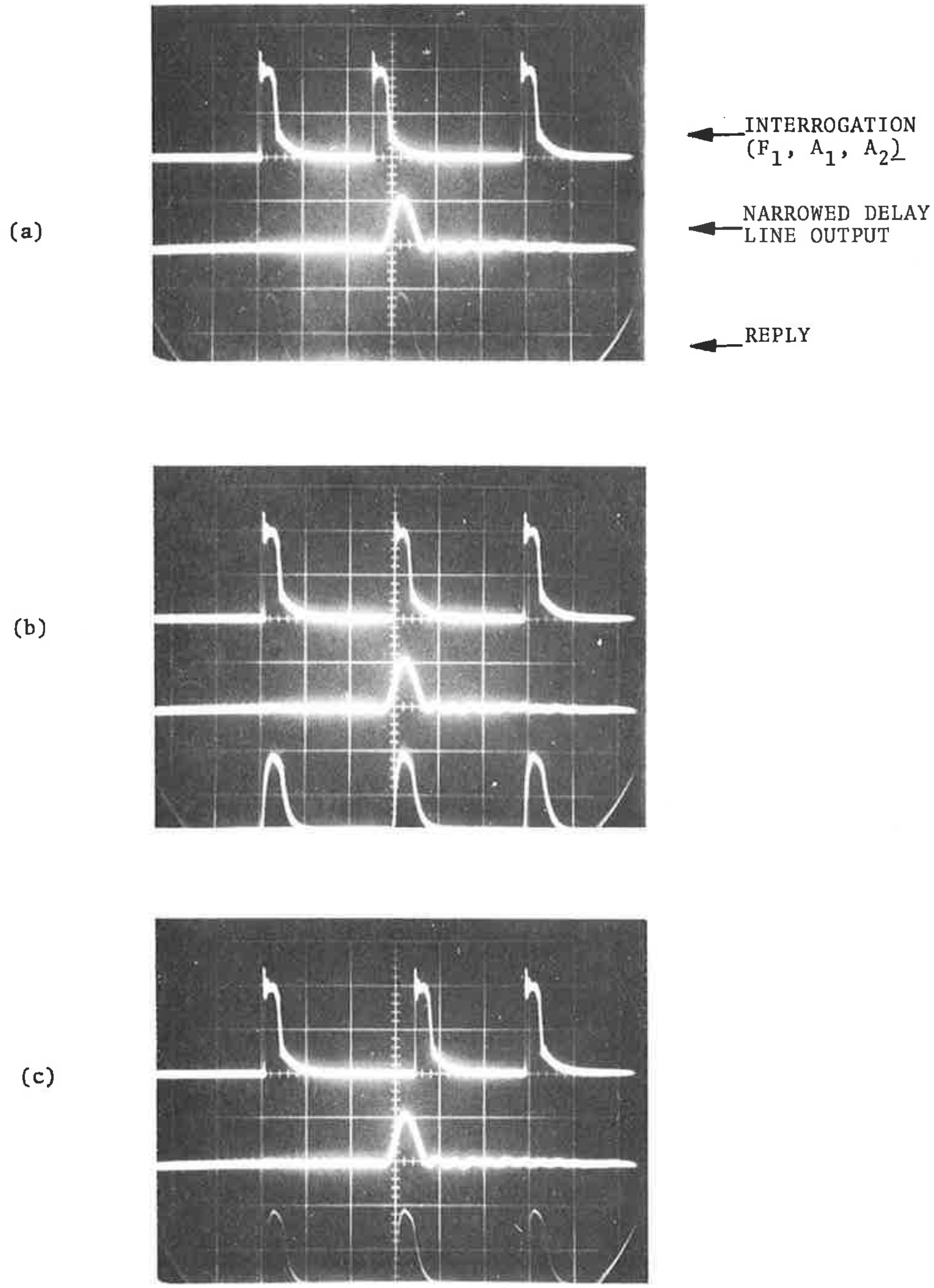


Figure 14. Measurement of Improved Circuit Pulse Period Tolerance (Sweep 1 μs/cm)

difficulties because of synchronization problems having to do with the basic pulse propagation delays inherent both in the original transponder and the modification circuit. Although the circuit components of Figure 12 might need to be chosen with different values in order to accommodate a different transponder unit, because of component tolerances, the basic circuit approach deserves to be looked at for incorporation in future models.

6. CONCLUSIONS

A straw-man modification of an RCA Type AVQ-65 transponder was carried out, with the purpose of adding a discrete-address reply mode to the already existing Mode 3/A and Mode C reply capabilities. In the discrete-address mode, the transponder will reply if and only if it receives an interrogation pulse train that duplicates its own identity code. The modification was designed and implemented on contract by RCA, and it was tested at TSC. The unit was found to operate successfully in the desired mode.

Two modifications have been suggested in this report that would improve the operating characteristics within the context of the present design. These should not be construed to be a criticism, as this transponder modification is a straw-man design and therefore serves only as a starting point for further study. Both the coding, and the logic design selected for use in this unit are quite arbitrary.

It is hoped that the test data presented here will be useful to other groups active in the field of ATC radar beacon systems.