FAA-74-8

REPORT NO. FAA-RD-74-151

MULTIPATH CHANNEL SIMULATION
AND
MODEM EVALUATION PROGRAM

Christopher B. Duncombe

AUGUST 1974
INTERIM REPORT

1. Report No. FAA-RD-74-151	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle MULTIPATH CHANNEL SIMULATION AND MODEM EVALUATION PROGRAM		5. Report Date August 1974
		6. Performing Organization Code
7. Author's) Christopher B. Duncombe		8. Performing Organization Report No. DOT-TSC-FAA-74-8
9. Performing Organization Name and Address U.S. Department of Transportation Transportation Systems Center Kendall Square Cambridge MA 02142		10. Work Unit No. (TRAIS) FA-411/R4107
		11. Contract or Grant No.
12. Sponsoring Agency Name and Address U.S. Department of Transportation Federal Aviation Administration Systems Research and Development Office Washington DC 20591		13. Type of Report and Period Covered Interim Report Oct. 1973 - Apr. 1974
		14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

The Department of Transportation, Transportation Systems Center has developed a laboratory communications test facility. This facility, at present, is in support of DOT aeronautical satellite system (AEROSAT) developments and the associated implementation and evaluation of ground and airborne communications equipment. The facility has broad application to other DOT communications development interests. The facility is available to utilize at DOT/TSC, by interested parties. The purpose of the facility is to evaluate in a laboratory controlled simulated environment, alternative modulation techniques having potential application in aeronautical and maritime satellite communications and surveillance systems. The facility offers the advantage of a "quick-check" of candidate modem performance. It may also be used as a substitute for extensive costly field experiments particularly where typical field conditions are of interest. The main feature of the communication test facility is the hardware for simulating, by means of laboratory equipment, the narrowband (50 KHz) AEROSAT satellite-to-aircraft propagation channel. The simulator also simulates the maritime satellite-to ship propagation channel and is expandable to wideband (10 MHz) systems; e.g., future CONUS ATC Systems. The simulator includes provisions for duplicating multipath phenomena over the satellite links and includes provisions for adjustment and programming of channel parameters covering a wide range of environmental conditions. The features of the channel simulator and the test bed set up are described in detail in this interim report. Subsequent reports will present measured performance data obtained from extensive laboratory modem tests utilizing this facility.

17. Key Words Multipath, Simulator, Modem, Bandwidth	18. Distribution Statement DOCUMENT IS AVAILABLE TO THE PUBLIC THROUGH THE NATIONAL TECHNICAL INFORMATION SERVICE, SPRINGFIELD, VIRGINIA 22151.

19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No. of Pages 70	22. Price

Form DOT F 1700.7 (8-72)   Reproduction of completed page authorized

PREFACE

Many systems for aeronautical and maritime communication via satellite are being built. Thus, DOT/TSC has established a modem evaluation facility which rates a modem's performance in the aeronautical and maritime communication link including the multipath component. Each candidate modem will be evaluated according to the procedures of this report.

CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

The Department of Transportation/Transportation Systems Center (DOT/TSC) has assembled a simulator and test capability for evaluating various candidate modulation techniques having potential application in aeronautical and maritime satellite systems. The TSC facility provides a direct method of determining modem characteristics over a laboratory created satellite to aircraft "channel". The laboratory "channel" simulates the fading multipath channel encountered in aircraft to satellite L-band links. The system was established at TSC primarily for the evaluation of modems for use in the DOT aeronautical Oceanic Satellite ATC system, AEROSAT, plus the potential application of satellites in future CONUS ATC and maritime systems. Specifically, it will serve to assist in preparation of AEROSAT system and avionics specifications. The services of the facility are also offered to organizations interested in evaluating other modulation techniques.

The channel being simulated is a satellite to aircraft L-band link. The signal received at the aircraft can be expected to be perturbed by multipath of varying bandwidths, amplitudes, and time delays, along with doppler and relative doppler frequency shifts, all added with background noise appearing as white gaussian additive receiver front end noise.

In general, candidate modulations for voice, data, and ranging (surveillance) modems will be evaluated. Each will be subjected to the multipath environment of an AEROSAT system as created by the simulator and evaluated accordingly.

2. PURPOSE

In contemplation of aeronautical and maritime systems via satellite, many new avionics and maritime electronic systems have been suggested. Electronic equipment in the aircraft will be subjected to varying amounts of interference; i.e., multipath, additive receiver noise, and doppler shifts due to velocity differentials between the aircraft, satellite, and ground. Thus, the performance of each candidate system must be carefully evaluated under many different conditions in order to facilitate trade off analyses and arrive at decisions necessary to prepare system specifications. TSC has therefore, developed a modem (modulator-demodulator) evaluation program which will evaluate each proposed communication technique for voice, data, or ranging transmission. With data also collected from field experiments as a basis for comparing with laboratory generated data, the modem evaluation-channel simulation system may be directly validated.

As new modems are proposed and/or introduced the costly and time consuming process of field evaluation can be supplemented by the inexpensive process of laboratory evaluation.

3. MODEM EVALUATION

3.1 DATA

A criterion for data modem evaluation is bit error rate for a prescribed signal to noise power density ratio C/No and signal to multipath ratio S/M. See Figure 1 for test block diagram. In addition, acquisition performance and burst error characteristics are very important.

A data rate is generated consisting of a particular pseudo-noise pattern. It is modulated onto the carrier and sent to the multipath simulator where multipath and additive noise are added to the signal. The signal reaches the demodulator, is demodulated, and the output data is compared with the reference data for errors. From these data, a curve of probability of error versus signal to noise ratio is plotted.

The test generator is the International Data Sciences Inc., test generator, model 520. The test set is designed to facilitate the testing of both synchronous and asynchronous modems and digital transmission systems. When externally timed for synchronous applications, data rates of up to 500 KHz are possible. For asynchronous operation timing is internally generated providing data rates of 75, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, and 9600 bits per second. The test set generates six data patterns, three of which are pseudo-noise sequences required to establish system performance and three of which are levels and level inversions required to determine bias distortion. The test generator also has the ability to force errors for further system analysis.

The amplifier Al is used to present a respectable signal level to mixer Ml in the event that the demodulator requires other than a 70 MHz input. The bandpass filter eliminates the unwanted mixer product and provides the necessary gain for the demodulator front end.

The test set, which functions as the bit receiver and error counter, is the International Data Services Inc., model 1200 modem
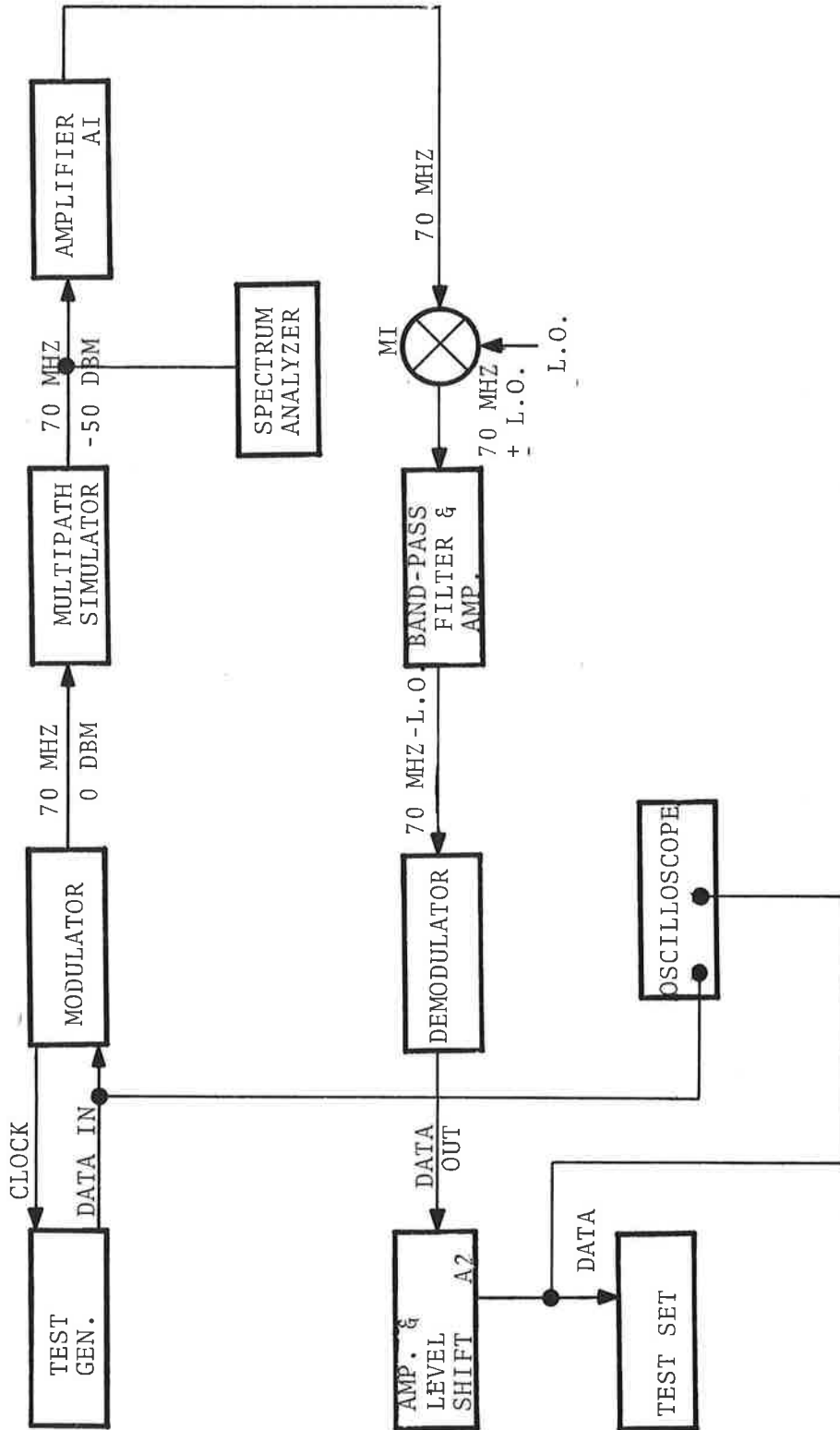
Figure 1. Block Diagram, Data Modem Evaluation

test set. The test set generates a pure replica of the pseudo-noise pattern generated by the test generator. Upon receipt of a pattern from the demodulator the test set synchronizes the locally generated pattern with the received pattern and commences a bit by bit comparison. The error counter is then incremented by one each time an error is detected and fed to a digital readout to give a cumulative count. An external clock is used in conjunction with the test set to establish the bit error rate.

3.2   VOICE

The criterion for voice modem evaluation will be intelligibility for a given value of C/No (carrier to noise density ratio in dB-Hz). A magnetic tape recorder will be used to play tapes consisting of lists of phonetically balanced (PB) word lists. These voice signals will be modulated onto the modem carrier and transmitted to the multipath simulator (the simulator operation is discussed under the multipath simulator section of this report). The modulated voice signal plus multipath and additive noise is returned to the demodulator where the signal is demodulated and recorded on the output tape recorder. The tapes are then processed to establish intelligibility. The equipment used here is of the high performance laboratory type. See Figure 2 for test block diagram.

The input and output tape recorders are Crown model 824, 2 channel 4 track, low distortion machines. They are solid state modular units that offer self-contained minicomputer control. The multipath simulator will add varying combinations of multipath signals, relative delays, and additive noise. The signal to noise meter is used to accurately record S/N and requires a 10 MHz input, thus the mixer M1 at 60 MHz. The amplifier A1 is used to increase the signal to the S/N meter to the required -20 to +10 dBm level. The 70 MHz signal is demodulated and the demodulated signal recorded onthe output tape recorder. The tapes are then listened to by trained listeners. The main objective of the performance of the intelligibility tests is to obtain a measure of the percentage of intelligibility afforded by the system; that is, a ratio of the number of word items correctly interpreted divided by the number of word items transmitted for any given test condition.
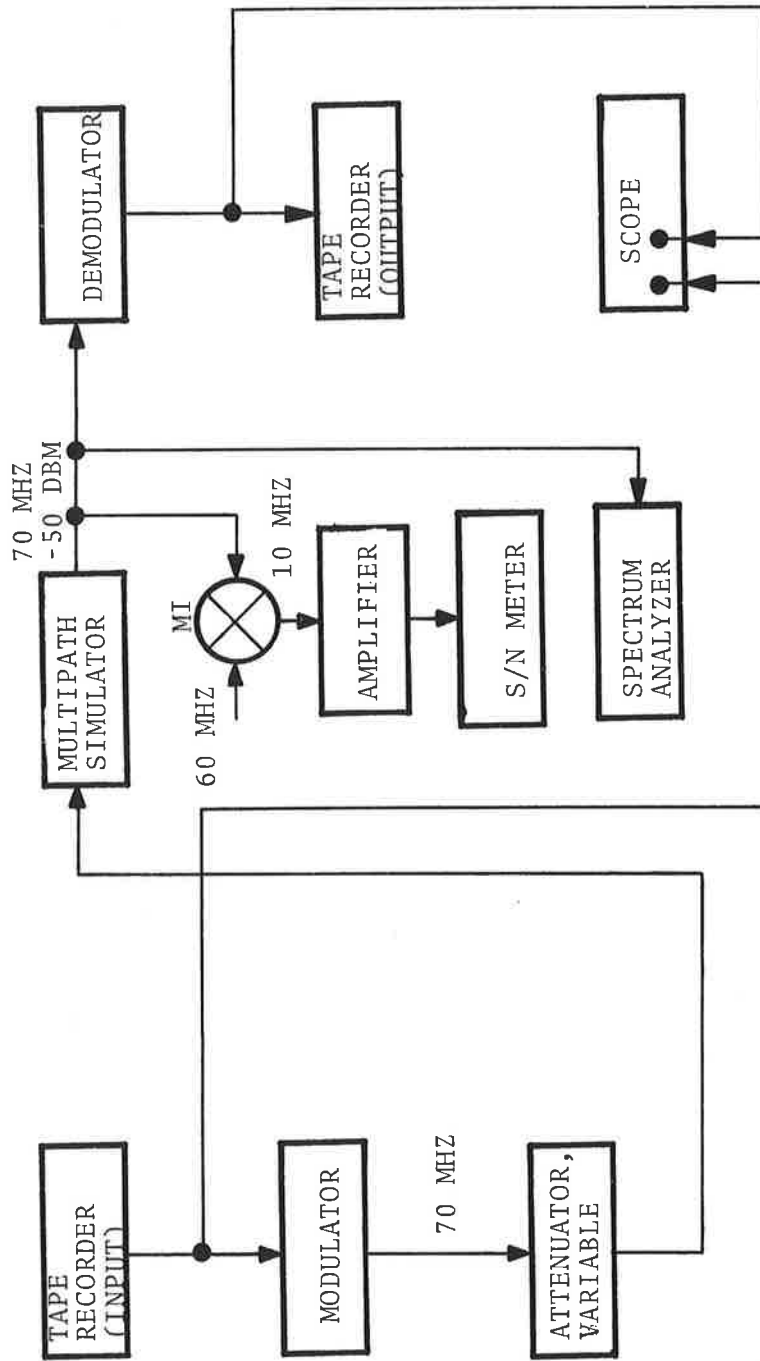
Figure 2. Block Diagram, Voice Modem Evaluation

6

3.3 RANGING

Testing of ranging modems requires determination of accuracies in range and range rate, as well as ambiguity resolution, as a function of C/No. The multipath simulator will be used to determine ranging performance in the fading airborne environment and to establish whether there exist major design defects which would cause problems in the airborne testing phase.

The first major consideration for evaluation of ranging modems is gross error, that is, a ranging measurement in error by more than 3 usec. This implies a gross malfunction. By using the simulator with its fixed delays of 5, 30, and 55 usec., range measurements of 5 ±3, 30 ±3, and 55 ±3 usec., should be obtained. The second criterion of evaluation is ranging accuracy. As C/No decreases phase jitter increases leading to ranging error. Thus phase jitter as a function of C/No will be established. The multipath simulator will produce the fading channel characteristics with its doppler, relative doppler, and multipath profile. See Figure 3 for block diagram.
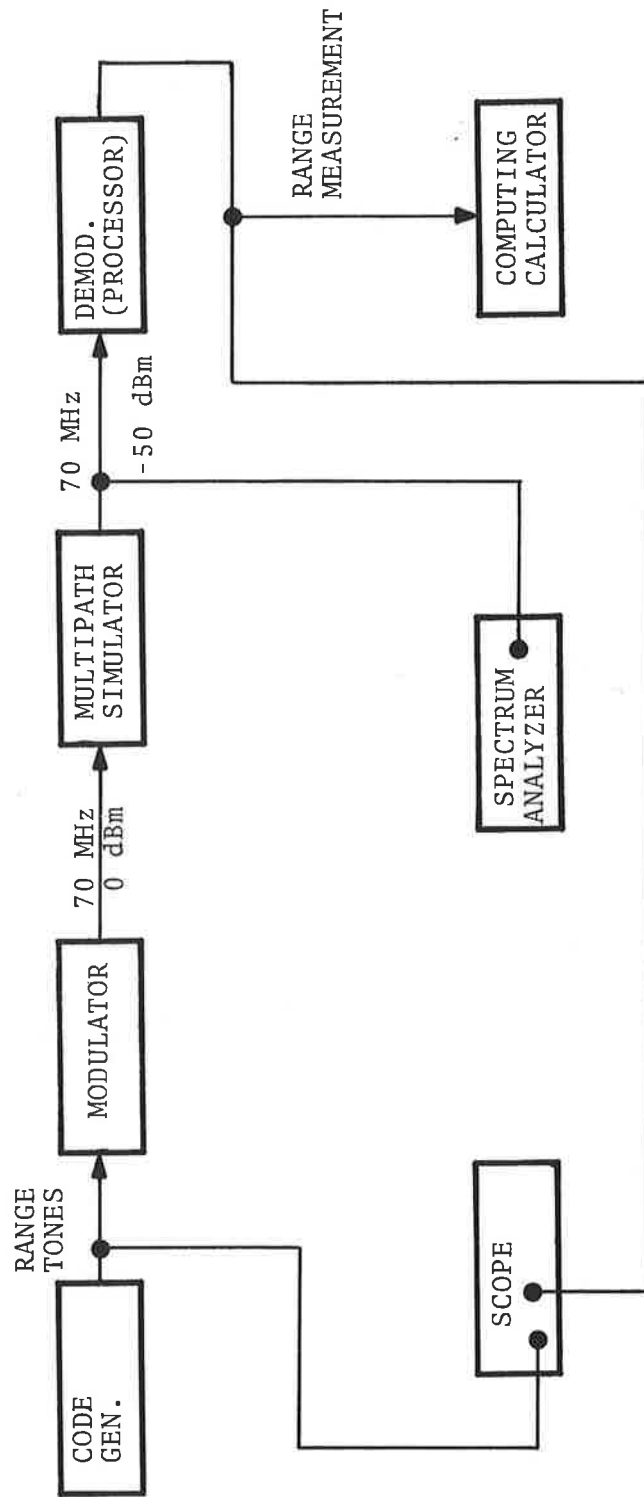
Figure 3. Block Diagram, Ranging Modem Evaluation

4. MULTIPATH SIMULATOR

The multipath simulator (See Figure 4) simulates multipath effects typical of the reflection characteristics and link geometries encountered in satellite to aircraft L-band radio links. (See Figure 5). A photograph of the multipath simulator is shown in Figure 6. The simulator generates a complex output signal composed of a direct signal and a multipath return. The multipath scattered return is approximated by a group of five noise modulated diffuse signals having a delay spread of 8 usec., and a selectable group delay of 5, 30, or 55 usec. Each of the five multipath scattered signals have statistically independent phase and amplitude variations. The diffuse characteristics are varied by independently controlling the rms bandwidths of the multipath signals as well as the rms level of the signals. Doppler frequency offsets can also be generated. These include both the frequency offset due to the relative motion between satellite and aircraft which appears on both the direct path and multipath, commonly called just "doppler", and the frequency offset on the multipath only, resulting from vertical motions and earth curvature effects, commonly called "relative doppler".

The simulator also generates white gaussian noise to simulate the additive noise effects of a receiver front end and received background noise. The signal to additive noise (S/N) as well as the direct signal to multipath signal (S/M) are both completely adjustable. The noise voltages which are used to cause the amplitude and phase fluctuation of the multipath signals and the additive noise are generated digitally. Thus they can be stopped at any time, "frozen", or can be reset to a known starting point for totally reproducible channel simulation. The simulator can handle the 400 kHZ AEROSAT channel, and with minor modification will be able to handle the 10 mHZ channel. A detailed description of the simulator appears as the Appendix.
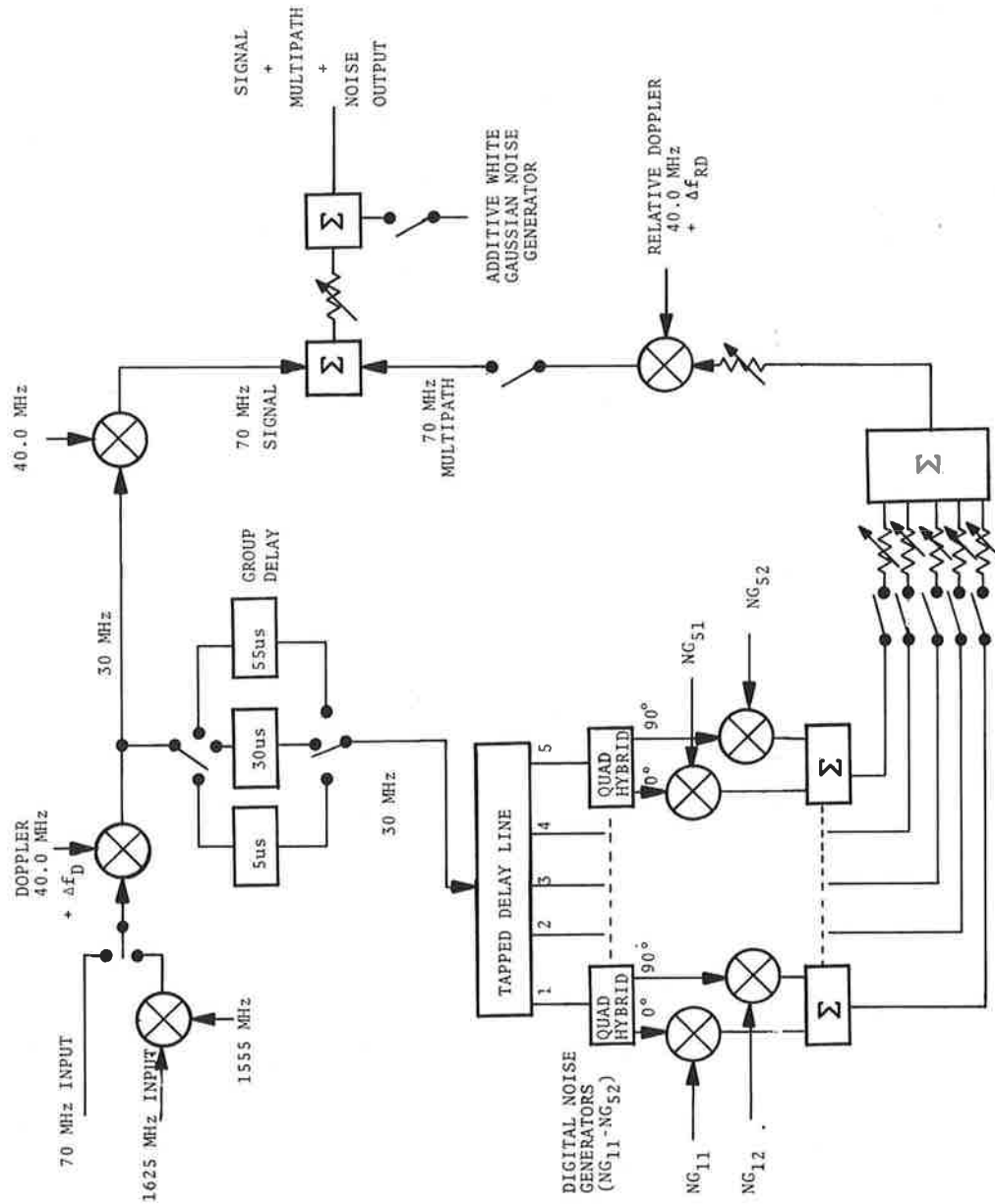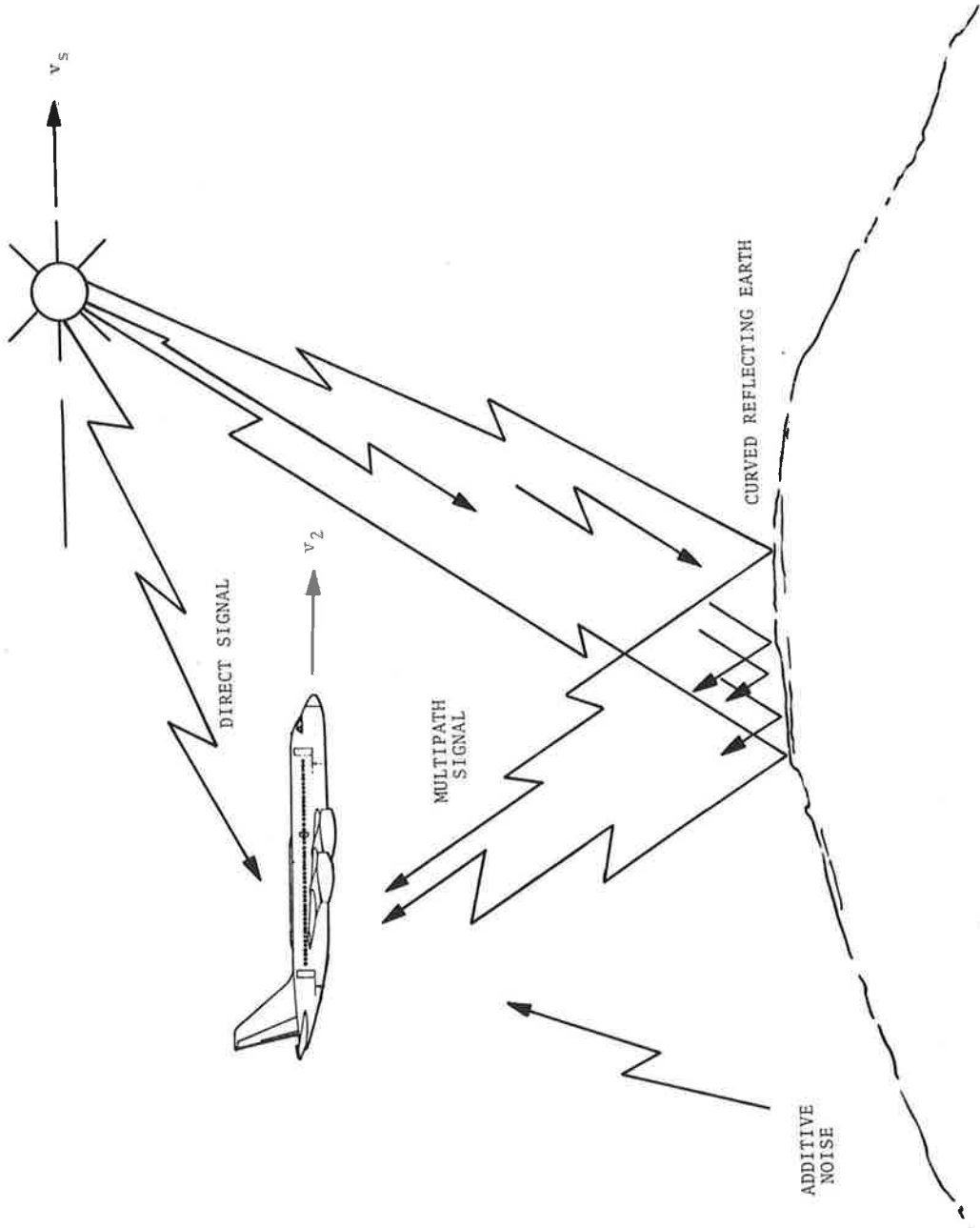
Figure 4. Multipath Simulator Block Diagram

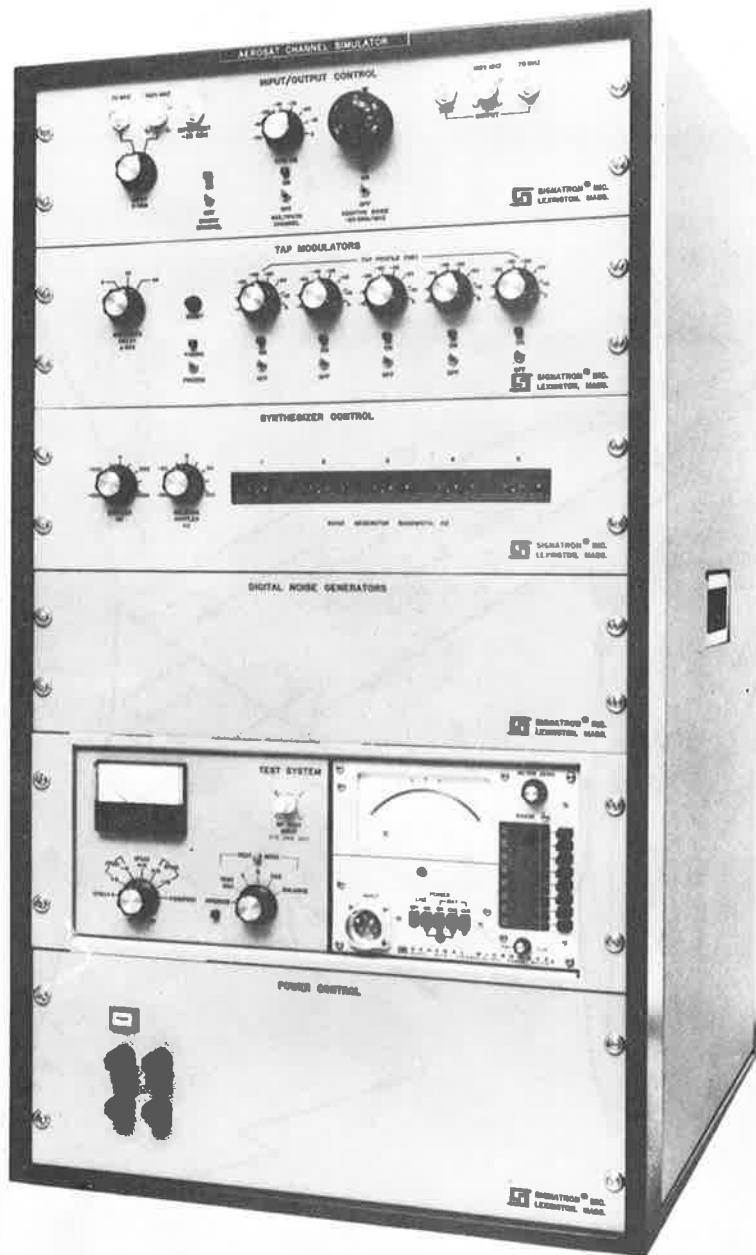Figure 5. Aerosat Communication Channel Geometry

Figure 6. Multipath Simulator

12

5. MODEM EVALUATION PROCEDURE

In order to evaluate all potential modulation candidates, TSC offers to provide a service test facility. The results of these tests will be made available to the public by TSC, and moreover, the results may be incorporated into specification of other associated equipment to be utilized in the overall system. In providing this service modems to be evaluated by DOT/TSC's modem evaluation facility should be received at TSC in good working condition. Manuals should be supplied by the manufacturer detailing operation of equipment. Information concerning input-output signals must be clearly specified as to frequency range, power range, type of modulation, and impedance. This applies to RF signals and modulating signals on both the input and output. Also, clearly available should be any and all alignment procedures necessary to afford peak performance of the modem. Alignment should be performed by manufacturer prior to reception at TSC, and manufacturer should state if any alignment is necessary after reception. It is also recommended that if at all possible, a suitable representative of the manufacturer be present on the first day of modem evaluation to insure that any modem idiosyncrasies are not overlooked.

Any equipment requiring unique or special connectors or cabling must come with these items as the modem evaluation facility obviously can not cater to individual specialized non-standard hardware. The modem evaluation facility does have a complete line of standard cabling, connectors, and instrumentation. Specialized equipment necessary for pretest alignment must be supplied with the modem along with detailed schematics as to modem interface with alignment equipment. Any questions concerning specialized equipment or non-standard hardware for purposes of TSC's modem evaluation facility should be directed to the facility before shipment of the modem.

6. TEST PLAN

Modems will be evaluated according to the dictates of the previous section. All modems will be subjected to the multipath environment previously discussed. Of primary interest are carrier to noise density ratios of approximately 33 dB-Hz to 45 dB-Hz, depending on the individual modem, signal to multipath ratios of 5 dB, 8 dB, and 11 dB, multipath bandwidths of 10, 100, 300, and 1000 Hz, relative doppler shift of 30 Hz, doppler shift of 500 Hz, and delay times of 5 usec., and 55 usec. Thus, the following multipath tests for modem evaluation (each test consisting of values of C/No from acquisition to approximately 10 dB above acquisition):

TEST	S/M(DB)	BW(HZ) MUL	DOP (HZ)	REL DOP (HZ)	T_D(USEC.)
1-4	5	10-1000	0	0	5
5-8	8	10-1000	0	0	5
9-12	11	10-1000	0	0	5
13	5	100	+500	30	5
14	8	100	+500	30	5
15	11	100	+500	30	5
16	5	100	-500	-30	5
17	8	100	-500	-30	5
18	11	100	-500	-30	5
19	5	100	+500	30	55
20	8	100	+500	30	55
21	11	100	+500	30	55

14

APPENDIX*

CIRCUIT DESCRIPTION

(Section 5 only)

A-1

SECTION 5

CIRCUIT DESCRIPTION

5.1 Input/Output Interface

The Input/Output Interface subsystem, illustrated in Drawing 0011-1-001, provides the following functions:

1. Input signal source selection (L band, 70 MHz, 70 MHz test oscillator),

2. L band input down-conversion and L band output up-conversion,

3. Multipath delay selection (5 μsec, 30 μsec, 55 μsec),

4. Doppler and Relative Doppler frequency offset generation,

5. Signal preconditioning for tap modulators, and

6. Signal, multipath, and additive noise combining' and power ratio control.

A front panel input signal selector is used to select either the 70 MHz or L band (1625 MHz) signal input. The 70 MHz test oscillator input is controlled by circuits in the input/output interface chassis but is selected from the Test System front panel. The composit Signal (Direct Signal plus Multipath) -to-Noise power ratio (S/N) and the Direct Signal-to-Multipath power ratio (S/M) are front panel controlled using attenuators. As illustrated in Drawing 0011-0-000, the additive Noise Signal, the Direct Channel, and the Multipath Channel each may be turned off for system calibration and testing. All signal selection, steering, and on/off control is performed by DC controlled solid state switches.

Both 70 MHz and L band outputs are simultaneously available. Also, input and output test points are provided to facilitate system setup, alignment, and continuous monitoring during operation.
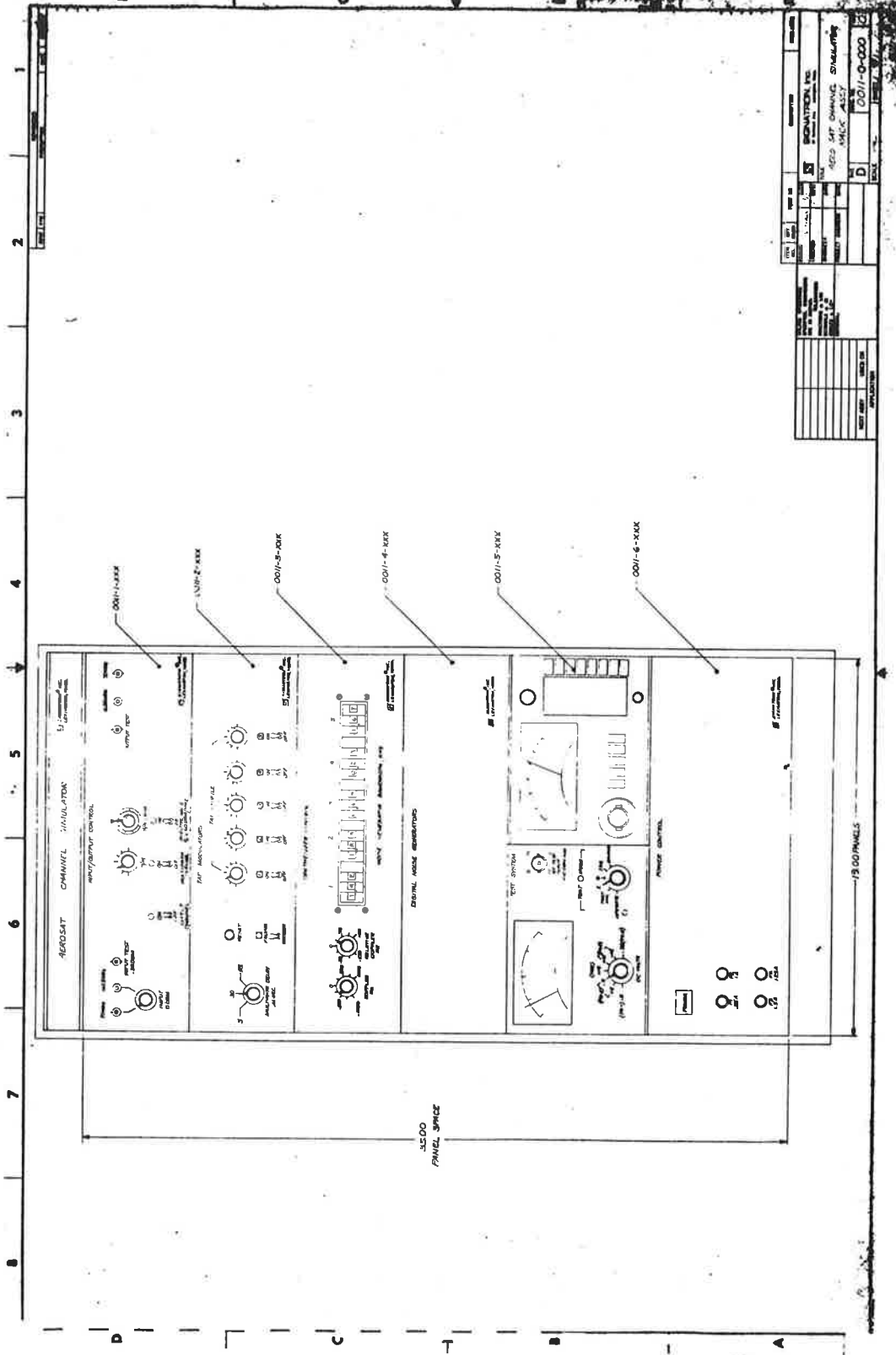
The operation of signal processing modules and circuits which comprise the Input/Output Interface subsystem are described in more detail in the following sections.

5.1.1 Input Selector Module No. 0011-1-010

Drawing No. 0011-1-011 is the schematic of the Input Selector. The Input Selector is used to select one of three possible signal sources:

1) the L band input at 1625 MHz,
2) the 70 MHz input,
or 3) the internal 70 MHz calibration and test oscillator.

The switching required to choose one of the three input signals is performed in a PIN diode switching matrix. All ports of the switching network are at 50Ω regardless of the state of the switch. The state of the PIN switch is determined by +5V (on), and -5V (off) levels appearing on switch control lines IS1, IS2, and IS3. For instance, if IS3 is +5V and IS1 and IS2 are -5V, the selected input will be the 70 MHz internal test oscillator.

The two direct 70 MHz inputs at J_2 and J_3 are attenuated to -13 dBm before appearing at the module output, J_4. The input at J_1, which is the converted L band input is at -27 dBm and is amplified by a wideband hybrid amplifier A_1. When selected, the signal at J_1 also appears at a -13 dBm level at the module output, J_4. The 70 MHz converted L band signal at J_1 is also low pass filtered in the Input Selector Module to attenuate possible spurious signals produced in the L Band-to-70 MHz conversion. All circuitry is constructed on a printed circuit using stripline techniques.
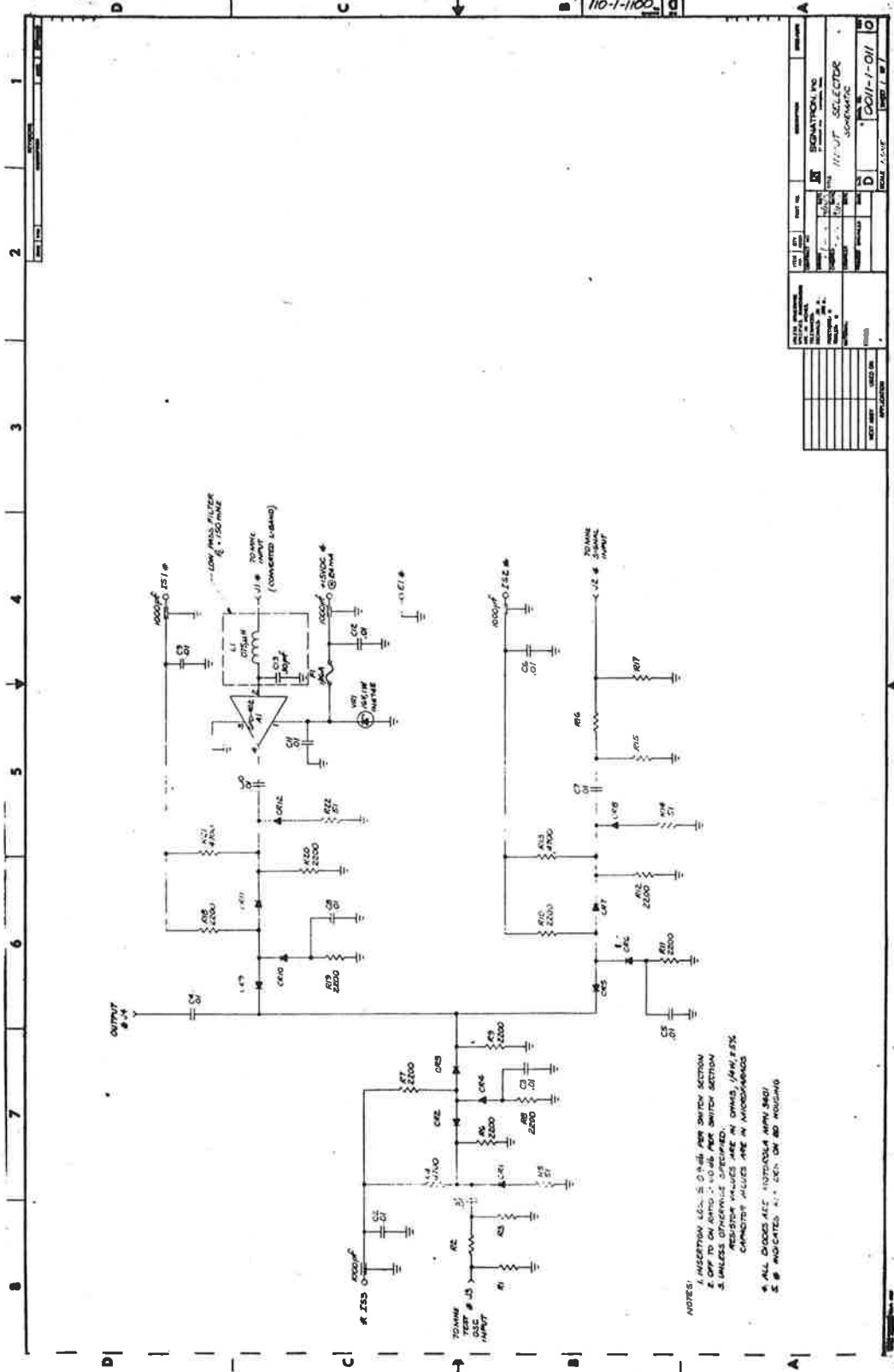
NOTES:
1. INSERTION LOSS: 0.5 dB PER SWITCH SECTION
2. OFF TO ON RATIO: 40 dB PER SWITCH SECTION
3. UNLESS OTHERWISE SPECIFIED;
   RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
   CAPACITOR VALUES ARE IN MICROFARADS

4. ALL DIODES ARE MOTOROLA MPN 3401
5. ⊕ INDICATES +5V ZEN OR BD HOLDING

5-4

5.1.2 Input Mixer-Amplifier Module No. 0011-1-012

Input Mixer-Amplifier Module, shown schematically in Drawing No. 0011-1-013, is used to split the input signals into a direct channel and a multipath channel and to introduce the ±1000 Hz Doppler frequency offset on both the direct and multipath signals.

The signal input at J_1 first passes through a 10 dB directional coupler. The coupled output provides the signal at the front panel INPUT TEST jack. The INPUT Test signal is suitably attenuated so that a zero dB signal at the S-140 simulator input will produce a -30 dBm signal at the INPUT TEST jack.

After the directional coupler the signal is down converted to 30 MHz.

The ±1000 Hz Doppler shift is generated in this down conversion from 70 MHz to 30 MHz by using an oven stabilized 40 MHz VCXO signal as a local oscillator. To produce the required ±1000 Hz Doppler offset the VCXO is adjusted to ±1000 Hz using a control located on the Synthesizer front panel. A 6 dB level adjusting pad and a third harmonic trap are used at the local oscillator input port of the mixer.

After down conversion, the signal is amplified in a wideband hybrid circuit amplifier and then filtered in a three pole Butterworth bandpass filter to remove spurious mixer products. The filtered 30 MHz signal is next split into three equal amplitude signals in a three-way power divider (TO-HJ-303H). These three 30 MHz signals are the output signals from the Input Mixer-Amplifier Module which appear at J_4, J_5, and J_6. The three output signals are identical except for level; J_4 and J_5 are

at approximately -12 dBm while the signal going to J_6 is first amplified to +9 dBm by two wideband hybrid amplifiers. The three output signals are used to develop the direct and delayed multi-path signals as described later.

Fuse F_1 and Zener diodes VR_1, VR_2, and VR_3 are used as over voltage protection in case excessive voltage is applied to the module.

The entire circuit illustrated in Drawing No. 0011-1-011 is mounted on a stripline printed circuit board.

5.1.3 Delay Line, 25 Microseconds

The 25 μsecond delay line is a quartz bulk effect delay line with a 1 dB bandwidth of 10 MHz centered on 30 MHz. Input and output impedances are 50 Ω with VSWR less than 2:1. Due to poor coupling efficiency at the input and output ports, an insertion loss of 53 dB is experienced in this device. In order to maintain signals at desirable processing levels the delay line is driven at a relatively high +9 dBm and followed by a high gain buffer-amplifier.

5.1.4 Buffer Amplifier Module No. 0011-1-014

Drawing No. 0011-1-015 is the schematic for the Buffer Amplifier module No. 0011-1-014 (serial #6). The purpose of this amplifier is to raise the low level 25 μsec delay line output (-44 dBm) to -12dBm to match the level of the J_4 and J_5 outputs of the Mixer-Amplifier, module 0011-1-012.

Three wideband hybrid circuit amplifiers, A_1, A_2 and A_3 provide more than the required 31 dB gain. The excess gain is
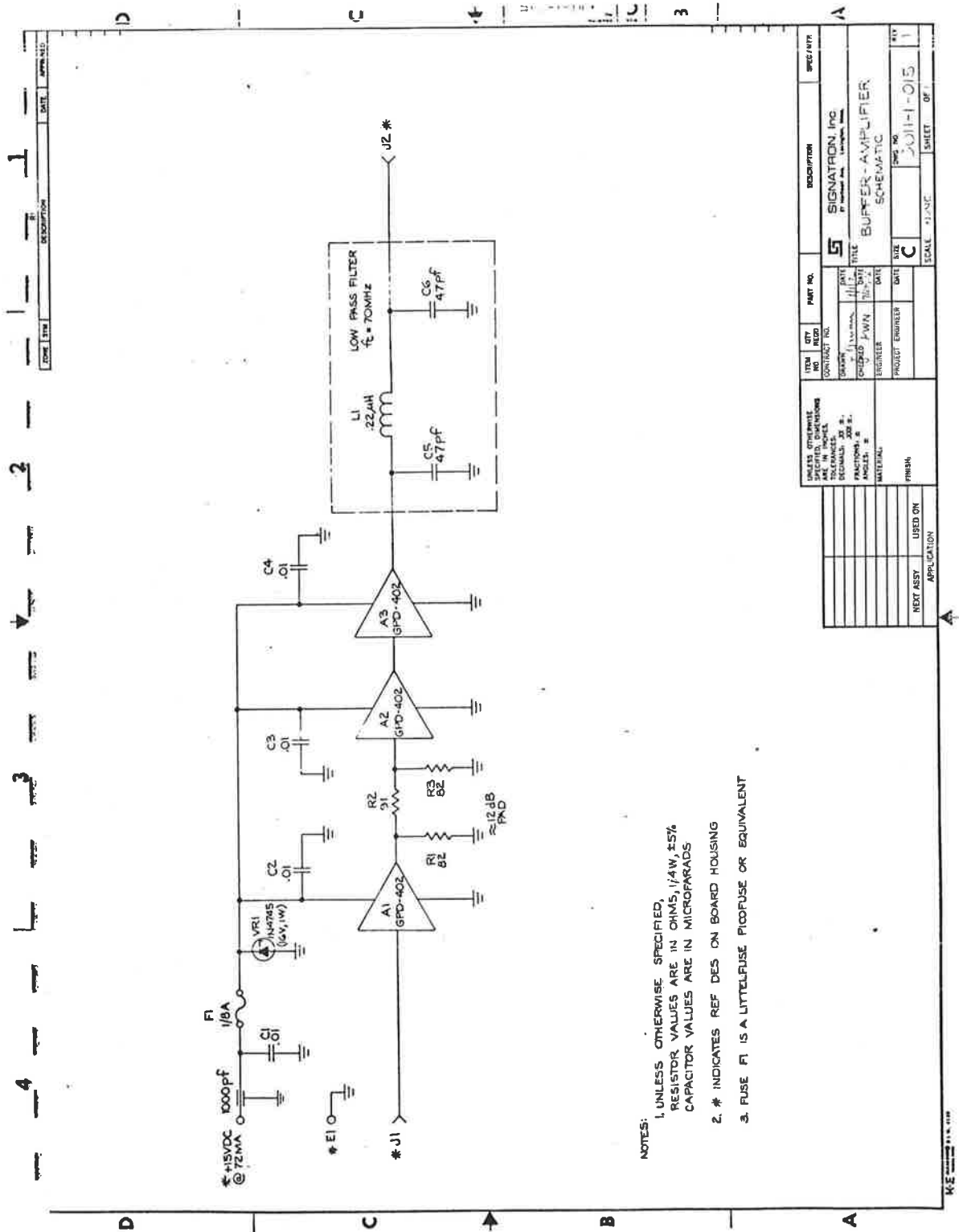
BUFFER-AMPLIFIER SCHEMATIC

LOW PASS FILTER
$f_c = 70\text{MHz}$

NOTES:

1. UNLESS OTHERWISE SPECIFIED,
   RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
   CAPACITOR VALUES ARE IN MICROFARADS

2. * INDICATES REF DES ON BOARD HOUSING

3. FUSE F1 IS A LITTELFUSE PICOFUSE OR EQUIVALENT

SIGNATRON, Inc.

BUFFER-AMPLIFIER SCHEMATIC

5-8

reduced using the 12 dB interstage pad between A_1 and A_2. The pad also serves to suppress instabilities due to the series connection of three high gain wide bandwidth RF amplifiers.

A 70 MHz cutoff lowpass filter is used to suppress the third harmonic of the signal which is unavoidably generated in the Buffer Amplifier. If unattenuated, the third harmonic of the 30 MHz signal would cause undesirable spurious signals in subsequent circuits of the Channel Simulator.

Fuse F_1 and Zener diode VR_1 provide over voltage protection in case excessive supply voltages are applied to the module. All circuitry is mounted on a stripline printed circuit board.

5.1.5 Multipath Delay Selector Module No. 0011-1-001

The Multipath Delay Selector combines signals from the three outputs of the Input Mixer-Amplifier (the output from J_6 being delayed 25 μsec and amplified by module 0011-1-014) to produce the selectable Direct Signal-to-Multipath channel gross delay separations of 5, 30, and 55 μseconds. These delay separations are developed as follows. The multipath channel has a built-in fixed delay of 30 μseconds. Referring to Drawing 0011-1-001, if the Multipath Delay Switch Selector Sw_2 connects the direct channel output J_4 to input J_1 and switch Sw_3 connects the multipath channel output J_5 to input J_2, the direct channel-to-multipath channel relative delay will be 30 μseconds, i.e., the built-in delay of the multipath channel. If Sw_2 connects J_4 to J_3, and Sw_3 connects J_2 and J_5, 25 μsec delay will be inserted into the direct channel which results in a 5 μsec direct signal channel-to multipath channel delay difference. Finally, if Sw_3 connects J_3 to J_5, and Sw_2 connects

J_4 and J_2 the total delay in the multipath channel will be 55 μseconds (25 + 30 μseconds) and no delay will be in the direct channel. This will result in a direct channel-to-multipath channel delay difference of 55 μseconds.
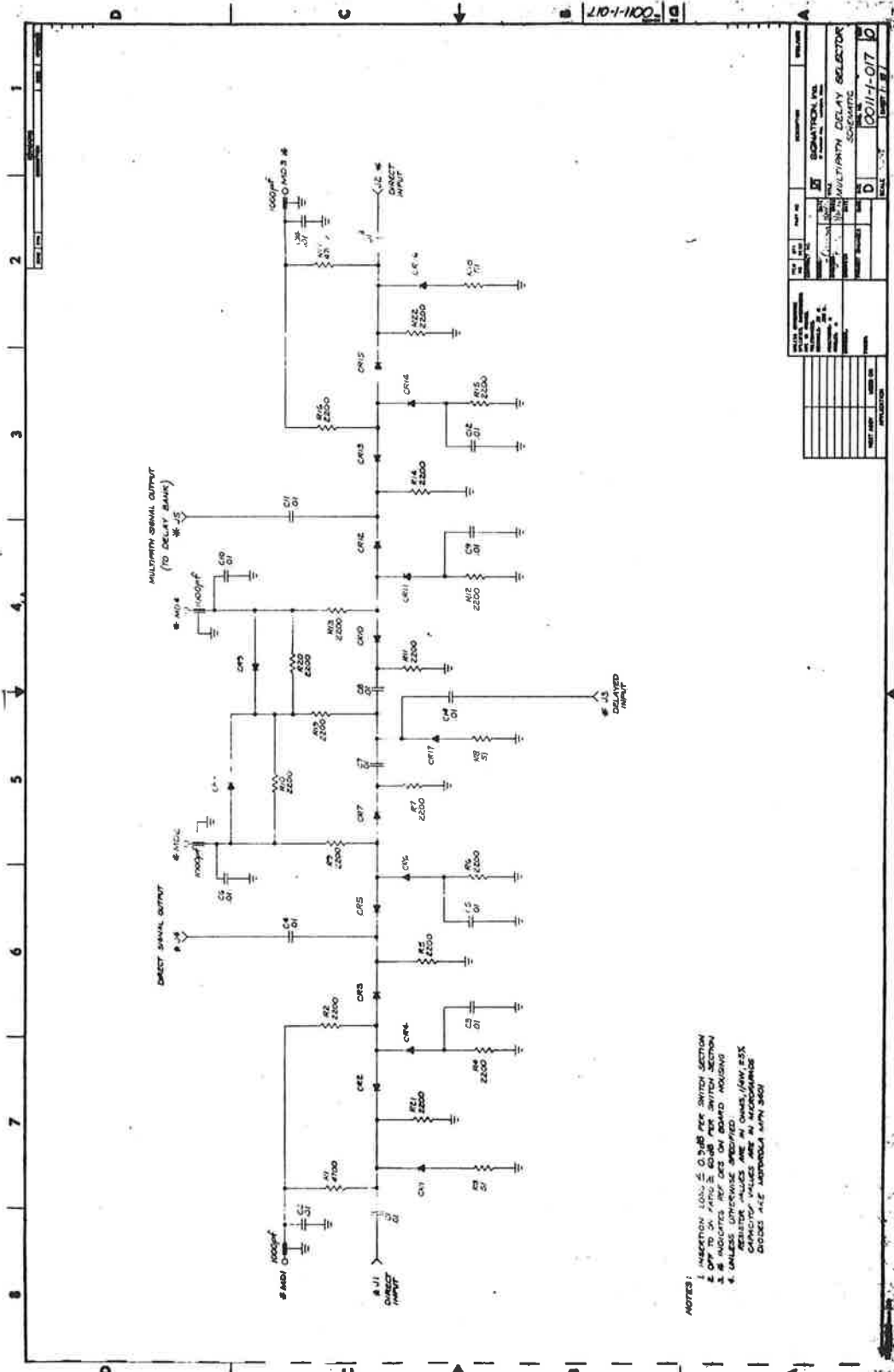
The schematic of the Multipath Delay Selector is shown in Drawing No. 0011-1-017. Switches Sw_2 and Sw_3 are a PIN diode switching matrix which maintains a constant 50 Ω impedance at all ports regardless of the "position" of the switches. The switch control lines MD_1, MD_2, MD_3, MD_4 activate the switches with +5 V (on) and -5 V (off). The control of Sw_2 and Sw_3 is such that J_4 and J_5 cannot both be simultanously connected to J_3.

The multipath delay selector switch matrix is constructed on a stripline printed circuit board.

5.1.6 Output Mixer/Filter Module No. 0011-1-018
(Serial No. 001)

The Direct Channel signal at 30 MHz from J_4 of the Multipath Delay Selector is up converted to 70 MHz in the Output Mixer/ Filter module No. 0011-018 (Serial No. 001). A fixed frequency 40 MHz oven stabilized crystal oscillator (located in the Synthesizer drawer) is used as a local oscillator for the up-conversion mixer. In this way the ±1000 Hz Doppler frequency shift on the direct channel is maintained.

Drawing No. 0011-1-019 illustrates the schematic of the Output Mixer-Filter module No. 0011-1-018. The local oscillator signal is padded down 8.5 dB to a level of 0 dBm to obtain optimum performance from this mixer. The mixer output is filtered using a three pole Butterworth filter centered at 70 MHz with a 3 dB bandwidth in the order of 15 MHz.

The filter is followed by a PIN diode switch to allow the direct signal channel to be turned off during test and calibration procedures. The switch maintains a 50 Ω impedance in both ON and OFF states. A control voltage of +5 V (on) or -5 V (off) at terminals DC control the switch.

A 9 dB pad is used at the module output to reduce the output signal to -32 dBm. All circuitry for the output mixer/filter is mounted on a stripline printed circuit board.

5.1.7   Output Mixer/Filter Module No. 0011-1-018
         (Serial No. 002)

The multipath channel at 30 MHz (from J_7 at the rear of the chassis) is up converted to 70 MHz in the Output Mixer/Filter module No. 0011-1-018 (serial No. 002). The schematic for this unit will be found in Drawing No. 0011-1-023.   Module No. 0011-1-018 (serial No. 002) is identical to serial No. 001 except for three details:

1) a three pole Butterworth bandpass filter is included in the input signal path before the mixer to attenuate spurious products developed in the tap modulation,

2) a different value for the output attenuator is used to set the multipath channel signal level at output terminal J_3 to -33 dBm*,

and 3) the local oscillator source is an oven stabilized 40 MHz VCXO. The VCXO is used to generate the ±100 Hz relative Doppler shift using a control located on the Synthesizer front panel.

_____

* With only one tap modulator on and the system in the TEST, I&Q mode. This is the RMS value of one tap modulator. The peak output of any one tap modulator when operating in the   OPERATE Mode is approximately 10 dB greater.

5.1.8 Output Combiner Module No. 0011-1-020

The direct channel and multipath channel are combined in the Combiner Module No. 0011-1-020. The schematic for this unit will be found in Drawing No. 0011-1-021. A four port hybrid (R-H-30V) is used to sum the direct signal and the multipath signal, the "sum" port being used as an output, and the "difference" port is used as an output test point which is brought to the output test jack located on the front panel of the Input/Output Interface Chassis.

Wideband hybrid circuit amplifier A_1 is used to boost the level of the multipath signal relative to the direct signal. Amplifier A_4 is used to raise the level of the sum of the signals.

Fuse F_1 and Zener. VR_1 are used to protect the module in case excessive DC supply voltages are applied.

5.1.9 S/M (Signal-to-Multipath) Attenuator

Note that the level of the direct channel signal into the Output Combiner is fixed. The Signal-to-Multipath (S/M) ratio is controlled by attenuating the multipath channel relative to the direct channel using the S/M attenuator located on the front panel of the Input/Output Interface Chassis.

5.1.10 S/N (Signal-to-Noise) Attenuator

In a manner similar to the S/M control, the signal, (i.e., direct and multipath to additive noise (S/N) ratio is controlled by the S/N attenuator located on the front panel of the Input/ Output Interface Chassis.

OUTPUT COMBINER SCHEMATIC

NOTES:
1. * INDICATES REF DES ON BOARD HOUSING
2. FUSE F1 IS LITTELFUSE PICOFUSE OR EQUIVALENT

5-16

5.1.11 L Band Input/Output

A single crystal controlled L band local oscillator source at 1555 MHz and a signal splitter are used to generate local oscillator signals for and L band to 70 MHz down converter mixer and a 70 MHz to L band up convertor mixer. The interconnection of these mixers and local oscillator source with the other elements of the Input/Output Interface subsystem is clearly shown by Drawing 0011-1-001 and is self-explanatory. The L Band source, consisting of a crystal oscillator/amplifier, multiplier chain, and output filter is not field repairable.

5.1.12 Input/Output Subsystem Chassis Wiring

Drawing 0011-1-001 (sheet 2) shows the Input/Output Subsystem chassis wiring diagram which includes all DC power supply and control wiring. Note that the Input Selector Switch is interconnected with the TEST MODE switch in the TEST SYSTEM chassis. The TEST MODE switch defeats the INPUT SELECTOR switch when the TEST MODE is in any position other than OPERATE. Refer to Dwg. 0011-1-001 for all RF signal interconnections.

5.2 Tap Modulator Subsystems

The tap modulator subsystem block diagram is illustrated in Dwg. No. 0011-2-001 (sheet 1). The purpose of the tap modulator subsystem is to produce five simulated multipath signals having a gross signal path delay of 30 μsec and a delay spread of 8 μsec, in 2 μsec intervals. This is accomplished in the following manner, refering to Dwg. No. 0011-2-001 (sheet 1).

A sample of the direct path signal at J_3 is amplified to +25 dBm by the high level buffer amplifier 0011-2-010. The output of the buffer amplifier is split five ways using an eight-way splitter with three output ports terminated. The five outputs from the signal splitter are each passed through a delay line. The five delay lines are 30, 32, 34, 36, and 38 μsec to develop
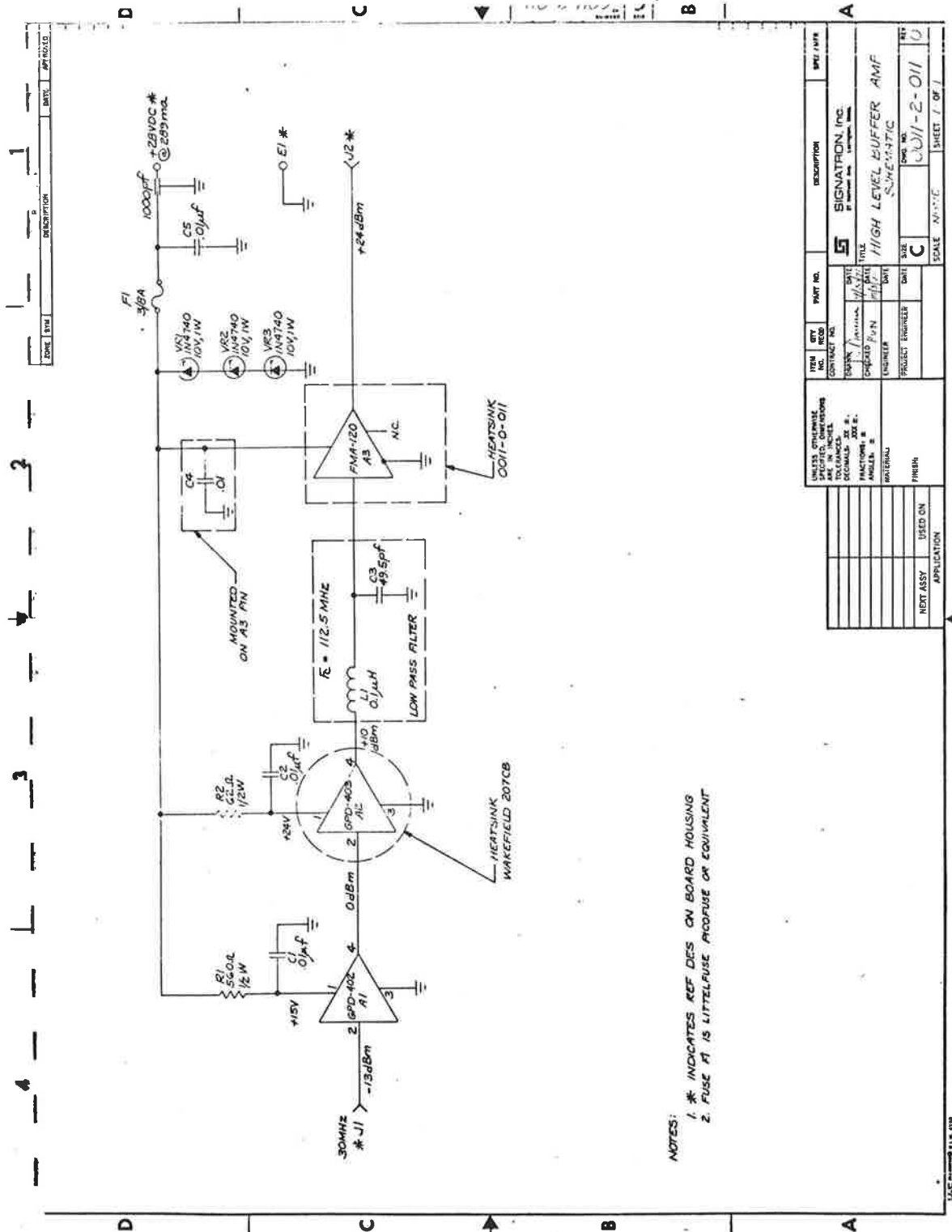
the required 2 μsec separation, 8 μsec delay spread, and 30 μsec gross delay. The delay lines have in the order of 45 to 50 dB insertion losses. Buffer-Amplifiers 0011-1-014 follow each delay line in order to compensate for the loss of the delay line. The gain of each amplifier is internally adjusted to compensate for the loss of the preceding delay line so that the output of all the buffer-amplifiers 0011-1-014 are at a level of +3 dBm ± 1 dB. This is the required drive level at the input to the five tap modulators. The tap modulators, described in more detail in Sec. 5.2.5 below, are used to multiply the delayed signals with noise so as to simulate the random amplitude and phase characteristics of multipath signals.

The output of each tap modulator represents a multipath signal. Each of the five output multipath signals passes through a front panel mounted continuously variable attenuator to allow manual setting of the multipath delay-power profile. After attenuation the five multipath signals are summed in the eight-way summer (with three ports terminated) and the final output of the tap modulator subsystem appears at J_4.

A detail description of each of the circuit modules of the tap modulator subsystem follows.

5.2.1 High Level Buffer Amplifier 0011-2-010

Drawing 0011-2-011 is the schematic for the High Level Buffer Amplifier 0011-2-010. The unit is constructed using three wideband hybrid integrated circuit amplifiers using stripline printed circuit techniques. The noise bandwidth of the A_1-A_2 preamplifier is approximately 500 MHz. To limit the noise loading of the power amplifier stage, A_3, the two pole lowpass filter with a cutoff frequency of 112.5 MHz is used as an interstage coupling device.

5-18

High Level Buffer Amp Schematic

NOTES:
1. * INDICATES REF DES ON BOARD HOUSING
2. FUSE F1 IS LITTELFUSE PICOFUSE OR EQUIVALENT

Resistors R_1 and R_2 are used as DC supply voltage dropping
resistors and also as RF decoupling elements. Capacitors C_1,
C_2, C_4, C_5, and C_6 serve as RF bypass and decoupling devices.
Fuse F_1 and Zener diodes VR_1, VR_2 and VR_3 serve as an over-
voltage protector in case the supply voltage should accidentally
exceed 28V DC.

5.2.2 Eight-Way Split BHJ-141-B

A five-way impedance matched power split is accomplished by
using an eight-way splitter and terminating three output ports
with 50 Ω loads. The eight-way splitter is formed by using a
tree of seven, two-way hybrid signal splitters. It is necessary
to use hybrid junctions to provide isolation (more than 30 dB)
between output ports. In this way mismatches and reflections
from the various delay lines are isolated from each other
effectively preventing "crosstalk" effects.

5.2.3 Tap Modulator Delay Lines

The five delay lines used in the tap modulator subsystem
are identical except for delay time, to the 25 μsec unit used in
the Input/Output interface subsystem.

5.2.4 Tap Modulator Buffer-Amplifier 0011-1-014

The schematic of the Tap Modulator Buffer-Amplifier Model
0011-1-014 is illustrated in schematic 0011-2-017. Three hybrid
integrated circuit amplifiers, A_1, A_2, and A_3 are used to amplify
the highly attenuated signal coming from each delay line. The

NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%. CAPACITOR VALUES ARE IN MICROFARADS

2. * INDICATES REF DES ON BOARD HOUSING

3. FUSE F1 IS LITTELFUSE PICOFUSE OR EQUIVALENT
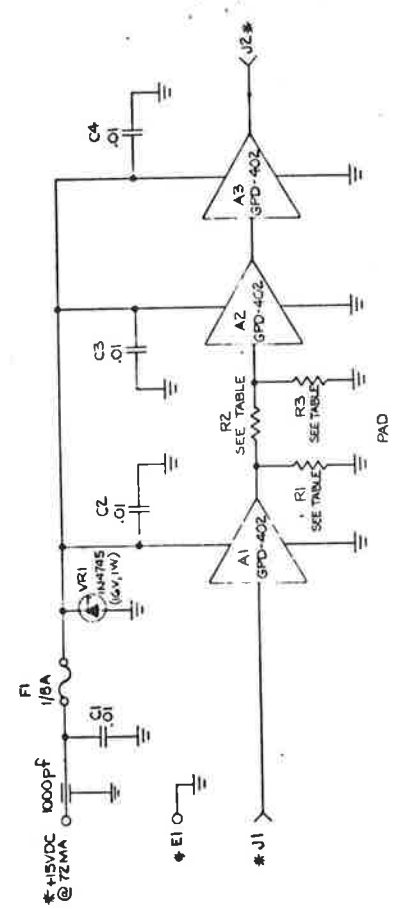
SERIAL NO	PAD VALUE	K1,R3 VALUE	R2 VALUE
001	3dB	300	18
002	6dB	150	39
003	12.5dB	82	100
004	10dB	100	68
005	2dB	430	12

+15VDC @ 72MA
1000pf
C1 .01
F1 1/8A
VR1 1N4745 (16V,1W)
*E1
*J1
A1 GPD-402
A2 GPD-402
A3 GPD-402
C2 .01
C3 .01
C4 .01
R1 SEE TABLE
R2 SEE TABLE
R3 SEE TABLE
PAD
*J2

SIGNATRON, Inc.

TAP 1400 BUFFER-AMPLIFIER SCHEMATIC

DWG NO. 001-2-07

SHEET OF 1

insertion loss and therefore its signal output of each delay
line differs slightly. However, the required input drive level
of each tap modulator is +3 dBm. Therefore, the gain of each
buffer-amplifier unit is adjusted at manufacture using an inter-
nal pad to produce exactly +3 dBm output when driven by its
designated delay line. The channel number, delay value, serial
number, and internal pad value of each of the five Top Modulator
Buffer-Amplifiers are listed in the schematic.

RF decoupling is provided by capacitors C_1 through C_5.
Fuse F_1 and Zener VR_1 provide protection against accidental
applications of excessive voltage.

5.2.5 Tap Modulator 0011-2-014

A Tap Modulator block diagram appears in Drawing No. 0011-2-001.
Drawing No. 0011-2-015 illustrates the schematic of a Tap Modula-
tor. These units are built on stripline printed circuit boards.

Each tap modulator consists of a wideband high level hybrid
power amplifier, A_1. The amplifier output is split in a.wide-
band 3 dB hybrid power splitter DS-109 and the two output signals
are phase shifted to develop a 90° relative phase difference
between the two equal signal components. The two signals in phase
quadrature are now multiplied by independent noise voltages in the
two precision modulators. Ten dB pads are placed between the
phase networks and the modulators to prevent phase variations due to
loading effects of the modulators. The insertion loss of each
modulator is approximately 6 dB. The outputs of each modulator is a
bipolar signal having a random amplitude as a result of the multipli-
cation process. The relative phases of the two modulator outputs
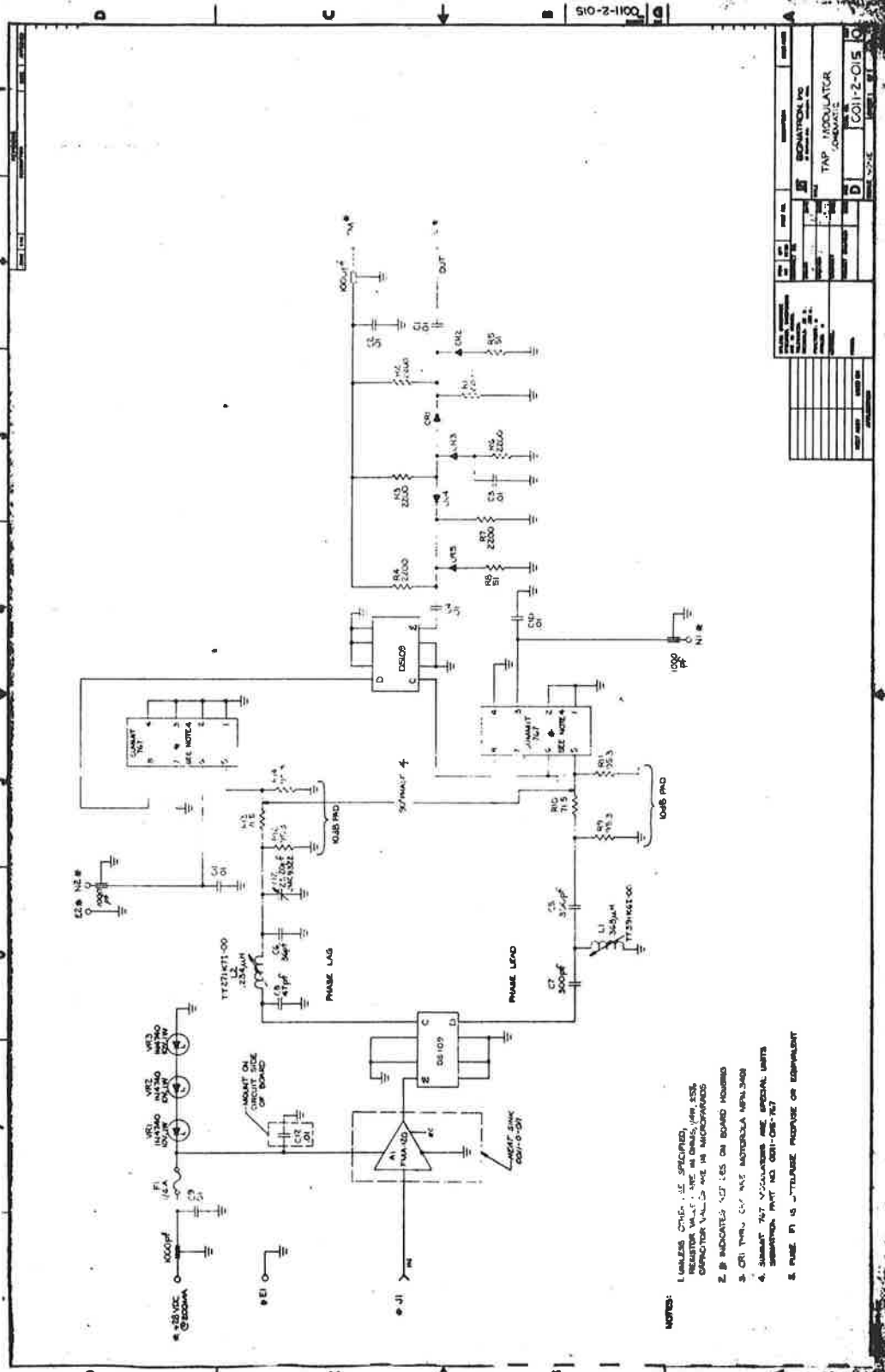
5-22

remain in phase quadrature. When added in a wideband 3 dB hybrid summer (DS-109), the combined outputs of the two modulators form a signal having the random amplitude random phase characteristics of a multipath signal.

Each tap modulator includes a stripline PIN diode switch to allow each multipath channel to be turned off to aid in calibration and alignment. The switch is designed to provide 50 Ω impedance at both input and output ports regardless of the state of the switch. The switch is controlled by +5 V (on) and -5 V (off) at terminal TM.

Fuse F_1 and Zener diodes VR_1, VR_2, VR_3 provide over voltage protection in case excessive supply voltage is applied.

5.2.6 Tap Modulator Subsystem Chassis Wiring

Drawing No. 0011-2-001 (sheet 2) shows the Tap Modulator Subsystem wiring diagram which includes all DC supply and control wiring. Note that the Multipath Delay Selector switch controls the Delay Selector module 0011-1-001 which is located in the Input/Output subsystem.

Refer to Dwg. No. 0011-2-001 for all RF signal interconnections.

5.3 Signal Synthesizer Subsystem

The Signal Synthesizer Subsystem of the RF signal processing portion of the Aerosat simulator is illustrated in Dwg.0011-3-001. This chassis contains the three 40 MHz precision oven controlled quartz oscillators used for local oscillators in the Input/Output Interface subsystem. One of the three 40 MHz osccillators (f_3) is fixed, the other two are voltage controllable using front panel potentiometers. One 40 MHz oscillator (f_1) generates the ±1000 Hz Doppler offset on all signals, the other (f_2) generates the ±100 Hz Relative Doppler offset on the multipath signal only.

A 70 MHz crystal oscillator used as a built-in test signal source is also a part of the signal synthesizer subsystem.

Finally, as shown in Dwg. 0011-3-001, the Additive Noise Modulator 0011-3-010 and the Additive Noise Low Pass Filter used to generate 50 kHz bandwidth Additive Noise is also located in the signal synthesizer subsystem.

It will be noted from observations of the S-140 front panel layout that the digital noise generator bandwidth controls are located on the front panel of the Synthesizer Control subsystem. This is a mechanical and operational convenience only. Mounting of the digital system control switches on the panel above the digital system permits easy access to the digital cards for servicing and alignment. All electronics of the digital noise generator except the bandwidth control switches are located in the digital noise generator drawer.

Two Pamotor 4500C Cooling fans are located in the Synthesizer Control chassis. They serve to cool the digital system and flush cooling air throughout the Channel Simulator mainframe.

5.3.1 Additive Noise Low Pass Filters

The additive noise low pass filters are located in the synthesizer drawer. The inputs to this unit are the two pseudo-random sequences produced by the Additive Noise PRN Generator located in the Digital Noise Generator subsystem drawer.

Drawing 0011-3-013 is a schematic of this unit. The bit rate of the input sequences is 500 kHz. It has been found that a filter with a 3 dB cutoff frequency which is approximately one twentieth the bit rate is most suitable for producing pseudo-random noise. Accordingly, the input sequences are each filtered in a two-pole 25 kHz Butterworth filter.

The filtered pseudo-random noise is then passed through a 20 Hz high pass filter to remove the DC component. Next the signals are amplified by a pair of wideband operational amplifiers. The outputs of the amplifiers drive the Additive Noise Modulator inphase and quadrature inputs.

The rms value of the noise voltages at the output is 133 millivolts. This may be adjusted by means of P1 and P2.

The bandwidth of the 25 kHz low pass filters may be trimmed by means of L1 and L2.

5.3.2 Additive Noise Modulator

The schematic of the Additive Noise Modulator 0011-3-10 is illustrated in Dwg. No. 0011-3-011. A 70 MHz input signal from the 70 MHz test oscillator is split in a hybrid power divider DS-109. Each output from the divider is multiplied by an independent 25 kHz baseband noise signal (N_1 and N_2) in the two 767 modulators. The noise modulated signals are attenuated to approximately -20 dBm and combined using a quadrature power summer, JH-115.

The output of each 767 modulator is a double sideband noise modulated signal. After combining in the JH-115 quadrature combiner, the resultant signal is an approximately Gaussian bandpass noise with an rms noise bandwidth of 50 kHz.

The output of the additive Noise modulator is switched ON or OFF in a PIN diode switching matrix. The switch is controlled by + 5V (ON) and - 5V (OFF) on control line AN. The switch output is further attenuated at the noise modulators output to achieve the desired - 60 dBm/MHz equivalent noise density.

5.4 Digital Noise Generator System

The noise waveforms which modulate the outputs of the five delay line taps are produced by the digital noise generators.

Since the waveforms must be exactly reproducible both in shape and in time scale, the noise is derived from a set of digital pseudo-random number generators. Since the bandwidth of each tap must be independently variable while maintaining reproducible sets of noise waveforms the clock pulses for the pseudo-random number (PRN) generators must be synthesized from a common source.

Figure 5.4-1 is a block diagram of the digital noise generators. The timing source is a crystal oscillator. The oscillator drives clock synthesizer which is controlled by a bank of digi-switches located on the "Synthesizer Control" panel. By means of these switches the double sided rms bandwidth of the noise waveform may be varied from 10 Hz to 1.99 kHz in 10 Hz steps.

The five outputs of the clock synthesizer drive five digital noise generators. Each noise generator contains a pair of maximal length shift registers plus a pair of digital filters. The feedback connections in each of the shift registers are different
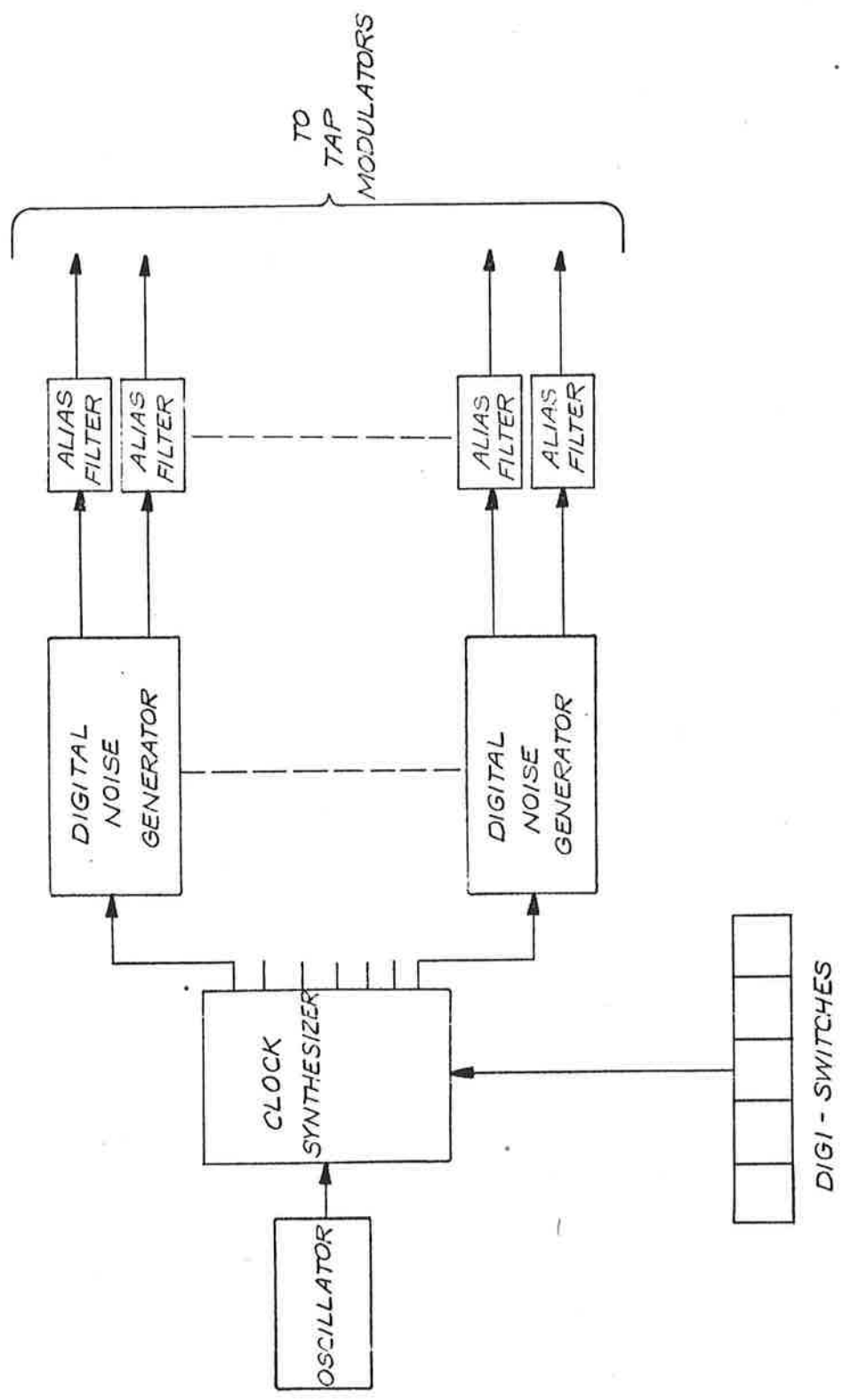
5-28

Fig. 5.4-1 Block Diagram of Digital Noise Generator System

so that the noise patterns produced are different. The two outputs of each noise generators are the same bandwidth but statistically independent thus they are appropriate signals to drive the inphase and quadrature inputs of a tap modulator.

The outputs of the digital noise generators are filtered by a set of alias filters which remove the unwanted high frequency components.

5.4.1 Mechanical Assembly

The digital noise generator system is built on CAMBION wire wrap cards. The timing is synthesized on one card which drives five nearly identical noise generator cards. The alias filter network requires half a card so three cards are required to contain this circuitry. The digi-switches are located on the front panel of the synthesizer control drawer which is directly above the digital noise generator drawer.

The wire wrap cards are contained in a Cambion card rack, minor modifications have been made to this rack to allow connectors to the power and the analog outputs to be mounted on it. The connection between the digi-switches and the backplane of the Cambion rack is made by means of a wiring card which accepts a cable at one end and plugs into a wire wrap card slot on the other end.

Also located in this card rack is the Additive noise source PRN generator. This card drives the additive noise low-pass filters which is located in the synthesizer control drawer.

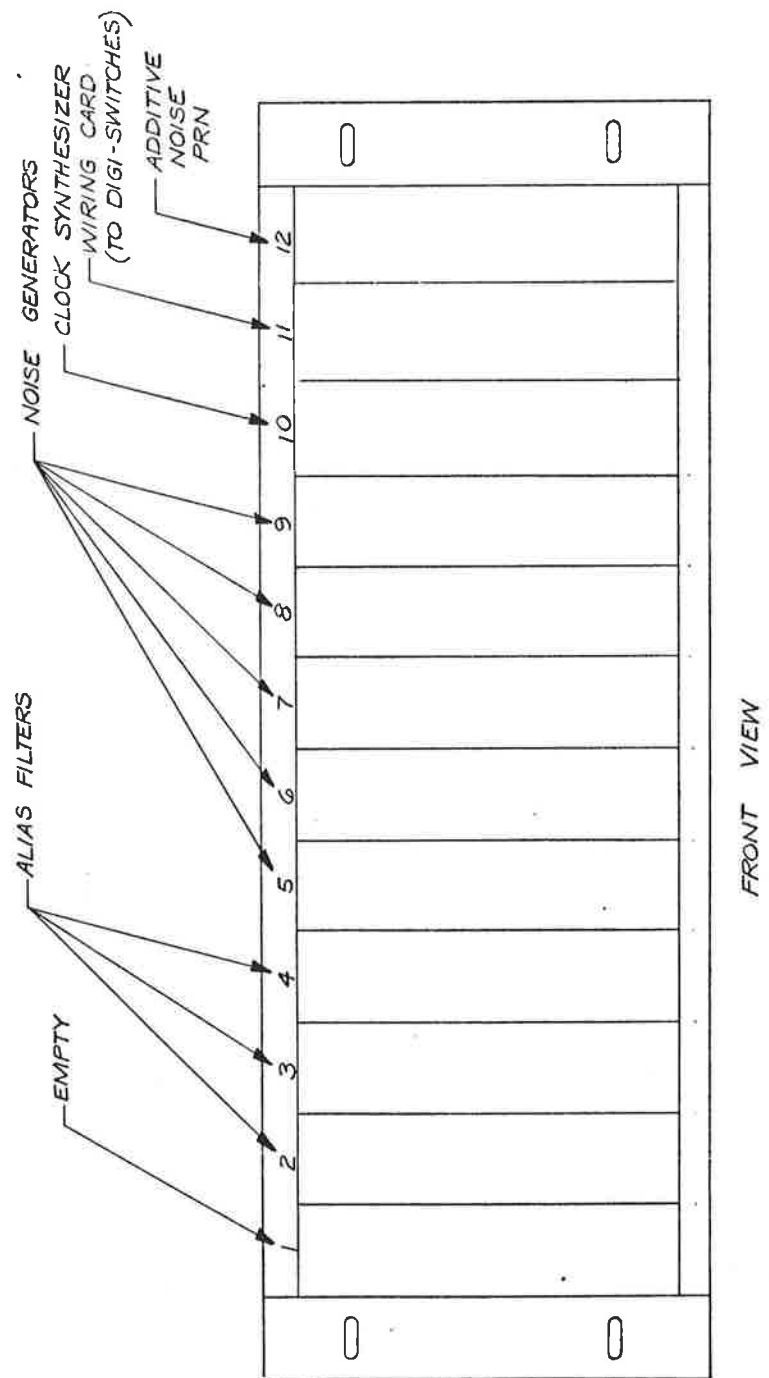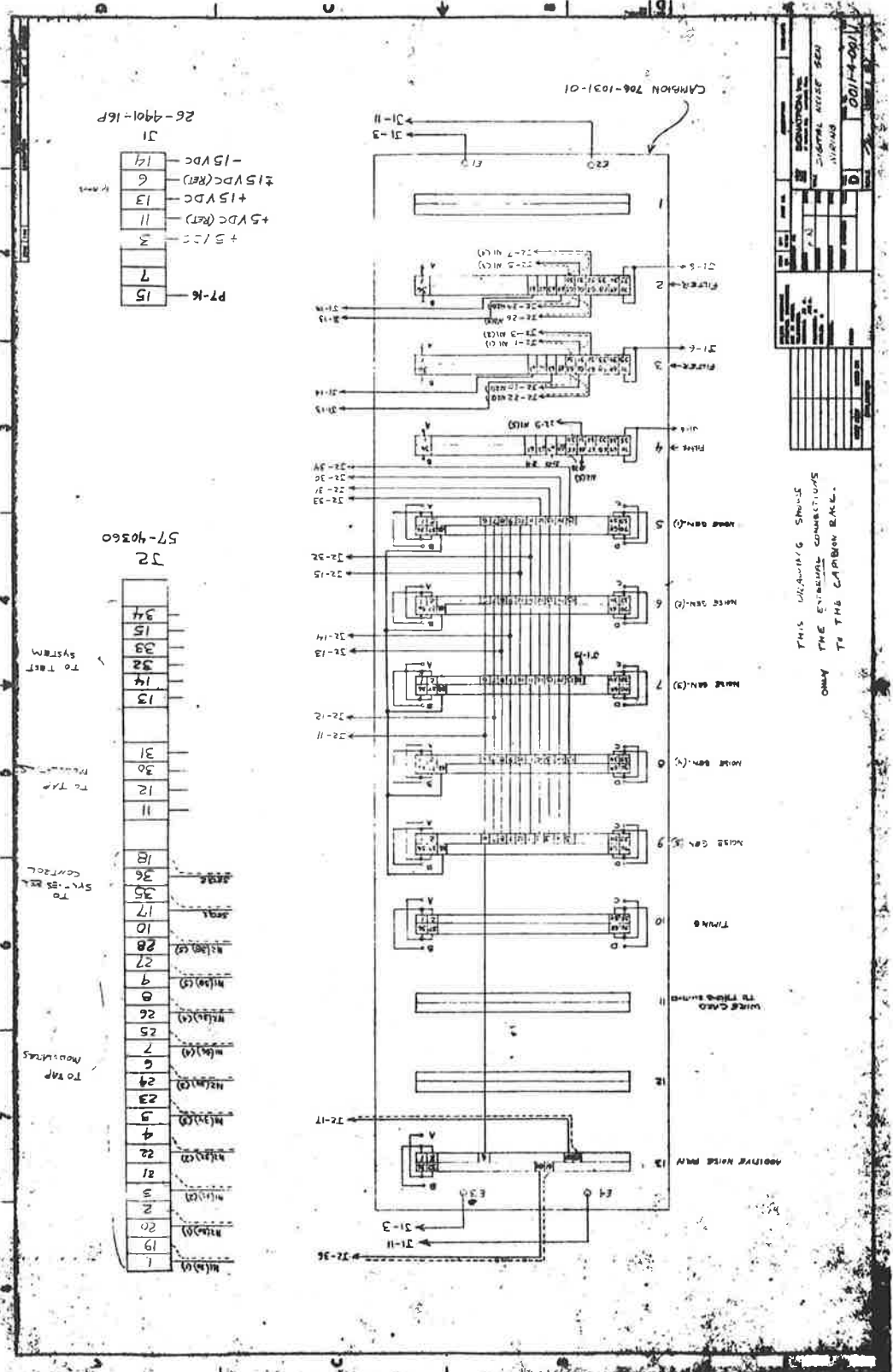Figure 5.4.1-1 shows the card locations while Dwg.0011-4-001 shows the connections to the backplane.

EMPTY

ALIAS FILTERS

NOISE GENERATORS

CLOCK SYNTHESIZER
WIRING CARD
(TO DIGI-SWITCHES)

ADDITIVE
NOISE
PRN

FRONT VIEW

Fig.5.4.1-1 Digital Noise Generator Chassis

5.4.2 Digital Noise Generators

Figure 5.4.2-1 is a detailed block diagram of one digital noise generator. The output of the clock synthesizer increments two maximal length shift registers (PRN generators). The PRN generators drive two digital filters. The digital filters use serial arithmetic. They contain two serial accumulators which are tapped at strategic points, the output of the taps are subtracted from the input to the filter. The resulting network is a second order Butterworth filter. The accumulators consist of a shift register whose output is fed back and added to its input. By making the length of these shift registers twice as long as one word length, it is possible to time multiplex the filter between the two sets of pseudo-random data so that the two filters share a common set of adders and subtractors. The output of this network is alternately read into one output buffer register and then the other.

Provision is made at the output buffer to insert a digital number which equals the rms value of the noise voltage. This number is switched in when the rms channel gain is set.

Drawing No. 0011-4-011 is the logic diagram of the digital filter boards. Sheet one shows the timing and control logic. Sheet two shows the shift registers, adders, subtractors and output buffer and sheet three shows the PRN generators and then divided by seventy-two counters.

The first forty bit register is made of of I.C.'s 25, 26 27 and 28; the second is made up of I.C.'s 41, 42, 43, and 44.

In the first accumulator the data word is shifted four bits and subtracted from itself. This is done by taking the output
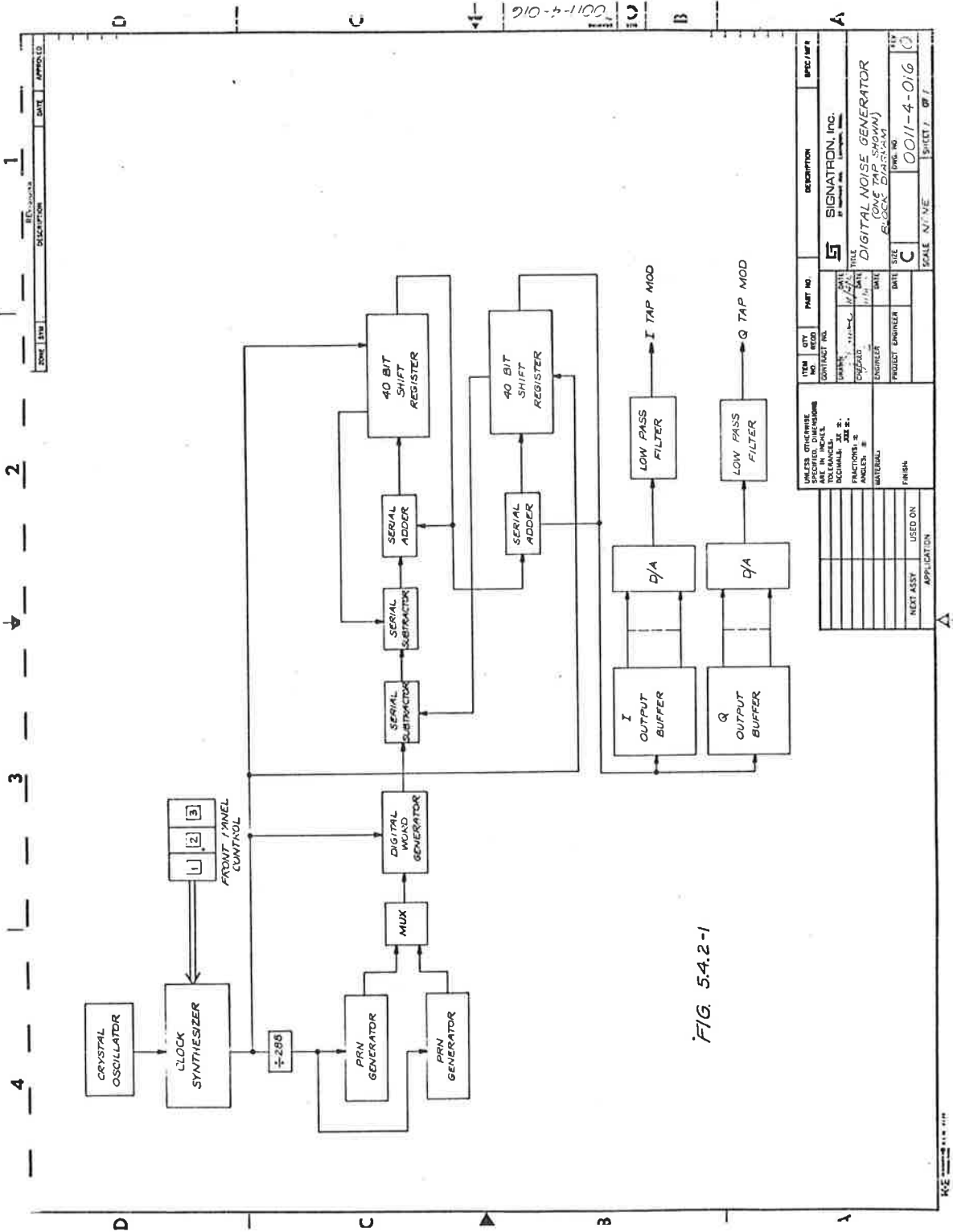
FIG. 5.4.2-1

SIGNATRON, Inc.

DIGITAL NOISE GENERATOR
(ONE TAP SHOWN)
BLOCK DIAGRAM

DWG. NO. 0011-4-016

of the fourth from the last stage, inverting it and adding it to the output of the last stage. Since the arithmetic is serial the sign of the work must be stretched from the most significant bit of each word to the final bit (least significant) of the next word.

The sign stretching is performed by I.C.'s #37 and 36. The most significant bit appears at the fourth from last stage four bits before it appears at the last stage. It is sampled and held in the flip-flop and gated into the adder for the last four bit times of the word.

The input to the filter is one of two seven bit serial words corresponding to the numbers plus thirty-two and minus thirty-two. These words are produced by the logic on I.C.'s #32, 24 and 39.

When the PRN generator produces a one the plus word is used. When it produces a zero the minus word is used.

The feedback connections for the second forty bit shift register are similar to those of the first register except that the output of the ninth from the last stage is fed back. Again, the sign is stretched to the end of the word.

The output of the second accumulator is alternately read into one then the other of the two output registers made up of I.C.'s 49, 50 and 51 and 52, 53 and 54. The outputs of these registers are passed through a pair of twelve pole double throw digital switches. When the noise generators are in the calibrated mode these switches provide a digital word at the output whose

value is such that the output of the D/A will be equal to the rms value of the normal noise signal.

Sheet one of Dwg. No. 0011-4-011 shows the timing and control circuitry. I.C.'s 4 and 5 make a modulo twenty counter. This is used to clear the carry flip-flop in the adders at the end of each word cycle of the serial accumulators and to generate the timing for the sign extention. The signals SQA, SQB and SEX are produced for this purpose.

The unit may be used in several modes according to the switch positions. The normal operating mode is with the FREEZE/FADE switch in the FADE position, STA and STB in the normal position and the RESET pushbutton not pressed. Putting the switch in the FREEZE position stops the PRN generators forces the PLUS and MINUS words to zero and rearranges the feedback logic in the accumulators such that the data simply recirculates without changing its value.

To prevent transients the unit must enter and leave the freeze mode synchronously. This is done by means of the flip-flop on I.C. #7. This flip-flop follows the Freeze/Fade switch position but only changes state at the end of a word cycle.

The Reset pushbutton clears the accumulators and resets the PRN generators. Again this must be done synchronously. This is accomplished by the PRCLR flip-flop.

The STA and STB switches are ganged together; they control the twelve pole double throw digital switches. The output word to DA #1 is forced to its rms value when the switch is in the I position the other word is forced to zero. When the switch is in the Q position DA #1 is forced to zero and DA #2 is forced to its

rms value. When the switch is in the I & Q position both DA's are forced to the rms value. When the switch is in the BALANCE position both DAs are set to zero.

Sheet three of Dwg 0011-4-011 shows the PRN generators. The input clock is taken from the second stage of the modulo twenty counter QB. This is in turn divided by 144. This gives a clock which is 1/288 of the shift rate of the accumulators.

The PRN generators are twenty-five bit shift registers .
The outputs of several stages are exclusively ored together to yield a maximum length sequence generator with a period of $2^{25}-1$ bits. The ten PRN generators on the five boards each have different feedback connections so the sequences are all different. The table and sheet 3 indicate the feedback connections for each generator.

The outputs of the two generators are multiplexed into the digital filter such that the data for one filter is always derived from the same PRN generator.

5.4.3 Clock Synthesizer

The clock synthesizer produces a coherent set of clocks to drive the noise generator. The relationship between the sample rate and the three dB cutoff frequency of the digital filter is:

$$S = \frac{64\pi}{\sqrt{2}} \, f_{3dB} = 137 \, f_{3dB}$$

The design of the filter is such that forty clock pulses are required for each output sample. Thus the maximum clock rate (for a double sided B.W. = 1.99 kHz) equals

$$C\ell_{max} = 142 \times 40 \times 995 = 5.68 \text{ MHz}$$

The minimum clock rate is

$$Cl_{min} = 142 \times 40 \times 5 = 28.4 \text{ kHz.}$$

Figure 011-4-013 shows the clock synthesizer. A mod 200 counter
is driven by a 28.4 MHz crystal oscillator. At the time when the
counter reads zero a flip-flop is cleared. The flip-flop con-
trols a gate which allows the 28.4 MHz to pass while the flip-flop
is cleared. When the count in the counter reaches the number
which matches the number set on the digi-switches the flip-flop
is set, gating off the 28.4 MHz pulses.

Thus the number of pulses out of the gate during each cycle
of the mod 200 counter is between one and 199 according to the
setting of the digi-switches.

The pulse trains produced in this manner are uneven, however,
if the pulses are divided by a modulo 200 divider a set of evenly
spaced pulses will result. The clock pulse into the digital
filters need not be evenly spaced as long as the samples which
appear at the output are evenly spaced. Since the output samples
occur once for every forty input clock pulses, the digital filter
acts like a modulo forty divider. Therefore if the gated 28.4
MHz pulses are divided by five before being applied to the digital
filters the overall divide ratio will be 200. Since the maximum
clock rate required is 5.68 MHz and it must be pre-divided by five
the counter must operate at 5 x 5.68 = 28.4 MHz.

Referring to the figure the mod 200 counter is the I.C.'s
numbered 15, 23, 31, 39, and 47 the feedback connections for the
counter or I.C.'s #16, 24 and 56. The flip-flop shown on the left
in I.C. #46 controls the pulses for Cll the clock for the first
noise generator. I.C.'s # 14, 30, and 62 form a comparator which
compares the state of the counter with the number set in the

digit-switches when a comparison occurs the flip-flop is set.
C28A is the 28.4 MHz clock . It is gated by IC #55 in accordance
with the state of the flip-flop. I.C.'s #53 and 54 form the
divide by five counter which divides the pulses to produce C11.
This network is repeated on the right hand side of sheet 1 to
produce C12 and three more times on sheet 2 to produce C13, C14
and C15.

5.4.4 Alias Filters

Drawing No. 0011-4-015 is the schematic of the alias filter
boards for the noise generators. This board converts the digital
output of the noise generators to analog form then removes the
alias spectrum of the noise and adjust the signal to a level
suitable for driving the tap modulators. Each alias board con-
tains four alias filters and four D/A converters so that each
board can accommodate two noise generators.

Since the bandwidth of the noise varies by a two hundred
to one ratio it is not possible to remove the alias spectrum
with one single pole filter. Therefore two single pole low pass
filters are used, an analog switch selects one filter or the other
depending upon the setting of the digi switches. The gain and
offset of each output amplifier may be adjusted by means of
potentiometers.

5.4.5 Additive Noise PRN Generator

The Additive noise pseudo-random number (PRN) generator is
part of the additive noise system. A pair of binary pseudo-random
sequences are generated on this card then go to the Additive Noise
low-pass filters. The low-pass filtering converts the wideband
binary sequence to continuous noise waveforms which may be ex-
actly reproduced by resetting the PRN generator.

The two noise waveforms modulate the inphase-and quadrature components of a carrier in the additive noise modulator to produce a 50 kHz wide noise.

The PRN generator board contains a 1 MHz crystal oscillator which clocks a thirty-nine bit maximal length sequence generator; at this rate the period of the sequence is about six days. Alternate bits of the sequence are read into a pair of flip-flops to produce two sequences each going at a bit rate of 500 kc .
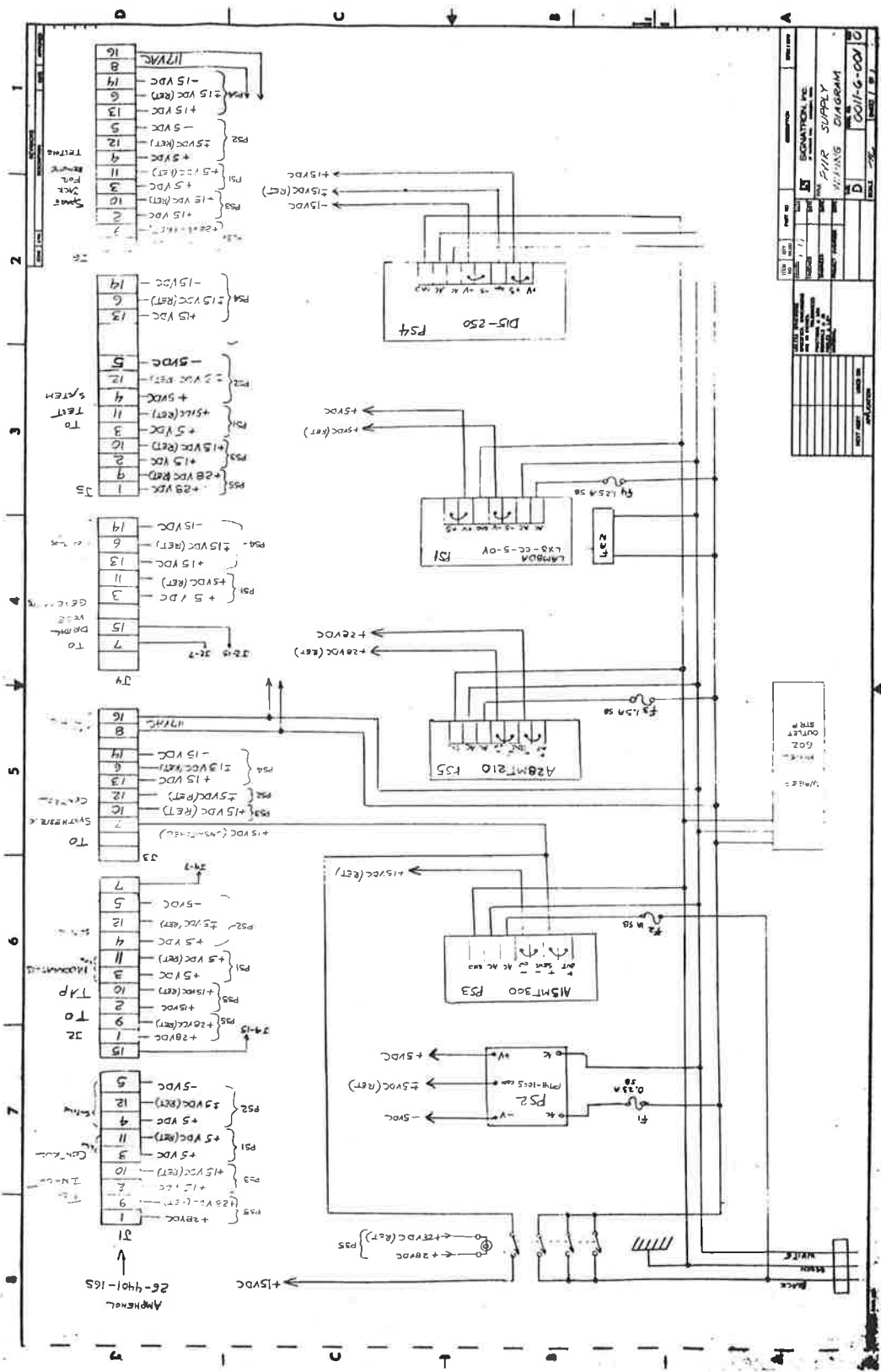
The sequences of bits which occur at the output of these two flip-flops are identical; however, they are shifted with respect to one another by a number of bits equal to one-half the sequence length. Therefore, there is delay of six days between the two sequences.

The PRN generator is set to a particular state each time the reset button is pushed.

5.5 Power Supply Subsystem

The schematic for the Power Supply subsystem is shown in Dwg. No. 0011-6-001. There are five power supplies used in the system. The primary function of each is listed below.

PS1	High current + 5 VDC supply used for digital logic
PS2	Low current $\pm$ 5 VDC supply used to control the PIN diode RF switches
PS3	+ 15 VDC unswitched supply for precision oven stabilized crystal oscillators
PS4	$\pm$ 15 VDC supply used for Digital-to-Analog converter and operational amplifiers
PS5	+ 28 VDC supply used for RF amplifiers.

It should be noted that PS3 is operating whenever the simulator is connected to a 115 VAC power source.

Drawing No. 0011-0-002 is the mainframe power cable wiring diagram from the power supply subsytem to all simulator sub-systems.

5.6 Test System

The schematic of the Test System appears in Dwg.No.0011-5-001. The primary functions of the test system are to control sub-systems elsewhere in the Simulator mainframe via the Test Mode Switch, and to provide means to measure RF power levels and to monitor System operating DC voltages.

5.7 Subsystem RF Signal Cable Interconnections

The RF interface between all signal processing subsystem of the Aerosat Channel Simulator occurs via rear panel. Coaxial con-nections are shown in Dwg. No. 0011-0-004.

5.8 Subsystem Data and Control Signal Cable Interconnections

Drawing # 0011-0-003 illustrates the Cable and Connector interface connections between all S-140 subsystems.

PWR CABLES DIAGRAM

CO11-0-00210

SIGMATRON Inc
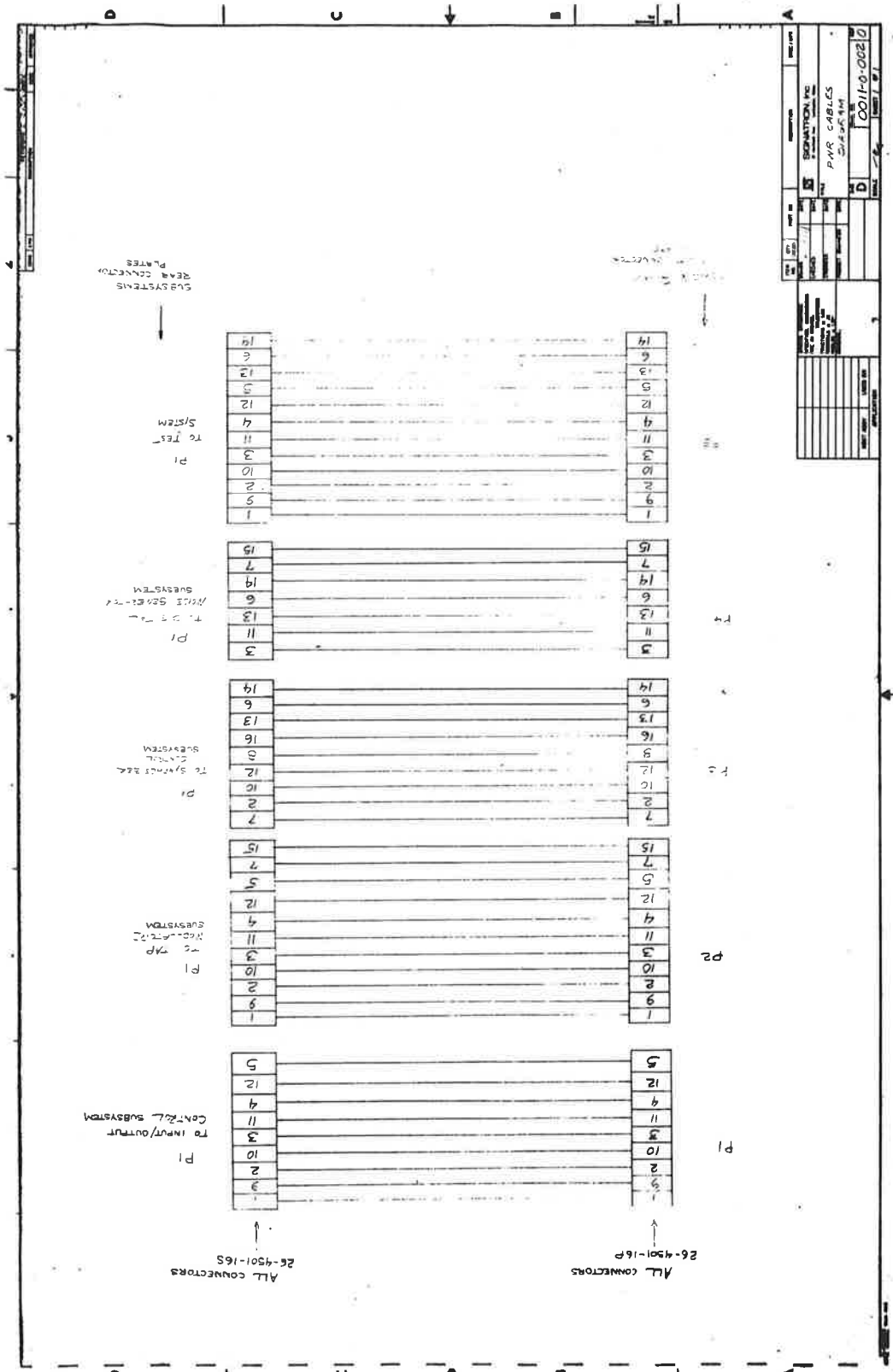
SUBSYSTEMS REAR CONNECTOR PLATES

P1 — TO TEST SYSTEM
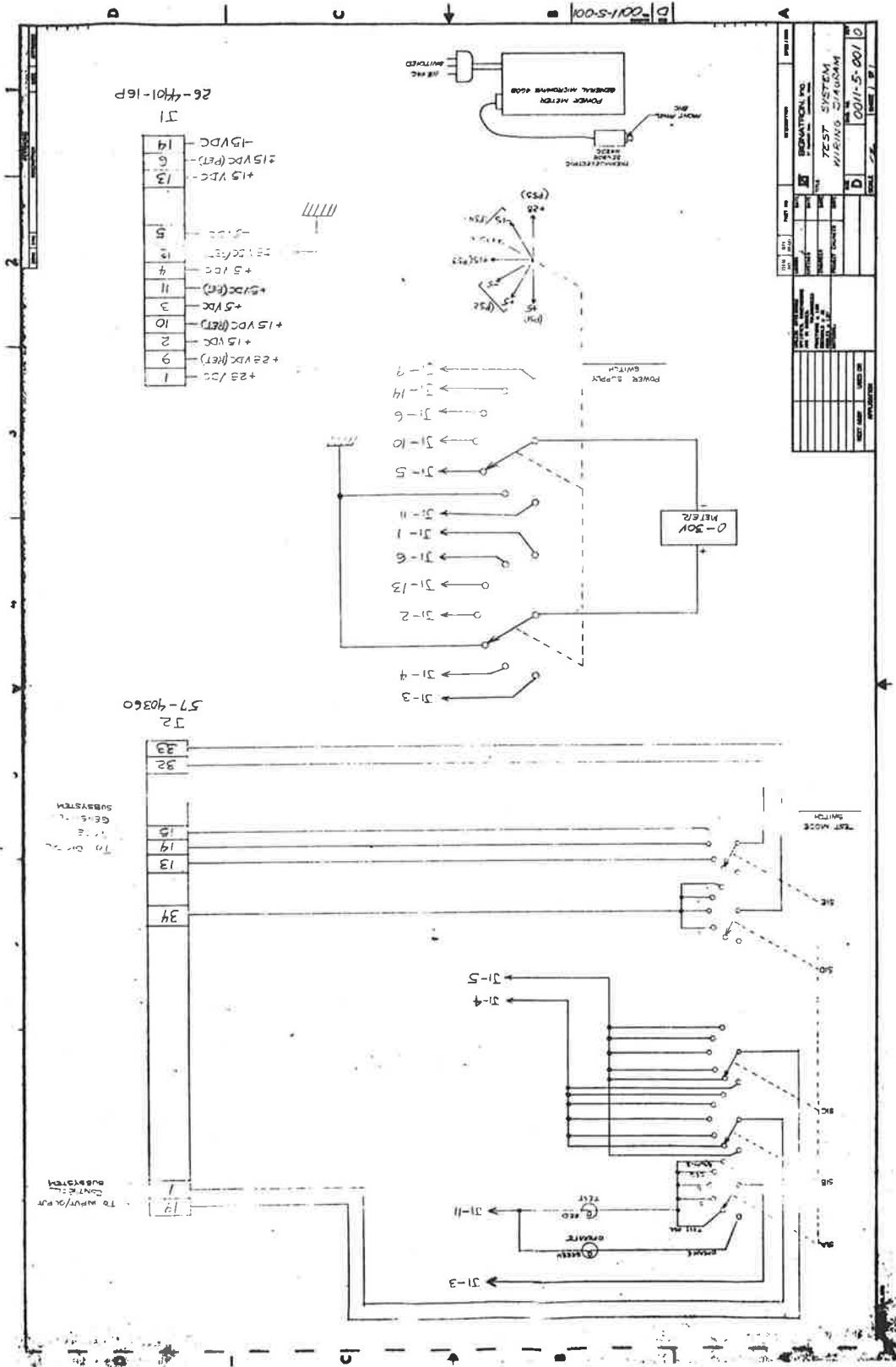
P1 — TO SIGNAL GENERATOR SUBSYSTEM

P1 — TO SYNTHESIZER SUBSYSTEM

P1 — TO TAP REGULATOR SUBSYSTEM

P1 — TO INPUT/OUTPUT CONTROL SUBSYSTEM

ALL CONNECTORS
26-4501-16S

ALL CONNECTORS
26-4501-16P

INPUT/OUTPUT CONTROL SUBSYSTEM

- J3 FREQUENCY 1 (40 MHz + Δ, L.O.)
- J4 FREQUENCY 2 (40 MHz + δ, L.O.)
- J5 FREQUENCY 3 (40 MHz, L.O.)
- J6 TEST FREQUENCY (70 MHz)
- J8 ADDITIVE NOISE
- J7 MULTIPATH SIGNAL
- J9 MULTIPATH DELAY

TAP MODULATOR SUBSYSTEM

- J3 INPUT
- J4 OUTPUT

SYNTHESIZER SUBSYSTEM

- J7 ADDITIVE NOISE
- J3 TEST FREQUENCY (70 MHz)
- J6 FREQUENCY 3 (40 MHz, L.O.)
- J5 FREQUENCY 2 (40 MHz + δ, L.O.)
- J4 FREQUENCY 1 (40 MHz + Δ, L.O.)

SIGNATRON, Inc.

TITLE: R.F. CABLES DIAGRAM

SIZE C   DWG NO 0011-0-0C4

SHEET 1 OF

5-46