technical note tech

En Route Radar Display Recording System (ERDIRS)

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February 1983

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16. Abstract

Characteristics and requirements for an En Route Radar Display Recording System (ERDIRS) which would record, store and playback air traffic control display data being provided to the National Airspace System Plan View Displays in an Air Route Traffic Control Center were developed. In addition, an ERDIRS Engineering Model was designed and fabricated as a total in-house effort in order to explore various ideas and to provide background and experience to define the details of a field system design. Following the design and concurrent with the fabrication of the engineering model, the system design data for the engineering model was generated, and a functional specification for an operational field version of the ERDIRS was drafted for the Airway Facilities Service.

As a result of the engineering effort, it was concluded that the specification does describe the complete functional characteristics of a practical field ERDIRS that meets all basic operational requirements and that the engineering model does demonstrate that a practical field ERDIRS can be developed.

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INTRODUCTION

PURPOSE.

The purpose of this project was to develop the characteristics and requirements for an En Route Radar Display Recording System (ERDIRS) which would record, store, and playback air traffic control display data being provided to the National Airspace System (NAS) Plan View Displays (PVD) in an Air Route Traffic Control Center (ARTCC). In addition, this information was to be used to generate a draft functional specification for a system to be implemented into the field.

BACKGROUND.

There has long been a need within the Federal Aviation Administration (FAA) to recreate, on demand, air traffic histories for the purpose of performing an analysis of operational situations. As a step toward satisfying this need, the FAA Technical Center was tasked to conduct a feasibility investigation into various techniques and methods to record, store, and reproduce en route air traffic control display data exactly as seen by the controller. During this study period, several data pick-off points were investigated along with possible recording techniques, including television raster scan recording, analog deflection recording, and digital recording. As a result of this study, the most promising technique was selected and a single display breadboard model was designed, fabricated, and demonstrated at the FAA Technical Center, Atlantic City, New Jersey. This investigation, including breadboard model development and demonstration, was documented in FAA Final Report, FAA-RD-78-97 dated September 1978, entitled "A Breadboard Model Used to Demonstrate the Feasibility of Recording National Airspace System En Route Display Data." In this report, it was concluded that the breadboard model, employing the digital recording technique and utilizing the interface between the Display Generator Input-Output (DGIO) and the Display Control and Vector Generator (DCVG) as the display data pick-off point, adequately demonstrated feasibility. Further, it was recommended that a full-scale multiple-channel engineering model be designed and fabricated as the next logical step toward development of a detailed functional specification for an operational field system. Subsequently, the FAA Technical Center was assigned this task as a total in-house effort.

GENERAL APPROACH.

Although the breadboard model demonstrated the feasibility of recording and playing back air traffic control display data from a single PVD, there were many details that needed to be investigated before the breadboard concepts could be expanded to meet the needs of an operational field system. One primary point of investigation involved the development of a permanent method of picking off the data to replace the temporary method used with the breadboard model. This included the development of a modification to the Display Generator Unit (DGU) that would provide a permanent recording port. Therefore, an engineering model of the ERDIRS was used as a vehicle to explore various ideas and to provide the background and experience needed for team members to define the details of a field system design. Following the design and concurrent with the fabrication of the engineering model, a document entitled "ERDIRS Engineering Model System Design Data" was generated, and a functional specification for an operational field version of the ERDIRS was drafted. While the system design data cover the characteristics of the engineering

model, and the draft functional specification defines the characteristics of a proposed operational field system, this report will summarize the various primary characteristics and functions of the field system and discuss differences between the engineering model and the proposed operational field system. In addition, it will provide other information pertinent to the further development of the specification. Copies of both the system design data and draft functional specification are included as appendices.

DISCUSSION

GENERAL DISCUSSION.

Before designing the engineering model, the basic operational characteristics were defined by, and coordinated with, Systems Research and Development Service, Air Traffic Service, and Airway Facilities Service. These characteristics, which generally established the broad aspects of the system design, were modified and expanded as the design, fabrication, and testing of the engineering model proceeded and were used to form the basis of the field system specification. These final characteristics are briefly discussed in the following section. In later sections, both the engineering model and the proposed field system are described at the system level in order to show how these characteristics were implemented in the two systems.

BASIC SYSTEM CHARACTERISTICS. A recording system for use in an ARTCC must be capable of recording all data presented on each PVD by picking off the digital data sent to the associated DCVG. The display data to be recorded are those used to refresh the PVD primary cathode-ray tube. This includes aircraft targets and associated data blocks, map data, weather data, time of day, trackball, assorted lines, etc., and does not include information concerning brightness or focus settings, or data associated with the Radar Keyboard Multiplexer.

The recording system must have sufficient capacity to record air traffic display data being provided to all active sectors (R-positions) in a particular ARTCC. In addition, the system must be capable of being expanded to record display data for up to a maximum of 120 PVD's.

The interface between the display computer and the recording system must be "transparent" to the host system. That is, there must be no software load on the display computer, a minimum of hardware changes, and a minimal added load on existing power supplies. In addition, the interface must be applicable for recording data from any of the existing display computers (i.e., Computer Display Channel, Display Channel Complex, or Direct Access Radar Channel used in the field.

In order to minimize the amount of data to be recorded and to reduce the amount of redundancy in the recorded data, a sampling technique, by which a complete presentation from each PVD is recorded periodically, must be used.

Each recorder used in the system must be capable of recording on a single reel of tape for at least 4 hours, after which the tape will be removed for storage for a specified time period. The system must employ pairs of recorders operating in a sequential mode so that when one recorder approaches end-of-tape, the second will automatically begin to record, thus providing an overlap of recorded data. This same automatic switchover operation must occur in the event of a failure of the on-line unit, with the exception that there will be no overlapping of data. Manual switchover must also be a feature of this system in order to recover and secure specific tapes. Another important feature is machine-to-machine compatibility so that a tape recorded on one machine can be played back on another of the same type and manufacturer without the need for any special adjustments. Also, the recorders must incorporate a read-after-write feature to facilitate visual monitoring of the recorded data via playback equipment and a PVD.

The system must be capable of playing back data from up to two PVD's simultaneously. It must not require the use of any part of the operational display computer equipment and must not allow playback at any operational position, that is, a position being used to control live traffic. In addition, it must be capable of updating the presentation at both normal and twice normal playback speeds, as well as being capable of freezing any specific presentation indefinitely. The system must also be capable of synchronizing the playback of a tape containing recorded PVD data with the playback of an associated voice tape and of searching a data tape at a high speed in order to locate specific sections of interest.

Finally, all major equipment must be monitored for errors and failures. This information must be reported at a panel in the main equipment area where it will be used to form the basis of determining system status that will be reported to the System Maintenance Monitor Console.

SYSTEM DESCRIPTION — ENGINEERING MODEL. The engineering model is a developmental PVD recording system designed, built, and tested in-house by the FAA Technical Center. A block diagram is shown in figure 1. Photographs of the primary units are shown in figures 2 and 3. The System Design Data, prepared by the FAA Technical Center, is contained in appendix A. This recording system interfaces with the DGU which is utilized by all of the en route display computer systems presently in use by the FAA. The recording interface is located at a point that is beyond all software processing and data filtering and is as close to the PVD as was practical, taking into consideration the ability to detect and sample complete frames of data, ease of interfacing, cost, etc.

The ERDIRS unit which receives data from a DGU and transmits these data to the recorders is called the Record Interface Buffer (RIB). The actual interface between the DGU and the RIB is the ERDIRS record interface which consists of a modification to the DGIO unit within the DGU. Each RIB is capable of acquiring data being provided to all six DCVG/PVD's associated with each DGU.

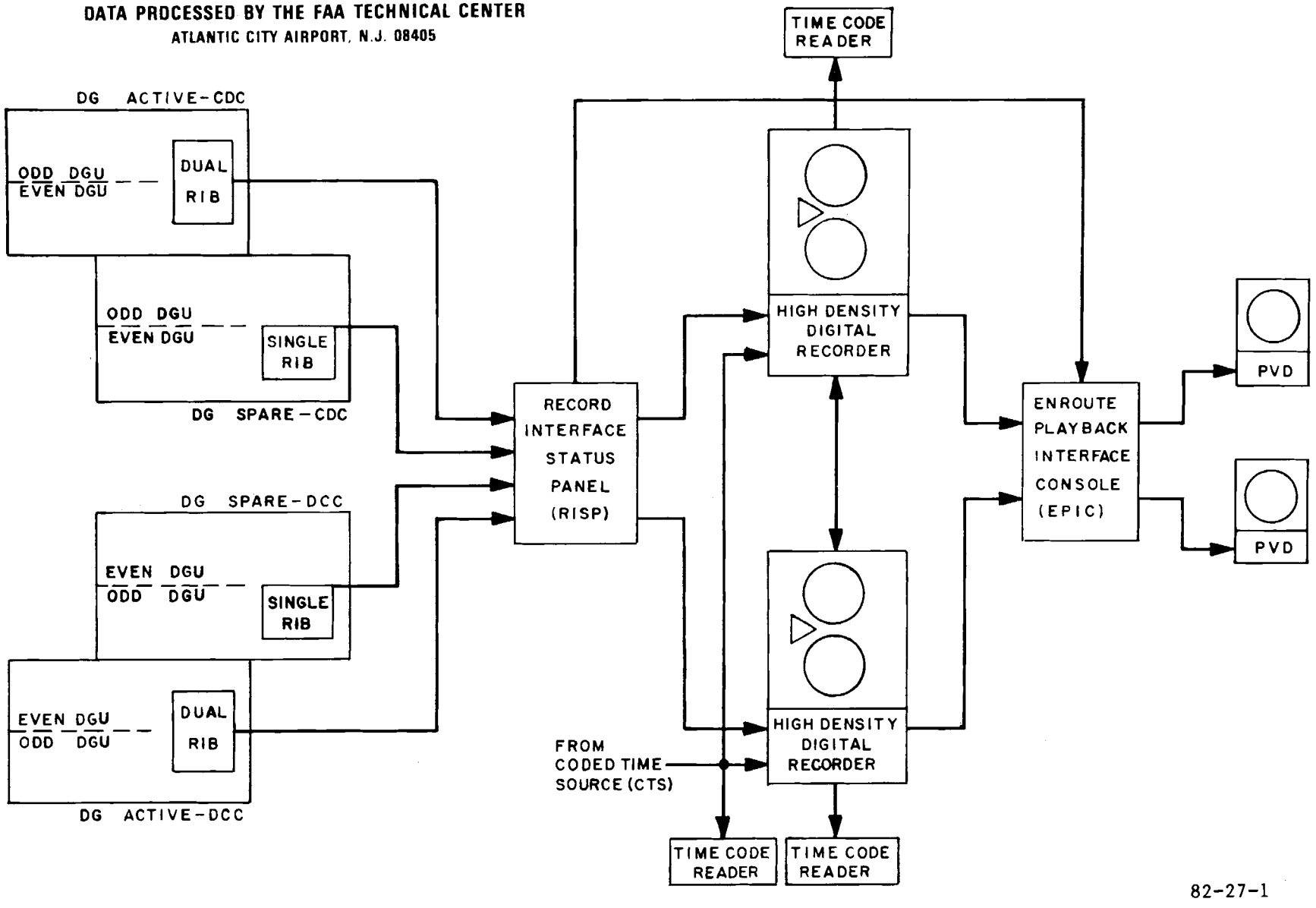


FIGURE 1. ERDIRS ENGINEERING MODEL BLOCK DIAGRAM

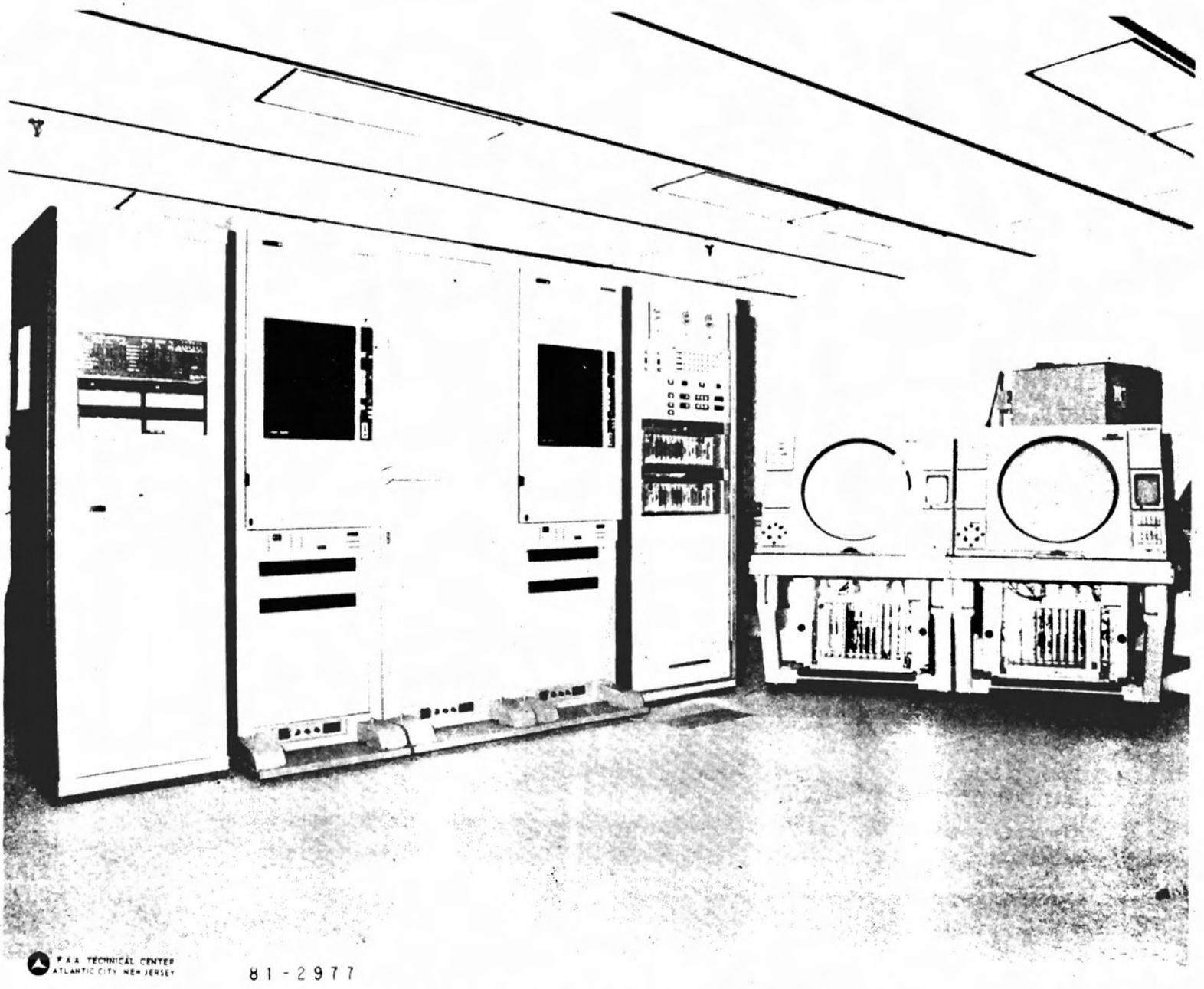


FIGURE 2. ERDIRS ENGINEERING MODEL EQUIPMENT

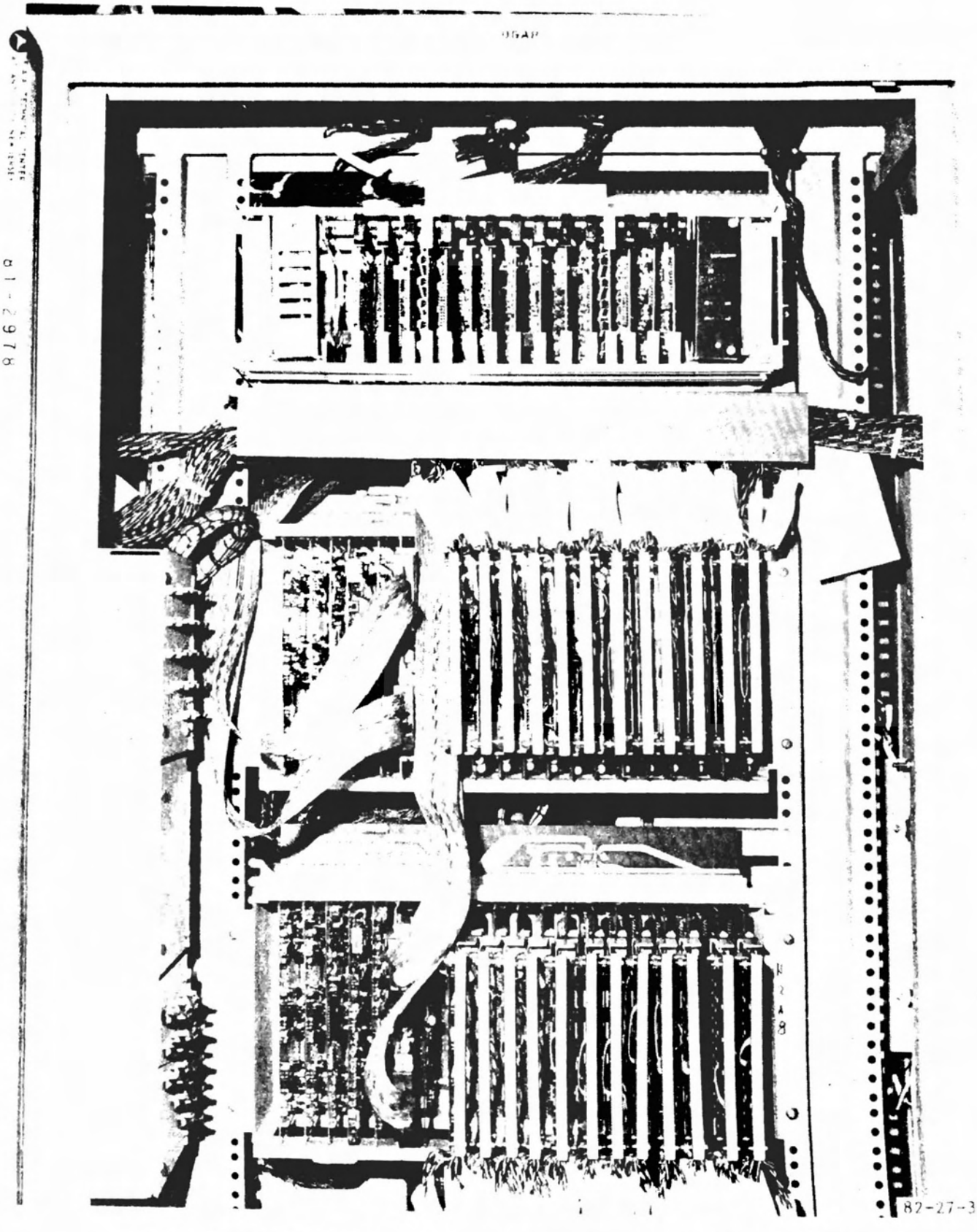


FIGURE 3. ERDIRS ENGINEERING MODEL — RECORD INTERFACE BUFFER

The recorders used in the engineering model were configured to record the output of six RIB's, for a total display capacity of 36 PVD's. Although the Technical Center has both a DCC and a CDC system, each has only two active DGU's, for a total of 24 active DCVG's. Therefore, a single card cage containing two RIB's was installed in each active Display Generator (DG) cabinet. (Each DG cabinet consists of two DGU's.) This provided for the recording of all 24 active DCVG's. The balance of the recording capacity was used to record two spare DGU's (12 DCVG's). It was the intention of the project team to install a RIB with each of the four spare DGU's in the two host systems. This would provide for tracking reconfigurations in either the CDC or DCC systems on playback. Due to a limitation on the number of DGU's that could be recorded, a RIB would be installed in each of the four spare DGU's and only two spare DGU's (from either the CDC or DCC systems) would be recorded at a given time. However, since Airway Facilities Service requested that one spare DGU in each display computer system be left unmodified, only single RIB's were installed in the spare DG cabinets. This limited the ability to track reconfigurations.

During recording, one complete refresh frame of data for each of the six PVD's is sampled by the RIB and temporarily stored in a semiconductor memory, nominally every 1/3 second (depending on the data load). Each frame contains all data necessary to build a single display image on playback. These frames of data are transferred from each RIB to the Record Interface and Status Panel (RISP) before being transferred to the recorder. They are also sent to a multiplexer within the RISP which allows the En Route Playback Interface Console (EPIC) to receive the sampled PVD data directly, bypassing the recorders. The recorder bypass is primarily used to check the quality of data prior to recording. In addition, status information from the RIB's is received and displayed at the RISP.

The recorders consist of two Ampex HBR-3000 28-track High Density Digital Instrumentation Recorders capable of operating in an alternating or sequential mode in order to provide for continuous recording. These recorders also have a read-after-write capability so that data written on tape may be monitored immediately after recording. The tape speed employed is 7 1/2 inches per second, thus providing approximately 4.1 hours of recording on 9,200 feet of tape (14-inch reel).

Playback of display data is performed using the EPIC which contains two En Route Playback Interfaces (EPI), two DCVG's, and a control and status panel. Since there are two EPI's and two DCVG's within each EPIC, the capability exists to play back display data from any two PVD positions simultaneously, allowing for side-by-side review of handoffs between sectors, etc. Each EPI is designed to emulate that portion of the display computer refresh subsystem that provides data to the DCVG/PVD. It receives the sampled display data from the recorders via two playback multiplexers in the RISP, stores it in one of two alternating memories, and refreshes a PVD with the data at the proper rate through a DCVG. Controls at the EPIC provide the capability to select which recorded PVD is to be displayed at the playback PVD, to select data from each recorder, or to select data at the input to both recorders (bypass). In addition, other controls including freeze controls, master reset, etc., along with status information concerning each EPI, are provided at the EPIC. Also, for maintenance purposes, there are controls which allow one EPI to monitor the input data of the other EPI.

SYSTEM DESCRIPTION — FIELD SYSTEM. The following is a description of the proposed ERDIRS field system that could be used to record PVD data at ARTCC's in the contiguous United States. The block diagram is shown in figure 4. A detailed draft functional specification (appendix B) has been prepared and is based upon the concepts utilized in the engineering model and the knowledge gained during its development.

The proposed field system consists of two subsystems: The Recording Subsystem and the Playback Subsystem. The Recording Subsystem would perform the functions of sampling and recording operational and training display data being sent to all operational and training PVD positions in the ARTCC. It would also provide the capability to visually monitor the sampled operational and training display data using either the SMMC PVD, or the maintenance PVD, or both. These two PVD's would serve a dual function since they would be capable of being switched independently between displaying "live" data directly from the display computer system and displaying recorded data from the ERDIRS. Since these PVD's are already used to monitor the operation of the display computer system, their dual use eliminates the need for additional dedicated PVD's to monitor the ERDIRS.

The Record Interface Equipment would perform all the functions handled by the RIB's and the RISP in the engineering model in that it would sample all the display data and provide it to recorders. With the exception of a printed circuit board which would be installed in the DGU and would provide the actual interface with the display computer system, all other units of the Record Interface Equipment would be located external to the DG cabinet.

Display data from the Record Interface Equipment would be provided to the operational recorders, the training recorder, and directly to the Playback Interface Equipment which would be used to monitor the recording operation. Furnishing the display data directly to the Playback Interface Equipment would bypass the recorders and provide the ability to view the display data prior to being recorded. By using this capability, along with the read-after-write capability of the recorders, it would be possible to view the display data both before and immediately after recording, using the monitor PVD's previously described. This would enable an operator to visually check the quality of the data being recorded.

Recording of display data would be on magnetic tape utilizing high density digital recorders similar to those used in the engineering model. The operational recorders would be paired and operated in a sequential mode in order to provide for continuous recording. Each recorder would be capable of recording data going to 72 PVD's, which is more than sufficient to handle all current ARTCC's. However, expansion is possible by adding another recorder pair. The training recorder would be identical to an operational recorder. Should it become necessary, the training recorder could be used to replace a failed operational recorder. Since training PVD's are generally intermixed with operational PVD's within the display computer system, both operational and training display data would be recorded on the operational recorders. Also due to this intermix, the training recorder could record both operational and training PVD data. There would be remote controls at two training positions that would be used to control the operation of the training recorder; however, these controls would not affect the operational recorders in any way.

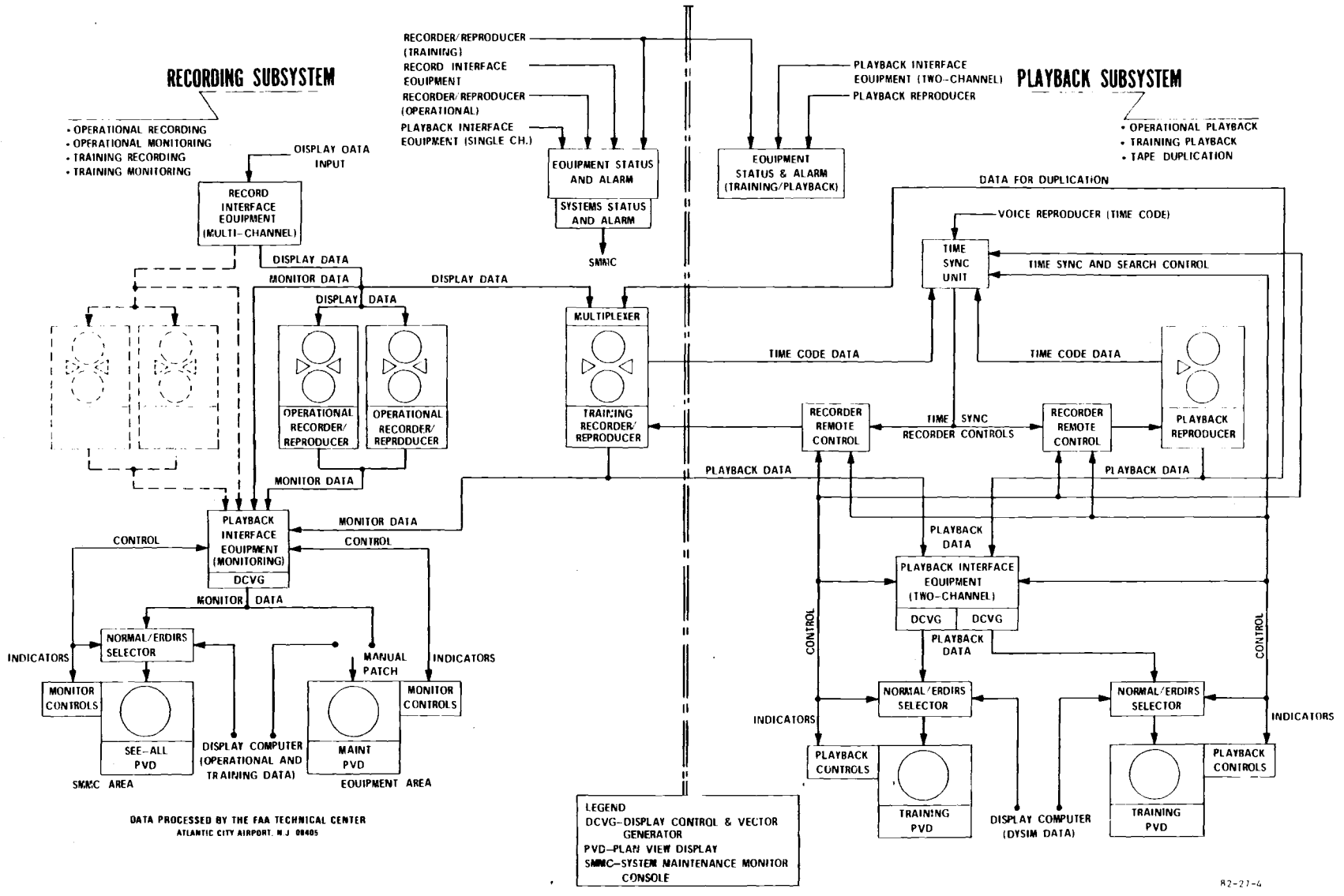


FIGURE 4. PROPOSED ERDIRS FIELD SYSTEM

The Playback Subsystem would perform the function of playing back both operational and training display data, and when required, perform the tape duplication function. The Playback Interface Equipment used to perform the playback function would be a two-channel unit so that display data from any two PVD's could be viewed simultaneously. Playback of operational display data would normally be performed using the operational reproducer, the Playback Interface Equipment, and either one or two PVD's. These two PVD's would be existing training positions which would also be used to perform the playback function. The dual use of training PVD's for both training and operational playback is considered practical since it eliminates the costly need for two dedicated off-line playback PVD's. The operational reproducer would be identical to the other recorders except it would have no record electronics or record heads. Playback of training display data would normally be performed using the training recorder, the Playback Interface Equipment, and either one or two of the training/playback PVD's.

During the record operation, the requirement exists to record a time code on a single dedicated track. This time code would provide the capability to synchronize the playback of an ERDIRS data tape and a voice communication tape so that a complete air traffic scenario could be recreated. In addition, this time code could be used to locate specific time periods on tape via high-speed search. With future air traffic control expansion, it is possible that two recorder pairs could be required in order to record an increased number of displays. This could result in having to playback two tapes simultaneously using both the training recorder and the operational reproducer. These two tapes would have to be synchronized with each other; and if a voice communication tape were to be played back also, the system must be capable of synchronizing all three tapes. Normally, the time synchronization function would be controlled remotely from either or both playback PVD's.

The tape duplication function would be performed utilizing the operational reproducer as the playback unit and the training recorder as the recording unit, with the balance of the Playback Subsystem available for monitoring the duplication process. In addition, the Playback Subsystem would have the capability to merge display data and voice onto a single tape.

Status monitoring would be performed by the ERDIRS, with error reports, status information, and alarm information being collected, processed, and displayed at the equipment. In addition, this detailed data would be used to generate system status information (i.e., operational, degraded, or failed states) for display at the Record Interface Equipment. System status information pertaining only to the Recording Subsystem would also be displayed at the SMMC.

DETAILED DISCUSSION.

The following paragraphs will describe some of the major features of the ERDIRS. Comparisons between the actual implementation of the engineering model and the recommended implementation of the proposed field system will be discussed along with the background information that forms the basis for our recommendations.

RECORD INTERFACE CONFIGURATION. In the engineering model, the equipment that acquire the data at the DGU's and transmit it to the recorders are called the RIB's and the RISP. This function is performed by the Record Interface Equipment in the field system.

The engineering model was designed such that the RIB is physically located inside the DG cabinet. This was done to minimize noise interference and signal degradation. Two RIB's, each servicing a DGU, share a single card cage (dual RIB cage) and are functionally independent except for sharing common output clock and status lines. Each RIB acquires refresh frames from up to six DCVG's associated with a DGU and provides these data to the RISP. The RISP then retransmits the data to the recorders and supplies a master clock to the RIB's and the recorders. In addition, because the RIB's are located inside the DG cabinet, the RIB status and alarm information is sent to the RISP for display.

The potential for expanding the engineering model, by increasing the number of PVD's that can be recorded, was investigated, and the design work was performed. Essentially, the design called for modifying the single RIB such that it could service, in a sequential manner, 12 DCVG's rather than six, thus eliminating the need for two RIB's in each DG cabinet. This would double the number of displays that could be recorded per reel of tape without changing the tape speed, but it would also double the display sample period. However, it is expected that doubling the sample period would not adversely affect the playback presentation. Although the design work was accomplished, the hardware modifications were not incorporated because of time and resource constraints. If redundant units are required, the proposed modification of the RIB does offer this potential. This could be accomplished by retaining the dual RIB cage design, with two modified RIB's, using the first RIB as the on-line unit and the second RIB as the standby (redundant) unit.

In the engineering model, the problem of recording display data from a display whose DCVG has been reconfigured is overcome by recording the data going to the two spare DGU's (12 DCVG's) on separate ports within the ERDIRS. This means that normally the ERDIRS would be recording both of these ports even though the associated spare DGU's are inactive and no data are present. Data are available on these two ports only when a reconfiguration of the display computer system has occurred. On playback, it is necessary to switch manually at the EPIC from the "active" to the appropriate "spare" port in order to continue receiving playback data for a specific display that had its associated DCVG reconfigured out of the system. The major disadvantage to this method of tracking reconfigurations is that it requires the use of additional RIB's for the two spare DGU's and the dedicated use of two ports involving eight tracks in the recorders.

In the field system, it is specified that the Record Interface Equipment will be external to the DG cabinets with the exception of the A6 interface board. During the development of the interface, the use of the spare A6 card slot in the DGIO card cage for the ERDIRS provided the physical space necessary to incorporate differential line drivers. By providing good noise immunity and less signal degradation, these drivers are able to transmit signals at distances that would provide the capability of centralizing the Record Interface Equipment external to the DG cabinet. This provides several important advantages:

1. It allows reconfiguration of the DCVG's to be handled on the record side.

2. By centralizing the Record Interface Equipment, it becomes more practical to design redundancy into the system (being centralized, one unit can spare more than one active unit) and provides more flexibility by removing the restriction to record in multiples of six DCVG's.

3. Although heat was not a particular problem in the engineering model, there would also be no appreciable heat load added to the DG cabinet, nor would heat generated in the DG cabinet affect the Record Interface Equipment.

4. Since the Record Interface Equipment would be installed in its own equipment rack(s), improved access and improved maintenance would be possible.

Reconfiguration of the DCVG's within the display computer system would be handled by the field ERDIRS on the record side rather than on the playback side, as was done in the engineering model. This means the ERDIRS would not record the data to any DCVG that is not in an on-line status and would record data to the spare DCVG in place of data to the reconfigured DCVG. In order to accomplish this, the reconfiguration signals available within each DGU must be monitored by the ERDIRS. Since no dedicated equipment or tape tracks would be assigned to off-line DCVG's, this technique would provide better tape and track utilization and might reduce the amount of equipment required.

Status and error reporting in the field system is detailed in the specification (appendix B). It provides for this information to be centrally displayed at the Record Interface Equipment rack(s), thus facilitating maintenance activities. Although not provided in the engineering model, general system status (operational/ degraded/failed) will be derived for each major piece of equipment in the field system. It will be displayed in the ERDIRS equipment area and also remoted to the SMMC in the air traffic control room.

ERDIRS RECORD INTERFACE. In order to allow access to the display data and its associated control signals, an interface between the recording system and the existing display computer hardware is necessary. As was discussed in the final report on the breadboard model (FAA-RD-78-97), the general area within the existing display computer at which this interface is most practical is within each DGU on the interface between the DCIO and the inputs to the DCVG's. The major reasons for selecting this point were: (1) the refresh data to be recorded are most condensed and accessible; (2) this point is where the use of a sampling technique is easiest to implement; and (3) the format of the data recorded allowed the Playback Subsystem to operate with a minimum of NAS hardware; that is, one off-line DCVG and one PVD per playback channel.

Various methods of implementing the interface were considered during the initial phase of the engineering model development. The principal requirements of the interface are:

1. It should provide access to a 16-line data bus carrying data for six DCVG's.

2. It should provide access to the interface control signals necessary to perform the record operation, including the 4.4 megahertz clock, "Words-per-Bank" (W/B), "Valid Address" (VAD), Master Reset, and "On-Line" signals.

3. It should require a minimum number of hardware changes to existing NAS equipment.

4. It should be transparent to the operation of existing equipment, that is, it should not require the host system to interface with the recording system in an active manner.

In the breadboard model, the record interface consisted of a temporary slip-on connector which was attached to the J1 input connector on the backplane of the DCVG to be recorded. With the exception of the "on-line" signal, this point provided access to all signals required by the breadboard model to interface with one DCVG. In the development of the engineering model, a more permanent interface with access to at least six DCVG's was sought.

There is a 16-line data bus within the DGIO that contains display data for the six DCVG's and is distributed among several printed circuit boards within the DGIO with no direct access at the backplane.

This common bus is divided into six buses, one for each DCVG. In order to minimize the effects of electronic interference, each bus is driven by gated line drivers which restrict each bus to carrying data for one DCVG only. These six buses are accessible at the backplane. Appendix A of the System Design Data provides details of the operation and structure of the DGIO. Three alternative solutions to the problem of accessing the multi-DCVG data bus were developed. They are as follows:

Plan A. In this plan, the common bus lines prior to the gated DCVG line drivers were to be brought out to the spare edge connections on the A1, A2, and A3 boards using wire jumpers as illustrated in figure 5. These signals would then be routed to a new board in the spare A6 card slot which would contain line drivers for interfacing with the RIB. The main advantages of this plan are that it could be readily implemented at the Technical Center and that it would leave the existing DGIO/DCVG interface virtually unaffected. The main disadvantage is that it would require the use of the spare A6 card slot. Even though this plan would be implemented in the engineering model by adding wire jumpers to the A1, A2, and A3 boards, the need for these jumpers in the field version could be eliminated by replacing these boards with updated versions.

Plan B. This plan involved the addition of line drivers on the A1, A2, and A3 boards in the DGIO cage. These drivers would receive data from the common bus prior to the gated DCVG line drivers and transmit this data to the RIB through spare backplane pins associated with these boards as shown in figure 6. The advantages of this plan are that it would not require the use of the spare A6 card slot in the DGIO, thus keeping it available for future DGU modifications. Also, it would not affect or modify the DGIO/DCVG interface. The main disadvantage is that it would require either the modification or replacement of the existing A1, A2, and A3 boards.

Plan C. As shown in figure 7, this plan involved eliminating the gating function of one set of DCVG bus drivers, thus making the associated bus an extension of the multi-DCVG bus within the DGIO. This would place data for all six DCVG's on this one output bus. The advantages of this plan are that it would be simple to implement (requiring only a few backplane wire changes), it would not require modification of existing boards, and it would not require the use of the spare A6 card slot. The main disadvantage is that it would diminish the noise reduction benefits gained through the use of gated drivers by eliminating this gating function for one DCVG.

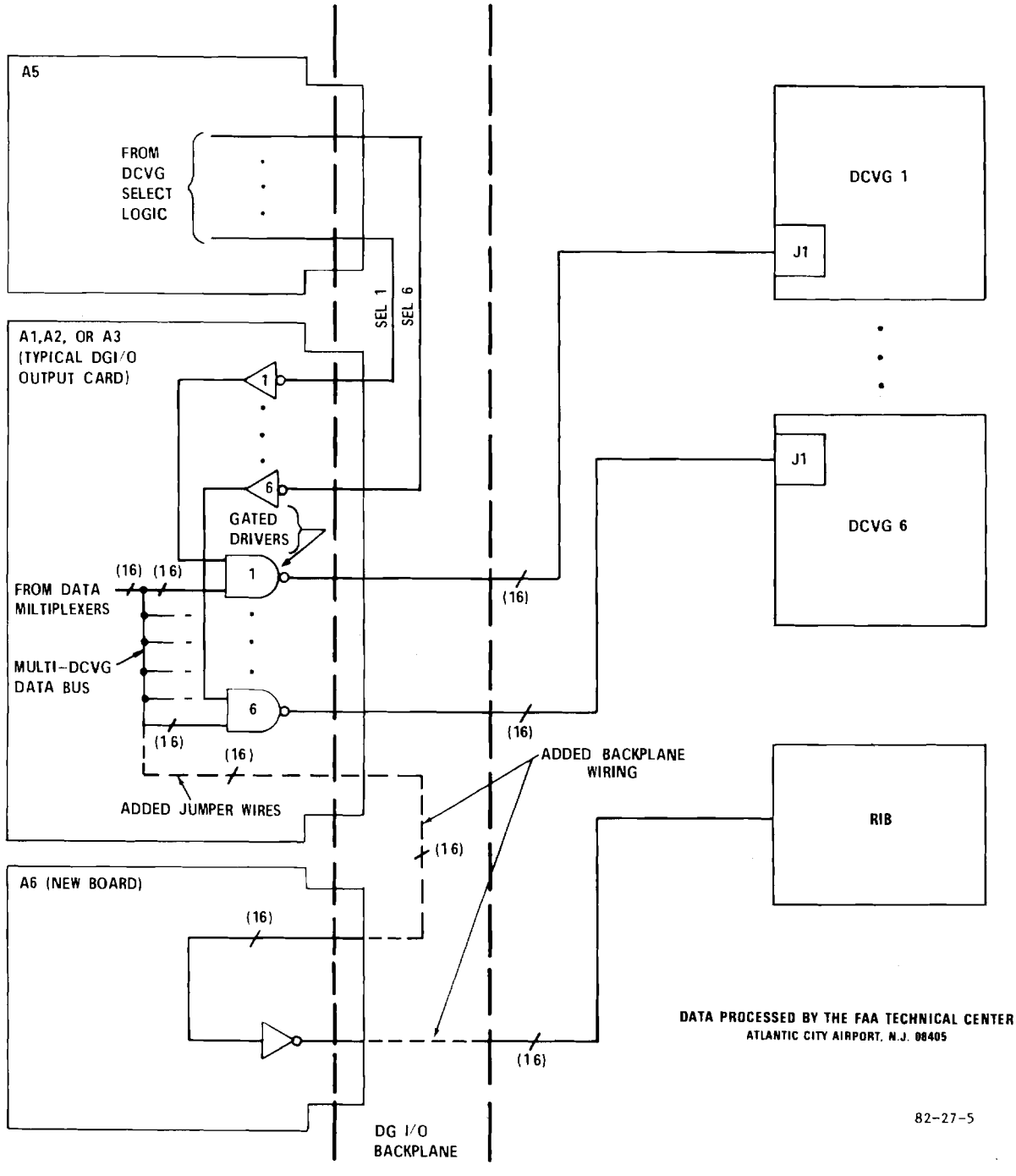


FIGURE 5. PLAN A BLOCK DIAGRAM

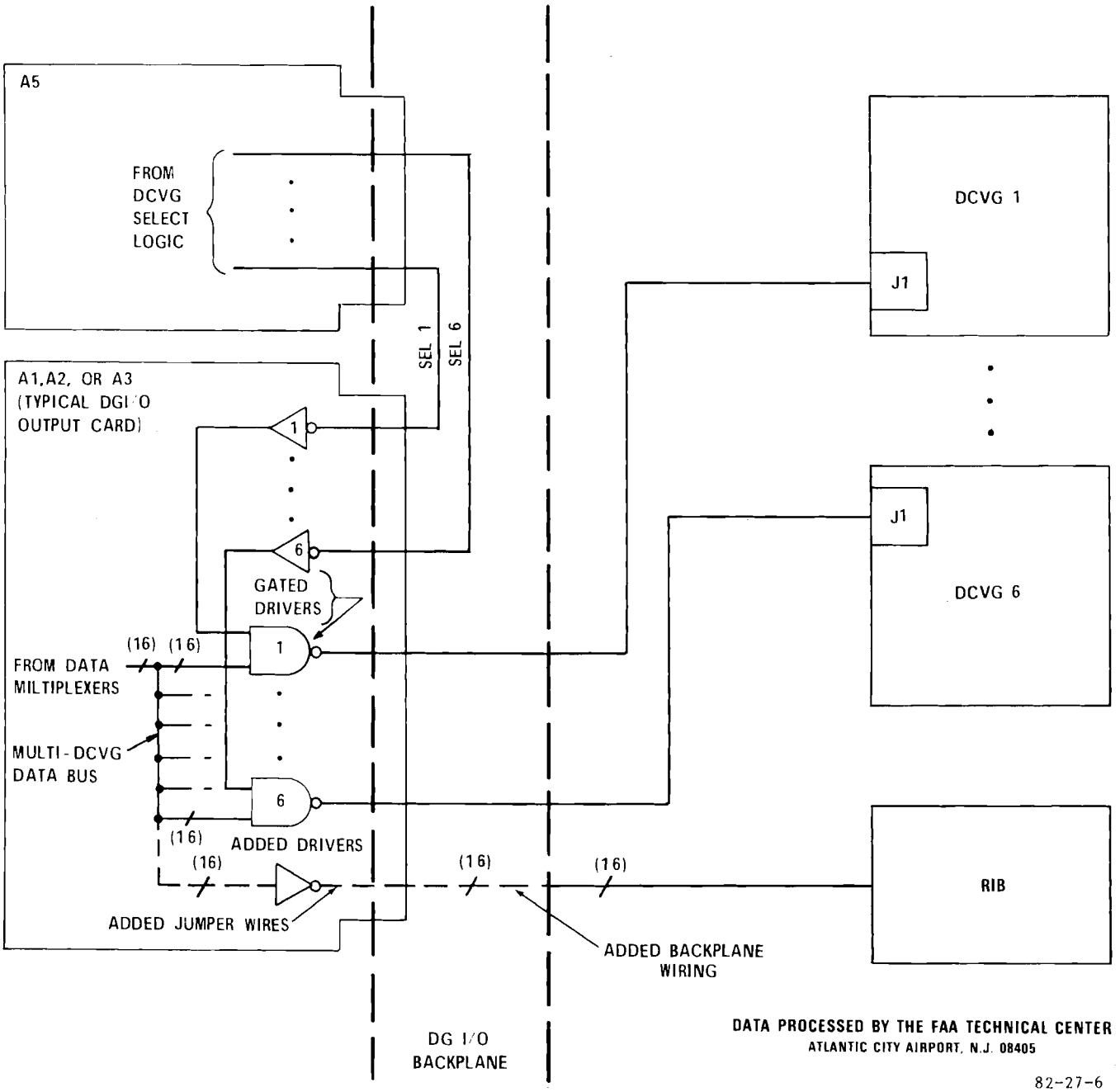


FIGURE 6. PLAN B BLOCK DIAGRAM

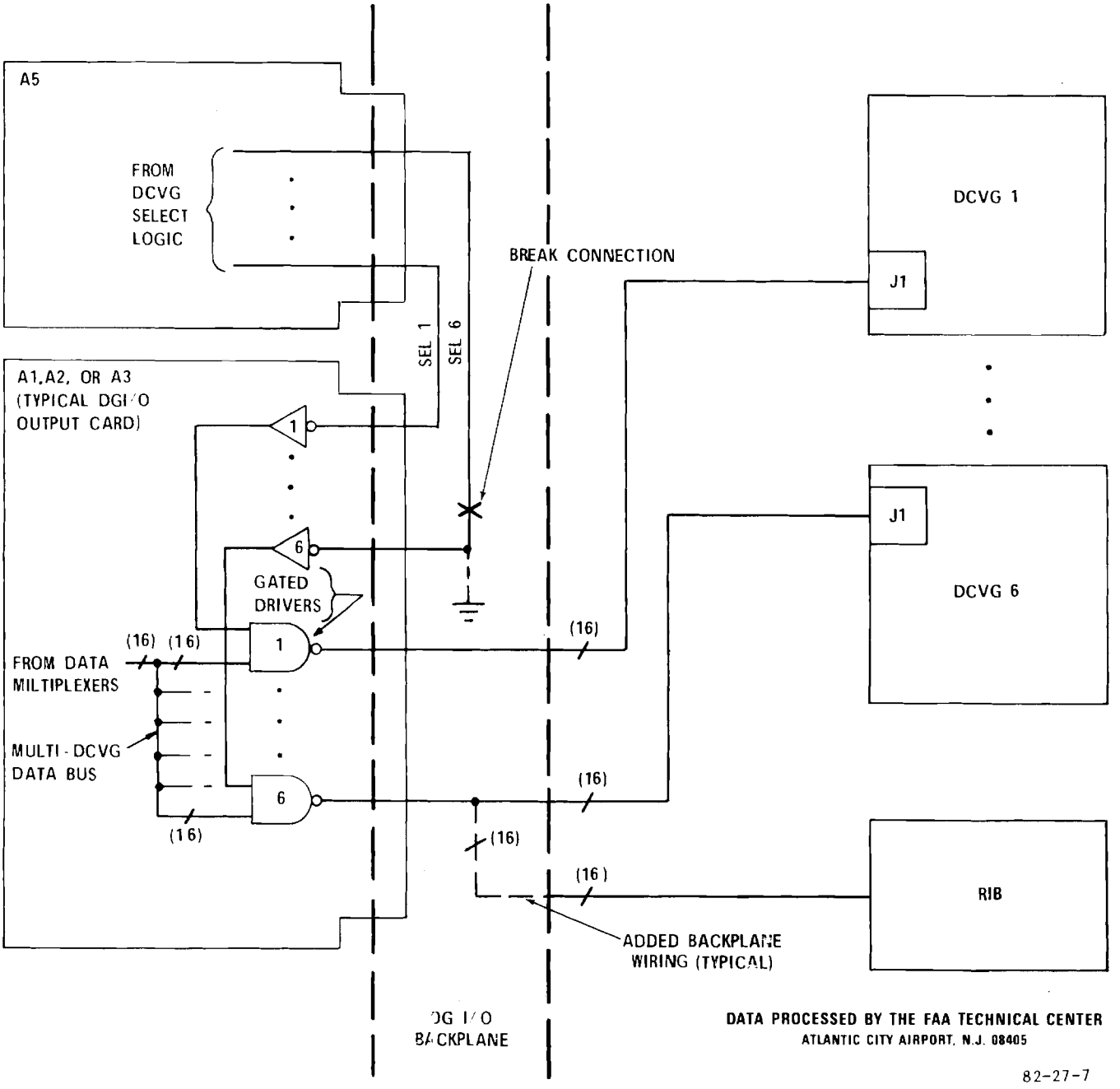


FIGURE 7. PLAN C BLOCK DIAGRAM

A meeting was held with representatives from the Airway Facilities Service (AAF-360) at the Technical Center for the purpose of discussing the record interface. It was decided that the use of Plan B for the engineering model was impractical. However, the Airway Facilities Service representatives indicated that this plan might be considered for the field implementation since some of these and other boards in the DGIO might be replaced with revised versions in the future. At that time, the record interface modification could be incorporated. They were opposed to Plan C, expressing a determination to avoid any plan which would eliminate the gating operation of drivers supplying data to even one DCVG. This left Plan A as the only viable option. However, through subsequent investigations, it was determined that the number of spare backplane pins for some of the boards was less than what was needed to accomplish Plan A. A reexamination of the problem resulted in a proposal that included modification and expansion of the concept presented in Plan C. This new proposal was the one that was finally adopted.

A detailed description of the resulting modification is given in appendix B of the System Design Data. The modification called for extending the multi-DCVG data bus by eliminating the gating function of the drivers for DCVG 6 and routing the bus to an additional set of line receivers and drivers on a new A6 board as shown in figure 8. These added drivers are gated using the same signal that was used to control the original DCVG 6 data bus drivers. The outputs of the line receivers on the A6 board now represent an extension of the multi-DCVG data bus which is distributed among the A1, A2, and A3 boards. A second set of line drivers on the A6 board is used to tap this extended bus and supply data to the RIB. In addition to these data drivers, other drivers were included on the new A6 board to transmit the other interface control signals required by the RIB. Since there were not enough backplane pins on the A6 slot to accommodate the three interface buses (one input bus and two output buses), the interconnection between the A6 board and the RIB was accomplished using two 50-pin connectors mounted on the outer edge of the A6 board. The number of pins on these two connectors was sufficient to allow the use of differential line drivers for the interface with the RIB. In addition to supplying a higher degree of noise immunity, the use of differential drivers provides the option of locating all RIB's external to the DG cabinet. This option was not exercised in the engineering model, but it provides the capability of meeting the requirement to place the Record Interface Equipment external to the DG cabinet in the field system.

The advantages of this plan are that (1) it would not require the modification or replacement of any existing DGIO boards, (2) all modifications to the DGIO would be made on the wire-wrap backplane, and (3) each DCVG input cable would continue to carry data for only one DCVG. The main disadvantage is that the existing data path to one DCVG (per DGU) would be physically, but not functionally, changed by the addition of the new A6 board which would become an integral part of the DGIO basket. This would add at least two additional stages of components in the interface between each DGIO and its associated DCVG 6. In addition to the A6 driver board, an A6 jumper board was specified that could be used in place of the A6 driver board to restore the original data path for DCVG 6.

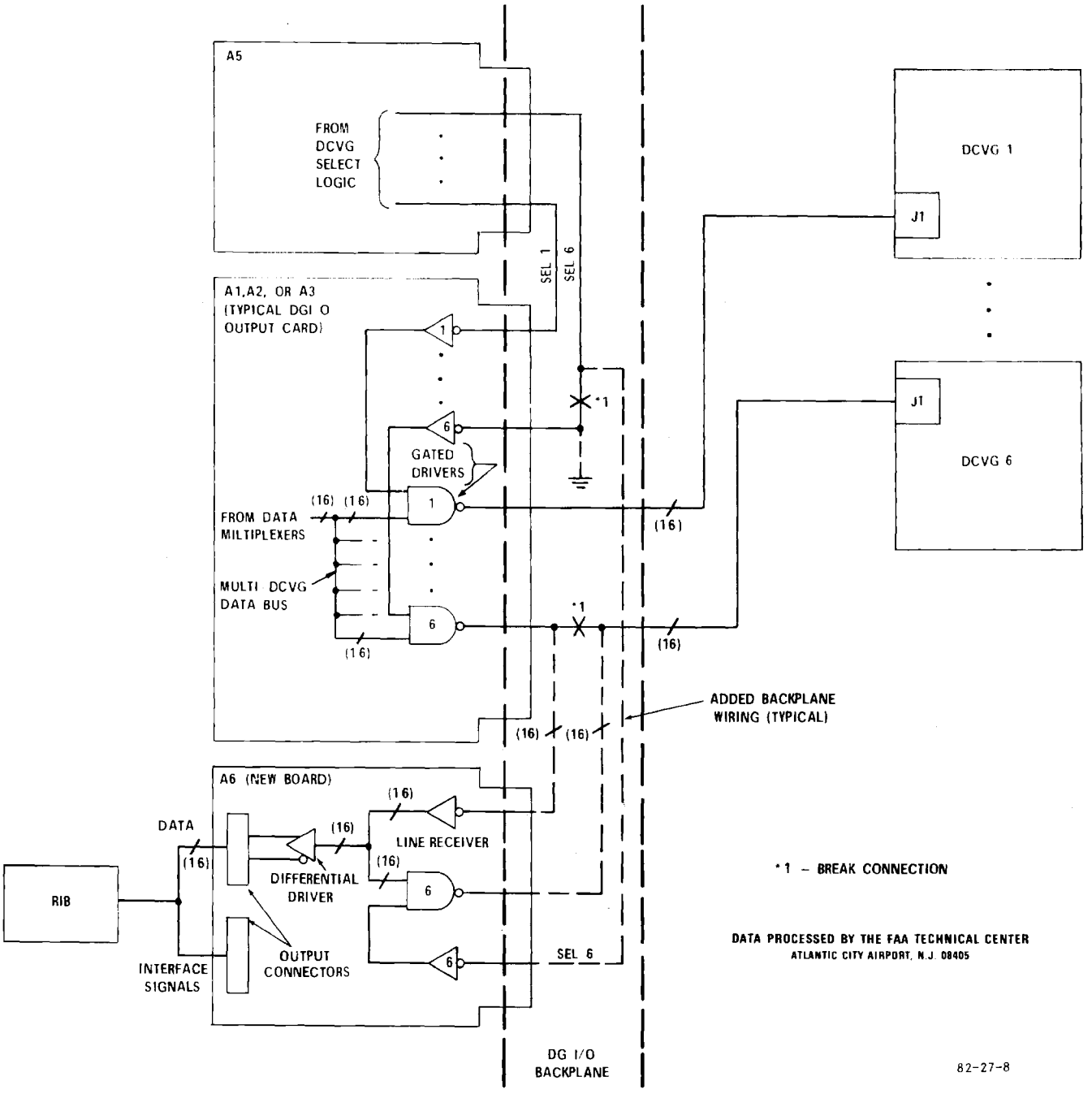


FIGURE 8. FINAL ADOPTED PLAN BLOCK DIAGRAM

This modification was installed and tested in six DGU's at the Technical Center and is presently in use in the ERDIRS engineering model. It is also included as part of the specification for the field system. However, it is suggested that the A6 driver board be revised to correct artwork and design errors that were discovered and corrected on each board during the tests performed with the engineering model. All modifications performed in the DG cabinets at the Technical Center were covered under Test NAS Change Proposal (NCP 5351A). Two DGU's, one on each display computer system at the Technical Center, were left unmodified at the request of Airway Facilities Service in order to retain the capability of testing future modification kits for the proposed field system.

RECORDER SELECTION. The basic requirements for the recording equipment were a 4-hour minimum record time, a high data storage capacity, a reusable storage medium, and the capability of providing continuous PVD data recording by switching to an alternate machine once the storage medium is filled. Also, it must be capable of recording and reproducing time-of-day (time code) information. The use of a magnetic storage medium appeared to be the most practical since it is reusable, relatively inexpensive, and a proven established product. To determine the required storage capacity, an estimate was made to determine the approximate quantity of data which needed to be recorded from the pick-off point. These computations were based on the normal data flow through the aforementioned interface between the DGIO and the DCVG(s). The record interface logic, which is located between the pick-off point and the recorder, operates in the sampling mode, periodically selecting and storing a complete refresh frame from each PVD from the data available at the pick-off point. An assumption was made that sampling one frame per second from a given PVD was satisfactory to produce an adequate reproduction of the original presentation. A second assumption, on which the calculations were based, was that the average PVD presentation at an active control sector position was comprised of approximately 1,000 DCVG words. Hence, a sample rate of one frame per second, with each frame consisting of 1,000 64-bit data words, provides a data rate of 64 kilobits per second for each PVD. Over the 4-hour minimum record time (14,400 seconds), the storage medium would have to store 9.2×10^8 data bits for a single PVD. One DGU (six PVD's) would require storage of 5.5×10^9 bits. This quantity is exclusive of any overhead bits added by the record interface logic or inserted internally by the recording device for sectoring, blocking, error checking, parallel deskewing, etc. The data quantities used in evaluating the following recording devices were exclusive of any overhead bits.

The various types of currently available magnetic recording devices were evaluated using the above criteria. The major sources of recorder information were published manufacturers' literature and contacts with manufacturers' representatives. Rigid and floppy disc systems, used extensively in the computer field, lacked sufficient storage capacity (3.2×10^6 bits per disc). As an example, one PVD could be recorded for 50 seconds on a single disc. Multiple rigid disc "stacks" would not significantly increase the storage capacity to a usable level.

The best magnetic medium appeared to be tape which offered more recording surface than a disc or disc stack. Digital tape recorders fall into two major categories: computer drives and instrumentation recorders. In considering these longitudinal multitrack recorders, it is assumed that the PVD data are distributed over all available tracks. Computer drives have a fixed maximum packing density of 6,250 bits per inch per track and utilize nine tape tracks. The storage capacity of a

standard 2,400-foot computer tape reel was calculated to be 1.6×10^9 bits. Using the aforementioned criteria, one PVD could be recorded on tape for approximately 420 minutes (7 hours) or one DGU for approximately 70 minutes. Instrumentation recorders are divided into several performance groups — Intermediate band, Wideband I and Wideband II — all conforming to Inter-Range Instrumentation Group (IRIG) Standards (IRIG 106-80). Each category has a different bandwidth capability and, therefore, a different maximum data rate and storage capacity per track. Each group is available in 7, 14, and 28 track configurations. At a tape speed of 7 1/2 inches per second, 9,200 feet of tape (14-inch reel) will record for approximately 4.1 hours. The following table summarizes their potential use in recording PVD data based on a 28-track recorder using a 9,200-foot reel of tape:

Category	Intermediate Band	Wideband I	Wideband II
Max Bit Capacity	3.1×10^{10} Bits	7.8×10^{10} Bits	1×10^{11} Bits
Number of PVD's (Max) at 7 1/2 inches per second	30	85	109
Number of DGU's (Max) at 7 1/2 inches per second	5	14	18

The quantities of PVD's and DGU's which can be recorded are calculated from published maximum data rates and do not include any overhead bits. This overhead decreases the usable data rate by 5 to 20 percent and therefore, reduces the number of PVD's that can be recorded. A more practical system would use lower data rates to avoid operating the recorder at its maximum limits.

Two instrumentation recorders can be interconnected to operate in a sequential mode and provide continuous PVD recording. In addition, the time code can be recorded on a spare track to provide time-of-day information. The Wideband II recorder exceeded the basic requirements for recording PVD data and was the type selected. Because of the high bit-packing density of the Wideband II recorder, it is commonly referred to as a high density digital (HDD) recorder.

The engineering model uses two 28-track Ampex HBR-3000 recorders which are Wideband II machines. A data rate of 222 kilohertz was selected which generates a packing density of 29.4 kilobits per inch at 7 1/2 inches per second. The engineering model is designed to record up to 36 PVD's (six DGU's); this quantity was later found to be quite conservative and could be easily doubled to 72 PVD's and still maintain an adequate PVD sample rate. Of the 28 tracks on each recorder, 24 tracks are used for the PVD data; one is used for time code; two are used internally by the recorder for parallel deskewing; one track is a spare. The two internally used tracks constitute the overhead in this recorder and result in an overhead figure of 7.7 percent.

ADDITIONAL RECORDER CONSIDERATIONS. Several operational aspects of the HDD recorders had to be considered in the ERDIRS application. These consisted of the bit error rate (BER), recording codes, track configurations, sequential mode operation, and head life.

Bit Error Rate. The BER is a figure that represents the average number data bits in error over a specified quantity of data bits. It is usually calculated by dividing the number of errors by the total number of data bits over a 100-foot section of tape. It is normally expressed in negative powers of ten; the smaller the number, the better the error rate. The HDD recorders currently available all have a published BER of one error in one million bits (10^{-6}) using standard magnetic tape. Since the major sources of data errors in HDD recording occur from scratches, debris, and other nonuniformities on the tape, or from dust or other particles (i.e., smoke, hair, finger oils, etc.) between the tape and heads, proper treatment of the tape, heads, tape path, and recorder environment can improve the BER to 10^{-7} or better. Use of certified instrumentation tape could further improve the BER.

Data errors are essentially random in nature and cannot be predicted. However, they can be analyzed by using probability and averaging techniques. At the maximum recorder data rate of 250 kilobits per second per track, an error could occur on each track every 4 seconds based on a BER of 10^{-6}. Considering that the average data rate per PVD is estimated to be about 64 kilobits per second, up to four PVD's could be recorded on a single track. Assuming an error occurs every 4 seconds, the probability of a particular PVD playback presentation experiencing two consecutive errors is 25 percent, with the playback data for the other three recorded PVD's being error free. However, over long time periods, with the errors evenly distributed among the four PVD's, each PVD would average one error every 16 seconds. If multiple tracks are used to record a group of PVD's, the number of errors occurring per unit time would increase as the number of tracks increases. However, the number of PVD's recorded would also increase proportionately so the probability and average frequency of errors discussed above would remain the same.

The BER is an average, and because of the nature of the causes of errors as mentioned above, it is expected (and has been observed) that many of the errors will occur in bursts rather than singly. This would indicate much longer periods between errors than that calculated from the average. Experience with the engineering model indicates that, when errors do occur, they usually affect only certain portions of the presentation. Since the presentation on the playback PVD is updated at the sample rate, any error will exist only until the next presentation update. It is considered improbable that two consecutive frames will have an error which will affect the same portion of the presentation. With this in mind, the BER specified by most HDD recorders manufacturers (10^{6}) is considered satisfactory for use with the ERDIRS.

Recording Codes. A second aspect of HDD recording is the use of recording codes for signal conditioning. Magnetic recorders are bandpass devices in that they have high and low frequency cutoffs. The bandwidth of the data to be stored on the tape must fit within this bandpass. Digital data containing long strings of logical 1's or 0's may not be recordable because the resulting instantaneous bandwidth could lie below the recorder bandwidth. Encoding the digital data through a fixed logic process constrains the data to the recorder's bandwidth. Decoding on playback restores the original digital data. There are many encoding/decoding techniques currently available. Among them are Randomized Non-Return to Zero (R-NRZ), Enhanced Non-Return to Zero (E-NRZ), and Miller Squared (M^2), along with variations of these codes. Each code has its merits and shortcomings, and one particular code may be better for a particular type of user data than the others.

The analysis of each code is lengthy and will not be covered in this report. However, each of the three codes mentioned above was emperically tested during the development of the breadboard model by using each for a short period, in conjunction with a recorder from four major manufacturers (one manufacturer used a combination of E-NRZ and R-NRZ). Each recorder used with the breadboard model recorded both "live" PVD data and computer-generated test patterns. No discernable difference between the performance of the codes was noted when the playback patterns were visually checked. Since the major parameters of the data to be recorded were the same in both the breadboard and engineering models, these codes were still considered acceptable for use in the engineering model. However, this should not imply that any of these codes will be acceptable for use in the field system, and the contractor should demonstrate compatability between his design and data format and the code selected.

It should be noted that there has been an ongoing attempt by concerned industry/user organizations to standardize on the HDD recording format in order to simplify recorder procurement and permit crossplay of tapes between machines of various manufacturers. Such standardization has greatly helped the computer tape drive field. The American National Standards Institute (ANSI) X3.B6 subcommittee has been working closely with the Tape Head Interface Committee (THIC) (a recorder manufacturer and user group) to establish standards for a HDD recording code and a parallel data deskewing format. To date, no standards have been adopted.

Recorder Track Allocation. A number of choices and tradeoffs are possible in the allocation of tape tracks to record data from a group of PVD's. These allocations determine, to a great extent, the design and quantities of the record interface logic units which perform the actual selection and sampling of PVD data from the pickoff points.

Track/PVD configurations could range from a configuration which would put a few PVD's on each track in a serial-only mode, to one which would put several DGU's in sequence on 16 parallel tracks. The more tracks used to record a fixed number of PVD's, the more data recorded per unit time, and hence, a faster sample rate can be obtained. Possible track assignments are 1, 2, 4, 8, or 16 track groups or "ports," with each port assigned to an individual record interface logic unit. As the number of tracks per port increases, so does the number of PVD's that can be recorded per port. Therefore, the number of ports required decreases so that fewer record interface logic units are needed. Also, it is desirable to minimize the amount of manipulation of the sampled PVD data by the record interface logic and the recorder. Based upon these two points, the 16-line parallel technique would seem to be optimum but, with 16 tracks used for data and one track used for time code recording, it leaves 11 unused tracks on a 28-track recorder. Several of the unused tracks in any configuration could be utilized for recording a code identifying the PVD and/or DGU associated with the data being recorded. Another use of these spare tracks could be in the area of error detection and correction (EDAC), which provides for the correction of some types of data errors.

In any parallel HDD recording (multiple track ports), the recorder electronics automatically inserts deskewing bits into the data supplied by the user prior to recording. These bits are used on playback to remove the variations in bit alignment which occur in recording and reproducing parallel data streams. The deskewing bits are stripped from the user data as part of the deskewing process, and only user data are provided at the recorder output. This deskewing process adds complexity to the recorder hardware.

Track allocations and the related configuration of the record interface logic appear to be a matter of engineering judgment, with the major trade-offs involving the efficient use of the recorder tracks, the simplification of the recorder hardware, and the minimization of the quantity of record interface logic units.

The configuration used in the engineering model utilizes a RIB for the record interface logic unit; each RIB is interfaced to a DGU (six PVD's) via the associated A6 boards. Four tracks are used by each RIB to record the sampled PVD data of each DGU. From the 28 tracks available, six 4-track ports are allocated to record PVD data, one track is used for the time code and two are used internally by the recorder for "master" deskewing. One track is spare.

Sequential Mode Operation. In both the engineering model and the proposed field system, the HDD recorders are required to operate in a sequential mode; i.e., as the active recorder approaches end of tape, the second recorder will begin recording, thus providing an overlap of recorded data. This overlap period is adjustable from 1 to 4 minutes, following which the first machine automatically rewinds its tape and goes to a standby status. The operator/technician can then remove the recorded tape for storage and thread a new reel of tape on the recorder. In addition to end-of-tape switchover, the standby recorder will come on-line whenever the active recorder becomes inoperative. Data are lost only for the short period of time between the occurrence of the fault and the standby recorder startup —- 2 to 3 seconds.

In the situation where a fully recorded reel of tape on the standby recorder has not been changed, an emergency automatic switchover will cause new data to be written over the existing old data. The old data would then be lost. However, the loss of the old data by overwriting is probably not as critical as the loss of new data that would result if overwriting did not occur. This is because the data at the beginning of the recorded reel would be at least 4 hours old, and it would seem that a serious incident occurring during this time period would have been reported so that the tape could be removed immediately after the incident or at least immediately after a full 4-hour run.

Another factor which must be considered when overwrite occurs is the quality of the new data that are recorded without the tape first being degaussed (erased). Instrumentation recorders, as a rule, do not have erase heads on the recorder. This is to minimize the possibility of accidental erasure of the data. Also, the high magnetic field generated by the erase head and erase oscillator could cause problems with the rest of the recorder electronics. For this reason, tapes are usually bulk-erased using an off-line degaussing unit. Conversations with recorder manufacturers have produced different opinions on how much, if any, degradation occurs in data which are written on a tape that has not been degaussed. In an effort to resolve this question, tests were conducted with the engineering model to determine the effects of overwriting data. The first series of tests involved the internal test circuitry of the recorder which wrote pseudorandom data on tape and performed a bit-by-bit check of the reproduced data. This circuitry is normally used to check the BER of the recorder, and it displays either the actual BER or the number of cumulative errors. These tests were performed over ten 100-foot sections of degaussed and cleaned tape. Pseudorandom data were first recorded and then checked during four playback passes to determine the number of errors in these sections of tape. Additional pseudorandom data were then overwritten on the same sections without degaussing. Four playback passes over the

same sections of tape were made to see if the numbers of errors were consistent. The overall result was that the errors in the overwrite data exceeded the errors in the original pseudorandom data; and in a majority of the overwrite passes, the errors exceeded the required BER of 10^{-6} (36 errors in 100 feet of tape at 122 kilohertz data rate). This series of tests indicated that overwriting of data may not be acceptable for the ERDIRS application. To verify the results, a set of subjective tests was performed in which live PVD data were recorded and visually monitored on playback using a PVD. The first recording pass was observed as it was being recorded using the read-after-write capability of the HDD recorder. Then a playback pass was used to visually verify the quality of the recorded PVD data. Following this, an overwrite was performed without degaussing and was visually reviewed during a playback pass. It was found that there was no discernable decrease in the quality of the presentation of the overwrite data as compared to the original data. Based upon these tests, it was determined that, although overwriting data does produce an increased error rate, the effect on the PVD data presentations due to overwriting appears to be minimal, as observed in the engineering model. A reason for the conflicting results of the two sets of overwrite tests may be that additional errors which may have existed in the second set of tests could have occurred in the display data for the other five PVD's in the port or in the overhead bits, neither of which affects the playback presentation. Another reason for the minimal effect on the playback presentation due to overwriting may be that the specified BER is too conservative. The recorders which were used for the tests used bias recording. A nonbias or saturation HDD recorder was not available for testing, so it was not possible to determine the effects of overwriting using this type of recorder. This means the use of overwriting in the field system may or may not cause degradation in the playback presentation, depending upon which recorder and data format is used. This indicates additional testing will be required during the development of the field system.

Even though the draft specification requires the field system to have the capability of overwriting in an emergency situation, the need for overwriting may never arise if a policy of replacing a tape at the end of each 4-hour recording run was adopted. If this was the case, it might be desirable to remove a recorded tape before it is rewound in order to reduce the amount of tape passing over the heads and, thus, extend head life. The usefulness or practicality of these procedures would depend on the available manpower at each site.

Head Life. The record and reproduce heads are a critical part of HDD recorders because they are the means by which data are transferred to and from the magnetic tape. They are also the part of the system which is most subject to wear. As the tape moves over the heads, the pole tips, which are the working surface of the heads, are very slowly worn down. On the average, the pole tips are only two to three thousanths of a inch (mils) deep, and once this depth is reached, the heads are at the end of their useful life. There are various engineering trade-offs which a recorder manufacturer considers in order to reduce the effects of wear. These include a choice of an optimum tape tension, and the selection of various head materials, such as alfasil, ferrites, and ceramics. There is evidence that the wear rate, in terms of the amount of wear per number of feet of tape passing over the head, may vary slightly with different tape speeds. The most important factors for the user to bear in mind in order to keep head wear to a minimum is to maintain a clean environment and a clean tape. Commercial equipment is available to clean and repack reels of tape.

Manufacturers' head-life warranties, which are usually conservative, range from 1,000 to 3,000 hours with standard head materials. With the new ceramic-tipped heads offered by one manufacturer, a warranty in the area of 5,000 hours may be obtained. These warranties also include an expiration clause of 1 or 2 years.

The engineering model recorders contained head assemblies which are normally warranted for 1,000 hours, unconditionally, and 3,000 hours, prorated. However, the specification to purchase the recorders for the engineering model required a head-life warranty of 2,000 hours, unconditionally, and 4,000 hours, prorated, to which the manufacturer agreed. This indicates that head-life warranties are negotiable, or more importantly, that the expected head-life is dependent upon the operating conditions imposed on the heads. Factors influencing the expected head-life include such items as tape tension, speed and type, and environmental conditions such as humidity, temperature, dust, etc.

In the field specification, the requirement for head-life warranty is specified in terms of the amount of tape passing over the heads rather than hours of operation. The figure of 23 million feet given in the specification is based on a calculation of the number of feet of tape that can pass over the heads in both the forward and reverse direction over a warranty period of 5,000 hours. This calculation was based on the use of 7 1/2 inches per second for recording and 240 inches per second for rewind. This figure is conservative because, if a fixed tape speed of 120 inches per second were used, the 5,000-hour warranty would equate to 180 million feet of tape passing over the heads. With alternating pairs of recorders operating continuously in the field ERDIRS, each recorder will take approximately 1 year to reach the specified warranty limit of 23 million feet. In order to verify warranty claims, each recorder is required to include a cumulative footage counter which counts the number of feet of tape passing over the heads in both directions. This is not a standard item in present off-the-shelf recorders. Normally, a running time meter, operating only when the tape is in motion, is used to verify warranty claims.

SAMPLING. Without a reduction in the amount of data to be recorded, the maximum data rate resulting from using a recorder tape speed of 7 1/2 inches per second would severely limit the number of PVD's that could be handled by a single recorder. In addition, the data rate at the ERDIRS record interface prohibits the direct real-time recording of data, hence requiring some interim storage for reducing the data rate prior to recording. Therefore, in order to minimize the amount of data to be recorded and to reduce the data rate, a sampling technique must be used. Since much of the data appearing at the ERDIRS record interface are redundant from a recording standpoint, sampling is feasible. In the display computer, a data base for each PVD is stored and updated nominally within 1.5 seconds. Target position data are updated once every 6 to 10 seconds depending upon the radar antenna scan rate. The display computer refreshes each PVD by sending a complete PVD presentation (frame of data) nominally 55 times each second. Since many of these frames are identical or change very little over a period of a few seconds, a sampling technique applied on a frame basis can be used to eliminate much of the redundant data while still capturing all essential changes in the data. An alternate technique was considered in which an initial baseline frame from each PVD would be sampled and recorded, and from then on, only that data which differed from the baseline data would be recorded. However, this technique was found to be impractical.

In the engineering model, each RIB samples a complete frame of data from each of six PVD's in sequence. The sample period is defined as the time during which all six PVD's are sampled once. This sample period is variable and depends upon the amount of data being sampled from each PVD in the sequence. The average sample period was estimated to be 0.32 seconds, based upon an average PVD presentation of 1,000 DCVG data words.

Sampling in the field system can be accomplished by using either a single sequence for sampling all the PVD's to be recorded or several parallel sequences among which the PVD's will be distributed. The choice depends upon the configuration and design of the Record Interface Equipment and the selected track configuration. As in the engineering model, the sample period is required to be variable, with the maximum sample period not to exceed 2 seconds. This maximum limit is considered to be an extreme case with the average sample period expected to be about 0.6 seconds. This increase in the expected average sample period from that of the engineering model is due to the fact that each field system recorder is required to record data for 72 PVD's rather than the 36 PVD's handled by the engineering model recorders.

PLAYBACK DISPLAY REFRESH AND UPDATE. In order to update the display on playback without interrupting the refresh operation, two blocks of memory are required. One block is used to store the frame of data that is currently being refreshed on the display, while the other is used to store an updated version of that frame. When the updated frame is completely stored, the blocks of memory switch roles. Both of the present en route display computer systems also use this general technique to update refresh data.

The engineering model is required to refresh and update two displays on playback. It uses two pairs of fixed-size memories, with each pair refreshing and updating a single display. The capacity of each memory is 3,072 DCVG data words, which is more than adequate to handle the heaviest traffic data loads. It is estimated that the average air traffic control display pattern consists of approximately 1,000 DCVG data words.

Even though there will be four displays used in the field system (see figure 4), two of the displays (which will be used to monitor the operational recording) will be sharing the same data. Therefore, there will be three independent data bases requiring refreshing and updating in the field system. Implementation of the engineering model technique using three pairs of fixed-sized memories would still be practical. The size and configuration of the memories can be adapted to the needs of the field system. A feature that was not incorporated in the engineering model but will be included in the field system is truncation, in the event of memory overflow. If during the sampling operation, the number of words to be stored in a memory exceeds its capacity, the data will be truncated at the point of memory overflow. The portion of the data sampled prior to truncation will be recorded and subsequently used for refreshing a display on playback, while that which follows the truncation will be ignored. During both recording and playback, the operator will be notified when an overflow/truncation condition exists (see appendix B, paragraph 3.2.1.1.1.3 and 3.2.1.2.2.1).

SECTOR SELECTION ON PLAYBACK. A means must be provided on playback to enable an operator to select which of the recorded PVD presentations are to be reproduced. To accomplish this, a code word must be recorded with the data to designate on playback from which sector the data were recorded.

In the engineering model, display data selection is performed on a port/DCVG basis. Each port corresponds to the sampled data from a single DGU (six DCVG's). Hence, data selection is equipment, rather than sector, oriented. In order to select data from a particular sector, a user must know the DGU and DCVG associated with that sector. A code word, generated by the RIB and recorded with the data, identifies each of the six DCVG's associated with a port, while the DGU is identified by selecting the appropriate port. Although this is adequate for the limited engineering type model used at the Technical Center, it would be unsuitable for use in the field because of the possibility of error and confusion. Therefore, the specification for the field system requires controls enabling an operator to select display data on a sector basis. The code word used in the field system could consist of either the sector number or a code designating the DGU and DCVG associated with the sector. In the latter case, the Playback Interface Equipment must be capable of automatic correlation between sectors and equipment so that data can be selected by designating the sector number only. In either case, the Playback Interface Equipment must be capable of selecting data from a particular sector whether those data were originally displayed using the active DGU/DCVG or, in case of reconfiguration, the spare DGU/DCVG.

PLAYBACK/MONITOR DISPLAYS. It is a general requirement of the ERDIRS that the reproduced data will be displayed on the same type of displays as was used to present the original data. The engineering model used two dedicated off-line PVD's, with two off-line DCVG's, operating for the single purpose of displaying ERDIRS data in either the monitor or playback mode.

Each field installation will require two PVD's for monitoring the recording operation and two PVD's for playing back data. The need for two independent pairs of displays is due to the fact that the monitor and playback functions are two separate and independent operations that could occur simultaneously. Each display that is used for playback requires one off-line DCVG since these displays are required to operate independently. The two displays used for monitoring will share a single DCVG. Hence, three off-line DCVG's will be required at each field site.

There are not enough spare PVD's available to fill the ERDIRS requirements for the 20 existing en route centers, and the cost of supplying the PVD's needed would be excessive. Therefore, the field specification calls for the use of four existing PVD's in each ARTCC to be used as dual purpose displays. Three of the four displays will receive their input data from multiplexer units supplied with the ERDIRS. These PVD Input Multiplexer Units (PIMU) will allow each display to operate independently in one of two modes. The first, called the normal mode, would provide the data that are normally sent to the display; the second, called the ERDIRS mode, would provide ERDIRS data to the display. One of the displays which will operate using a PIMU will be the SMMC PVD. When it is placed in the ERDIRS mode, this display will be used to monitor the record function. The other two displays operating with multiplexing units will be training displays designated as playback positions. The fourth display needed to meet the ERDIRS requirements will be the maintenance PVD located in the equipment area which will be used for monitoring when operating in the ERDIRS mode. This display will not use a multiplexing unit but will be switched between the normal and ERDIRS mode by disconnecting and reconnecting its input cable. Recabling is an operation normally associated with this display.

The design of the PIMU can take one of two forms. One form would be mechanical, which would include relays and switches. The other form would be electronic switching. Because of the number of data lines (30 twisted pairs) to be switched, the use of a single switch might prove impractical, even though it would require no power to function. The use of relays might be more practical and could provide a fail-safe operation. This is due to the fact that a two-position relay has a rest position (coil deactivated) and an active position (coil activated). The rest position could be used to designate the normal mode for a PVD, so that whenever the PVD is operating in the normal mode, it would be immune to any PIMU power failures. Since the normal mode is the primary mode for the PVD, this is a desirable feature for the PIMU. It should be noted that even if electronic switching was employed and the PIMU should fail, the PVD could be recabled into its original configuration. Also, a failure in the PIMU would only affect the SMMC PVD or a training PVD, neither of which is normally used to control live aircraft. In addition, this unit is required to use a minimum of space and power and have a high reliability. The control of the PIMU will be incorporated in the remote control unit at its associated ERDIRS position.

TIME SYNCHRONIZATION. Time synchronization is the method by which information simultaneously recorded on two or more tapes is reproduced, maintaining the original timing relationship. This is accomplished by recording a time code on each tape and using this information on playback to vary the tape speeds of one or more of the reproducers in order to realign the reproduced information. Time code readers are used to display the recorded time and provide the signals needed by the time synchronization circuits. It is possible for reproducers to be synchronized to within 1 second of each other using available techniques. The use of time synchronization in the field ERDIRS would permit the simultaneous playback of air traffic control PVD presentations and associated voice communications. In order to accomplish this, the specification requires that the operational reproducer and/or the training recorder must be capable of being synchronized with the High Capacity Voice Reproducer (HCVR). In addition, the operational reproducer and the training recorder may be synchronized with each other without the HCVR, as in the case where two PVD data tapes are to be reproduced simultaneously when no voice playback is required. Since the HCVR is a commissioned equipment, it seems more practical to leave this equipment unmodified and treat it as the master unit.

The time code utilized by the recorders is generated by the Coded Time Source (CTS) equipment located at each ARTCC and at the Technical Center. The time code is a modified IRIG-E serial code using a 600-hertz sine wave carrier rather than the standard 100 hertz carrier. The continuous carrier is amplitude modulated to encode the time information. The encoding contains hours, minutes, and seconds information with new time information updated every 10 seconds.

In the engineering model, a spare direct record track on the HDD recorders is used to record time. The time code reader used to display the recorded time-of-day must be capable of using a time code reproduced at normal speed (7 1/2 inches per second) or at higher speeds (up to 240 inches per second), in either the forward or reverse direction. The higher speeds are used when searching for a specific event on tape. The serial time code is decoded by the reader, converted to parallel binary-coded decimal (BCD) format, and used to drive the time display on the front panel of the reader. Synchronizing one or more reproducers (slave units) to another reproducer (master unit) can be achieved very readily by utilizing the BCD time code from each time code reader. The BCD code from each slave is digitally

compared with the code from the master, and a digital difference signal is produced. This relative time difference is then converted into an analog voltage via a D/A converter and filtered to eliminate noise and sudden conversion changes. This analog voltage is used to control the frequency of a voltage-controlled oscillator (VCO) which is used to determine the tape speed of the slave reproducer. This VCO is used in place of the internal servo reference oscillator which normally determines the speed of the slave reproducer. The center frequency of the VCO is selected to be the same frequency as this servo reference oscillator. By using the VCO output as the tape speed reference in place of the crystal-controlled reference, the speed of the slave reproducer can be varied as to minimize the relative time difference between the tapes. When two display data playback reproducers are to be slaved to the HCVR, each slave must do its own time comparison and adjust its own VCO to attain synchronization with the master HCVR.

Time synchronization was not incorporated in the engineering model at the Technical Center. However, some breadboarding of the synchronization circuitry was done but was not completed due to resource limitations and an inherent equipment problem. Since no HCVR was available at the Technical Center, the intent was to synchronize the two HDD recorders to each other on playback. The time code readers used in the engineering model were Systron-Donner Model 8030's which are capable of reading a reproduced time code over varying tape speeds and in either direction. However, they had a problem in reading time code data reproduced by the Ampex Recorder due to a modulation anomaly ("glitch") inherent in the signal generated by the CTS. This modulation glitch caused no error when reading the time code directly from the CTS, but a low-frequency phase shift in the direct-reproduce electronics of the HDD recorder shifted the glitch to a point where it caused a 1-second readout error every 10 seconds. Experimentation using a borrowed time code reader produced by a different manufacturer resulted in an error-free time code reading indicating that not all readers are sensitive to this condition. After examination of the problem, it became apparent that the use of FM record/reproduce electronics for time code recording would eliminate the shifting of the glitch, thereby rendering the Systron-Donner time code readers usable. However, due to resource limitations, no FM record/reproduce electronics were purchased for use with the recorders.

PLAYBACK, MONITOR, AND TRAINING CONTROLS. Two PVD's are dedicated for use in the engineering model and are located in the same area as the recorders and playback equipment. Hence, there was no need to provide remote controls at these displays for use in controlling the recorders and playback equipment.

In the proposed field system, the monitor and playback functions will be separate and independent and will be performed using two pairs of displays, one for monitor and one for playback. These displays will be used to perform the dual function as previously described and, with the exception of the maintenance display used for monitoring, will not be located close to the playback/monitor equipment. Because of the distance between the playback equipment and the displays, the controls for both the playback/monitor equipment and the recorders must be remoted to the displays. The required controls are listed in the specification and are similar to those used in the engineering model except that the field system controls must include the addition of the normal/ERDIRS select switch and, in the case of the two playback positions, synchronization and recorder controls. The controls for use with the maintenance PVD will be located with the playback/monitor equipment and will not include the normal/ERDIRS select switch.

As previously described, the SMMC PVD and the maintenance PVD, when being used for monitoring the recording operation, will be driven by a common off-line DCVG. Therefore, only one recorded display can be monitored at a time. Since both displays can be used to monitor the data simultaneously, priority will be given to the SMMC position for data selection.

The two displays used for playback are driven by separate DCVG's. Operators at these two positions can, therefore, select data independently. The controls used for playback will be the same as those used for monitoring with the addition of controls for synchronization and for operating the operational reproducer and the training recorder. The controls for the training recorder will also provide control of recording training data. Control of the synchronization unit and the recorders will be given to a position on a first-come, first-served basis with a lockout feature that prevents interference from the alternate position.

In general, these controls will be designed for easy attachment and detachment in order to facilitate PVD maintenance and replacement. The control units shall contain indicators for displaying all selections made at each position and for indicating which position is in control of the time synchronization unit, the operational reproducer, and the training recorder.

ERROR AND STATUS MONITORING. The purpose of this section is to discuss the methods of presenting and evaluating error and status information in the engineering model and in the field system. The types of error and status conditions monitored in each system are given in the System Design Data (appendix A) and the Field Specification (appendix B).

The presentation of error and status information in the engineering model is limited to a real-time indication of individual error and status conditions. In the Record Element, error and status information is sampled at various points within the RIB. These data are displayed at the RIB and are also used to form a status word which is sent serially on a separate data line to the RISP for display. The serial data rate is such that a status word is sent every 144 microseconds. This limits the rate for sampling error and status information to approximately 6,944 samples per second. Error conditions which occur momentarily between samples are temporarily stored in the RIB until the next sample so that such information is not lost. The information in each status word is stored and displayed at the RISP until the next status update is received.

In the Playback Element, there is an indicator panel located just above the two EPI's in the EPIC which provides an instantaneous presentation of error and status information concerning both EPI's. The error detection circuits in the EPI are designed to detect each error condition as it occurs, but only the first occurrence of each type detected in a given frame of data is indicated. Each error is stored and remains indicated until the start of the next frame. Some error and status conditions, such as memory overflow and asynchronous refresh, are indicated directly without storage.

In the engineering model, the indicators in both the Record and Playback Elements are not intended to give a quantitative measurement of the error and status conditions. They were designed to give an indication that certain error and status conditions are present within various parts of the system. Depending upon the frequency and persistence of different error and status conditions, an operator can make a subjective judgment as to the operational status of the equipment.

In the field system, two types of indicators are specified. The first type is a momentary indicator which will reflect the instantaneous real-time occurrence of each error and status condition. This indicator will show each error and status as it occurs and will be used to pinpoint which equipment is operating or malfunctioning. The second type of indicator is a resettable latching indicator which will be used to capture and store momentary error and status conditions which occur when an operator or technician is not present. The latter set of indicators will hold the information indefinitely until they are reset. In addition to error and status conditions, certain hard failure conditions will be indicated which were not indicated in the engineering model. Also some error and status conditions could be recorded with the data in order to provide some indication on playback of problems encountered by the recording subsystem which might impact the reliability of the playback presentation. However, the specification only calls for recording information concerning any memory overflow condition resulting in a truncation of a frame of data by the recording subsystem. The recording of system status information described below may be added as a requirement in the future.

Instead of depending on subjective judgment to determine system status, as is the case in the engineering model, the specification for the field system calls for the processing of error information for all equipment in order to derive system status on a quantitative basis. This processing consists of the following general procedure. First, the occurrences of each type of error condition will be counted per unit time (sample period). Second, each count will be multiplied by a weighting factor to determine an associated error rate figure. Each weighting factor will be derived specifically for each error condition, depending on how the error condition affects the system performance, and will be adjustable at each site. Next, all error rate figures from the various error conditions will be added together to form a total error rate figure for all equipment. At this point, additional factors may also be added or subtracted to compensate for interactions between error conditions. The total error figure for all equipment is then compared with two adjustable threshold levels. If the total error rate figure is less than the first threshold level (level 1), the equipment is considered to be in an operational state; if it lies between level 1 and the second threshold level (level 2), the equipment is considered to be in a degraded state; finally, if it lies above level 2, the equipment is considered to be in a failed state. This system status information is updated at the end of each sample period. There are three indicators assigned to each piece of equipment for use in displaying system status. These indicators are located with the equipment. Duplicate indicators are also provided at the SMMC. This type of system status is more accurately defined than that derived from a subjective appraisal of the error and status indicators. It allows each and every error condition detected to contribute towards the determination of system status. It also provides a means of balancing the effects of different error conditions occurring simultaneously and provides a means of determining the total effect of any combination of error conditions on the system status. It should be noted that there are certain failure conditions that will override the calculation of system status. These conditions include power supply failures, tape breakage, overtemperature, etc.

The following hypothetical examples will illustrate the anticipated procedure for deriving field system status information from error information. In these examples, the system status information will be derived for a hypothetical piece of equipment where it is assumed that only three types of error conditions contribute

towards the calculation of system status (EC_1, EC_2, and EC_3). It is also assumed that these three conditions do not interact with each other. To determine the system status based on the number of errors occurring in the three categories, an equation must be defined that combines the number of errors in each category to form a total error rate figure for the equipment. This equation could take a form as follows:

$$ERF_T = ERF_1 + ERF_2 + ERF_3 \quad (1)$$

$$= W_1 E_1 + W_2 E_2 + W_3 E_3 \quad (2)$$

Where ERF_T = Total error rate figure

ERF_i = ERF for condition EC

E_i = Number of errors counted per unit time for condition EC

W_i = Weighting factor associated with condition EC

The constants, W_i, are determined as follows: First, define the threshold limits against which ERF_T is compared in the determination of system status. For this example, level 1 (L_1) will be arbitrarily selected as 50 and level 2 (L_2) as 100. Next, subjectively determine the quantity of errors in each condition type that constitutes a degraded and failed state when taken individually. For the first example, the following values will be assumed:

	EC_1	EC_2	EC_3
E_i at degraded level (D_i)	25	5	10
E_i at failure level (F_i)	50	10	20

In order to calculate W_1 let

$ERF_T = L_1 = 50$

$E_1 = 25$ (degraded level)

$E_2 = 0$

and $E_3 = 0$

in equation (2) as follows

$$50 = W_1 (25) + W_2 (0) + W_3 (0)$$

This yields a value of 2 for W_1. Using L_2 instead of L_1 for ERF_T and using the failure level for E_1 in place of the degraded level will yield the same value for W_1. This indicates that a constant value for W_1 is adequate for this error condition. However, this will not always be the case as will be shown in a later example. If a similar procedure is followed for determining the other two weighting factors, it will be seen that they also are constants and have the values $W_2 = 10$ and $W_3 = 5$. Equation (2) therefore becomes

$$ERF_T = 2E_1 + 10E_2 + 5E_3 \qquad (3)$$

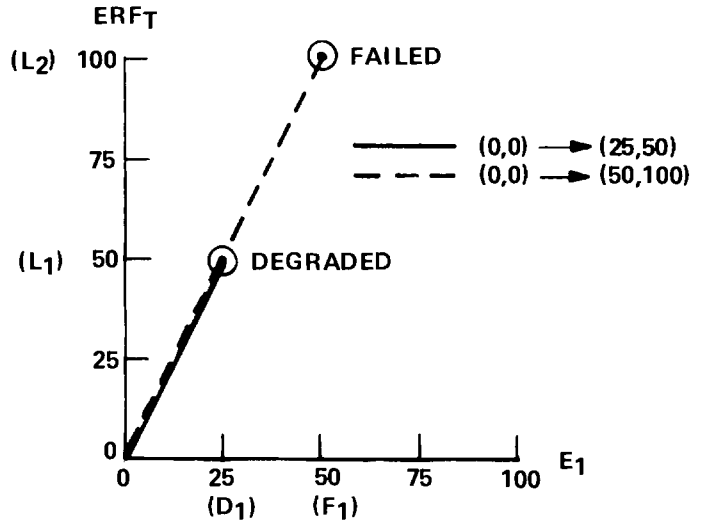
From the derivation of the weighting factors, it can be seen that if only one type of error occurs within a sample period, then, through the weighting process, the degraded and failure levels for that particular type of error condition becomes equivalent to L_1 and L_2, respectively. Also, it can be seen that five errors of the type EC_1 are equivalent to one error of the type EC_2, etc., so that when errors of more than one type are detected, they are combined to form an appropriate ERF.

Consider the following sample data:

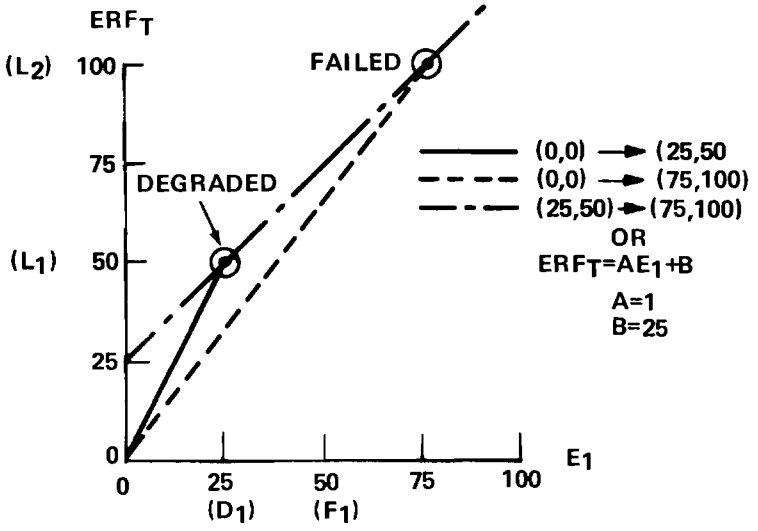
Sample Number	E_1	E_2	E_3	ERF_T	System Status
1	24	1	0	58	Degraded
2	24	4	9	133	Failed
3	4	2	4	48	Operational

The last two columns are based on the use of equation (3) with $L_1 = 50$ and $L_2 = 100$. In sample 1, it can be seen that if the single EC_1 error did not exist, the number of EC_1 errors alone would not be enough to place the equipment in the degraded state. In sample 2, even though each individual error condition is one short of independently causing a degraded state, together they push the equipment beyond the degraded state into the failed state. The final sample illustrates the equipment in the operational state but close to the degraded state.

The previous example was designed to use simple numbers and simple relationships and was used primarily to illustrate the effectiveness of counting, weighting, and summing errors to determine system status. The following example illustrates some considerations involved when the relationships become more complex. The primary relationships of concern are those between the individual levels for degraded and failure and the threshold levels L_1 and L_2. For example, if the relationship between the levels for EC_1 and L_1 and L_2 are plotted and a line is drawn from the origin to each of the two points (degraded and failed), the following plot is obtained:



It should be noted that both line segments have the same slope. Using this slope as the weighting factor W_1, the relationship between E_1 and ERF_T is linear and ERF_T is equal to zero when E_1 equals zero. If, however, the individual failure limit for EC_1 is changed to 75 instead of 50, the following plot is obtained:



In this case, the slopes are not equal. A linear equation of the form $y = A\,x + B$ could be used to relate ERF_T (the y term) with E_1 (the x term) with "A" equaling the slope of the line drawn between the points representing degraded and failed. It should be noted, however, that the "B" component of the equation, while required for satisfying the equation at both the degraded and failed points, causes the equation to yield a nonzero ERF_T when E_1 is zero. This is obviously unacceptable. In order to overcome this difficulty, a weighting factor of the form $W_1 = a_1\,E_1 + b_1$ can be used resulting in the following equation relating ERF_T to E_1:

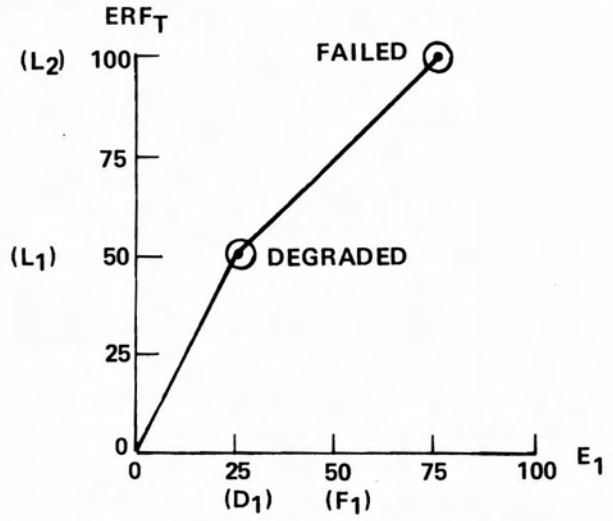
$$ERF_T = (a_1\,E_1 + b_1)\,E_1 \tag{4a}$$

$$= a_1\,E_1^2 + b_1\,E_1 \tag{4b}$$

Using the values for L_1, L_2, and E_1 for degraded and failed, a_1 and b_1 can be calculated producing the following equation relating ERF_T and E_1:

$$ERF_T = \frac{1}{75}\,E_1^2 + \frac{175}{75}\,E_1 \tag{5}$$

With this equation, the contribution to the ERF_T from EC_1 is zero when E_1 is zero. An alternative to this nonlinear approach would be to relate E_1 to ERF_T by a piecewise-linear function consisting of two line segments with one drawn from the origin to the degraded point and the other from the degraded point through the failure point as illustrated below:



However, the use of a nonlinear or piecewise-linear weighting factor could be eliminated if the error due to the "B" term in the linear expression can be reduced to a point where it is considered insignificant. This might be accomplished by a careful choice of L_1 and L_2; but when many types of error conditions are used to determine system status with all of their weighting factors being dependent on the choice of L_1 and L_1, choosing an optimum L_1 and L_2 may not be a simple task. It is for this reason that the individual and total threshold limits for the degraded and failed states are required to be site-adjustable so that optimum values can be determined from field experience. Thus, the choice between linear and nonlinear weighting factors will also be based upon field experience.

Another factor which must be considered concerns the interactions between different types of error conditions. For example, a missing clock pulse could cause a corresponding parity error. Error detection circuits should be designed to minimize such interactions. A further consideration concerns the probability that an error detection circuit will miss an error. For example, in the case of checking for an odd parity condition, usually there will be a circuit which will examine a group of bits to determine if the number of bits in a logic one state is odd or even. The circuit will then add a parity bit whose logic state will ensure that the total number of logic one states is odd. This modified group is then checked at various points and an error condition is declared whenever the number of bits in a logic one state is even. It can be seen that whenever an odd number of bits in the modified group are in error, an error condition will be declared. However, if an even number of bits are in error, the circuit is incapable of detecting these errors because the number of bits in a logic one state will remain odd. In order to compensate for this deficiency, either a more elaborate detection circuit could be developed or the weighting factor could be adjusted to include a factor related to the probability that an even number of bits are in error in a group of bits under test. Even in the case of an odd number of bits in error, the declared error condition does not provide any information regarding the exact number of bits within the group that is in error. For instance, if the number of bits in a group, including the added parity bit, was 64, the detection of a parity error could exist when the number of bits in error is as few as 1 or as many as 63. However, if the bits within this group are interrelated to the point that even a single error would warrant the rejection of the whole group, a single error condition would be adequate to represent any number of errors in a group. The process of counting, weighting, and summing will provide a standard, accurate means of determing system status without depending upon visual interpretations of the indicators. However, the levels designating a degraded or failed state will still be subjectively derived. This fact should be kept in mind when making a decision concerning the complexity of the equipment performing error and status monitoring.

It should be noted that this discussion was based on abstract examples because data directly applicable to this discussion were not collected from the engineering model.

BUDGETARY ANALYSIS. A cost estimate for implementing the field version of the ERDIRS at 21 sites was set forth in a document called "Budgetary Estimate to Design, Develop and Fabricate the ERDIRS Field Version in Production Quantities" dated April 1980. This cost estimate was based on the field configuration which was approved by Airway Facilities Service representatives at a meeting in Washington, D.C., held in April 1979. This configuration is the one described in this report and consists of the following items per site:

- 3 High Density Digital Recorders
- 1 High Density Digital Reproducer
- 1 Record Interface Equipment
- 3 Playback Interface Equipments (two used for playback; one for monitor)
- 1 Time Sync Unit (containing three time code readers)
- 3 DCVG's
- 3 Remote Control Units
- 120 Reels of tape (20 day supply)
- - Tape Racks

The following is a summary of the cost estimate taken from the budgetary estimate document:

Engineering	$ 600,000
Hardware	7,079,100
Installation/Checkout	210,000
Documentation	250,000
Spare Parts	1,281,000
Total Cost	$9,420,100
G&A at 10%	942,010
Subtotal	$10,362,110
Profit at 10%	1,036,211
Total Net Contract Cost	$11,398,321
Required GFE	462,000
Total Cost of Implementation	$11,860,321

This cost estimate is based on the initial implementation of a full system at 20 ARTCC's and at the Technical Center. However, should financial restrictions be a problem and if a minimal system would suffice for a period of time, then the procurement could be accomplished in two phases.

The first phase would include engineering costs and the cost of procuring the minimal amount of equipment needed for the record operation. This minimum configuration consists of the following:

2	High Density Digital Recorders
1	Record Interface Equipment
1	Playback Interface Equipment (used for monitor or playback)
1	DCVG
1	Remote Control Unit
120	Reels of tape (20 day supply)
-	Tape Racks

With this configuration, the system could record 72 displays continuously with each tape being stored for a suggested period of 20 days before reuse. This configuration would not be capable of independent off-line recording of training data and would be restricted to playing back data from one display only. The standby unit of the recorder pair would be required for playing back data. However, this would also restrict its availability for sparing the on-line recorder.

The cost figures for this initial phase based on the figures given in the budgetary estimate are summarized as follows:

Engineering	$ 600,000
Hardware	4,004,700
Installation/Checkout	105,000
Documentation	225,000
Spare Parts	966,000
Total Cost	$5,900,700
G&A at 10%	590,070
Subtotal	6,490,770
Profit at 10%	649,077
Total Net Contract Cost	7,139,847
Required GFE	336,000
Total Cost of Initial Phase	$7,475,847

The estimated cost of implementing the second phase procurement would be $4,384,474, although some additional cost could be incurred due to the two-phase procurement.

The overall cost of implementing the system could be reduced if several trade-offs were employed. For instance, if the design allowed the on-line DCVG's associated with the training PVD's to process either normal display computer data or ERDIRS playback data, the need for three off-line DCVG's per site would be reduced to one, thus saving a total of $126,000.

Cost savings could also be realized by reducing the quantity of tape used. One way would be to reduce the storage time for the tapes. The specified quantity (120) is enough to provide 20 days of continual recording before the supply is exhausted and reused. However, the intent is to use 90 for operational recording and 30 for training recording. By cutting the storage time in half, a total of $126,000 could be saved. Another way would be to double the record time to 8 hours on each tape. This would require increasing the maximum sample period to 4 seconds (double the present 2-second maximum) in order to record the same number of PVD's. Thus only half the quantity of tapes would be needed for the 15-day archival storage time, with a savings of $126,000. If both techniques were used, only 25 percent of the original quantity would be needed, thus saving a total of $189,000.

Additional savings of $1,270,500 could be accomplished by eliminating the operational reproducer. However, this would mean that in order to perform tape duplication, the standby recorder would have to be used in place of the operational reproducer. It would also prohibit the off-line recording of training data while the training recorder was being used to playback operational data. If it was decided that the minimum system configuration would be sufficient and the Phase II effort would be eliminated, savings of up to $4,384,474 could be realized.

Along with the cost of initial procurement is the yearly cost of operating and maintaining the system. In the area of maintenance, the reliability requirements, as stated in the specification for each equipment group, are as follows:

	Mean Time Between Failures	Mean Time to Repair	Maximum Time to Repair
Recording Subsystem			
Record Interface Equipment	2,500	0.5	2.0
HDD Recorder	1,000	1.0	3.5
Playback Interface Equipment	2,500	0.5	2.0
Playback Subsystem			
Reproducer	1,250	1.0	3.5
Playback Interface Equipment	1,250	0.5	2.0

Based on a figure of 8,760 hours per year, the estimated maximum amount of maintenance time that could be required on each recording subsystem per year (using the mean time between failures and the maximum time to repair figures) is 29.4 hours, not counting preventive maintenance which is estimated at 1 hour per day. In addition to repairs and preventive maintenance, some recorder alignment operations, averaging about 8 hours per month, are required. Since the playback subsystem is not generally required to be operated continuously, estimates on the time required to perform recorder maintenance and alignment cannot be made with certainty. If the subsystem were used continuously, the maximum time required for maintenance would be 38.5 hours. However, due to the noncontinuous operation of this subsystem, the actual amount would be somewhat less. Preventive maintenance could range from 10 minutes to 1 hour per day depending on usage, and alignment procedures could require as much as 4 hours per month. Additional manpower for operating the system would be minimal since it is designed as a tool to be used by existing personnel for training, maintenance, and operational analysis.

In the area of replacement costs, it should be noted that the useful life of each record and reproduce head assembly is specified in terms of the amount of tape passing over the heads. The figure stated in the specification is 23 million feet before replacement becomes necessary. This means that each head assembly could be expected to be replaced every 10,222 hours, based on a tape speed of 7 1/2 inches per second and ignoring footage accumulations due to rewind. If rewind is counted, this figure would be approximately 5,270 hours. In the recording subsystem, using alternating recorders operating continuously, this would result in the replacement of four head assemblies (two for record and two for reproduce) every 2.3 years (not counting rewind). If rewind is counted, the replacements would occur every 1.2 years. The estimated replacement cost for the two sets of head assemblies would be $30,000. The frequency of replacement for the training recorder and operational reproducer head assembles would depend on usage.

In addition to head replacement, the tape library would have to be replenished at an estimated rate of 10 percent per year costing approximately $1,200 annually per site. It should be noted, however, that proper care in handling the tapes used could significantly reduce this figure. It is assumed that the tape cleaner/packer which is currently in use at each ARTCC would be available for use with the ERDIRS tapes. Also included are spare parts replenishment at an estimated rate of 10 percent per year totaling $1,600 per site annually.

CONCLUSIONS

It is concluded that:

1. The specification does describe the complete functional characteristics of a practical En Route Radar Display Recording System (ERDIRS) that meets all the basic operational requirements as defined by, and coordinated with, Systems Research and Development Service/Air Traffic Service/Airway Facilities Service. Briefly these basic requirements are:

   a. Continuously sample and record display data from all operational and training Plan View Displays (PVD's) in any Air Route Traffic Control Center (ARTCC) without any affect upon the operational display computer system.

b. When required, sample and record display data from all training PVD's on a dedicated recorder.

c. On playback, recreate any two operational or training PVD presentations simultaneously without using any part of the operational display computer system.

d. On playback, synchronize a display data tape with an associated voice communication tape.

e. Monitor the status of the recording equipment.

f. Provide for the duplication of display data tapes without interfering with the operational recording function.

2. The engineering model does demonstrate that a practical field ERDIRS can be developed. The critical characteristics which the engineering model demonstrates are the ability to record display data for multiple PVD's and the ability to provide a practical modification to the Display Generator Unit that will allow the ERDIRS to access PVD data without affecting the normal operation of the display computer system.

3. Each 28-track high density digital recorder has the capacity to record, for 4 hours, all the sampled display data for up to 72 PVD's which is sufficient to handle the present number of active PVD's in any ARTCC.

RECOMMENDATIONS

It is recommended that:

1. The Federal Aviation Administration implement, as soon as possible, at least a limited En Route Radar Display Recording System (ERDIRS) capability in order to provide a valuable tool for analyzing operations, procedures, and controller training, all of which affect aviation safety. Suggested uses of the ERDIRS are:

a. Accident investigation

b. Analysis of near-miss situations

c. Traffic flow/delay studies

d. Controller workload studies

e. System performance investigations

f. Enhancement of controller local training

g. Computer overload investigations

h. Evaluation of the effectiveness of present and future program enhancements (conflict alert, minimum safe altitude warning, etc.)

i. Aid in resolving controller/pilot conflicts

j. Locating downed aircraft

k. Maintenance investigations

2. Prior to procuring an ERDIRS field system, because of advances in the state-of-the-art, recording devices and media be investigated once again to ensure the use of the best available recording technique.

3. An investigation be performed to determine if the ERDIRS record interface modification can be improved by reducing its complexity and reducing its impact on the data path for Display Control and Vector Generator number six (DCVG 6) in each Display Generator Unit.

APPENDIX A

SYSTEM DESIGN DATA FOR EN ROUTE RADAR DISPLAY RECORDING SYSTEM ENGINEERING MODEL

Prepared by
ACT-230
September 1981

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

SECTION 1

INTRODUCTION

This document describes the design and the functional characteristics of an En Route Radar Display Recording System (ERDIRS) Engineering Model (EM) that records, stores, and reproduces air traffic control data displayed on the National Airspace System (NAS) En Route Plan View Displays (PVD). It was designed, developed, and fabricated by the Federal Aviation Administration (FAA) Technical Center based upon the engineering and functional requirements defined in Engineering Requirement ER-110-210 dated December 1977. These requirements were established by the Technical Center and Systems Research and Development Service (SRDS) and coordinated with Air Traffic Service (ATS) and Airway Facility Service (AFS).

This ERDIRS EM evolved from the successful demonstration of a breadboard model that was also designed and developed at the Technical Center. The breadboard model was capable of recording data from a single PVD and was intended only to prove the feasiblity of recording and playing back display data. This feasibility effort is documented in Report No. FAA-RD-78-97 dated September 1978, and is entitled "A Breadboard Model Used to Demonstrate the Feasibility of Recording National Airspace System En Route Display Data." The success of this initial design effort resulted in an FAA decision for the Technical Center to design and develop an EM capable of multiple recording and playback of display data as an in-house task. The EM has been completed and will be used as a facility at the Technical Center. It was also used as the basis for developing a detailed functional specification for production systems to be used in Air Route Traffic Control Centers (ARTCC).

SECTION 2

GENERAL SYSTEM DESCRIPTION

2.1 Basic Features. - The ERDIRS EM has the capability to record data from 36 PVDs, and on playback, to reproduce simultaneously all the data sent to any two of the recorded PVDs. The design provides for expansion of the system up to the maximum configuration of the display computer equipment. All PVDs are recorded and reproduced with the same accuracy as the original on-line PVD presentations and there is no means by which the sampled PVD data can be changed or modified.

The block diagram of the ERDIRS EM is shown in figure 2-1. In general, the ERDIRS can be divided into two distinct areas--Record and Playback. On Record, PVD data is sampled by a Record Interface Buffer (RIB) and then recorded on one of two High Density Digital (HDD) Recorders. These record for 4 hours each in an alternating or sequential mode which will permit continuous data recording. The EM described in the block diagram is capable of recording a total of 36 PVDs. However, it is modular and can be expanded to record additional displays. Playback of recorded data in the EM is accomplished using one or both Recorders in the playback mode through the En Route Playback Interface Console (EPIC) to a standard PVD. The system is also capable of performing on-line monitoring and providing status and alarm information. Also the Recorders, with the use of additional hardware, have the potential of being time synchronized with another recorder during playback. Various photographs of the equipment comprising the ERDIRS EM are contained in appendix C.

2.2 Record Element. - The units comprising the Record Element are: the Recorders, the Record Interface and Status Panel (RISP), and the RIBs. A detailed description of this equipment is given in section 3 of this document.

A dual RIB consisting of two RIBs was physically installed in each of two active Display Generator (DG) Cabinets while a single RIB was installed in each spare DG Cabinet. Contained within each DG Cabinet are two identical Display Generator Units (DGU) with each DGU containing six Display Control and Vector Generators (DCVG). Each DCVG provides data and control to a single PVD. Each DGU also contains a Display Generator Input/Output (DGI/O) assembly which is the interface logic between the display computer refresh subsystem and each of the six DCVG's. Since the data pickoff point for sampling the display data is in the DGI/O-DCVG interface, background information on this interface is contained in appendix A. From this data pickoff point, each of the RIBs sequentially samples the refresh frames from each group of six DCVGs, starting with DCVG-1. The RIB stores one frame of display data then transmits this data to the recorder.

Both the Computer Display Channel (CDC) and the Display Channel Complex (DCC) equipments are installed at the Technical Center with each equipment having one active and one spare DG Cabinet. In addition, the Direct Access Radar Channel (DARC), which is the backup equipment for the CDC and the DCC systems, is also installed. Since the data pickoff point for the RIB's is after the DARC data enters the system, no change in the RIB is necessary to accommodate this backup equipment.

At the Technical Center, the 24 PVDs receiving data from two active DG Cabinets, plus one spare DGU from each of the wo display computer systems, will be recorded making a total of 36 data sources being recorded. Spare DGUs are recorded the same as active DGUs in order to ensure dislay data recording following reconfiguration.

The Record Element of the ERDIRS is capable of expansion to accommodate any PVD complement by adding a RIB for each DGU and an additional recorder pair for every group of 1-6 RIBs (36 data sources).

Status and alrm information on each RIB and on the record operation is available at the RISP and is described in paragraphs 3.3.5 and 3.4

2.3 PLAYBACK ELEMENT. - The units within the Playback Element are: the Playback Recorder(s), a Data Multiplexing Subunit (in RISP), the EPIC, and two off-line PVDs. A detailed description of these equipments is given in Section 4 of this document.

The playback element is designed to operate in three modes: the monitor mode, the playback mode, and the duplication mode. In the monitor mode, the Playback Element is used to visually monitor the function of the Record Element. This is accomplished by refreshing an off-line PVD with data from the read head of the active recorder. In this mode, the playback element also has access to data at the input to the recorders, thus providing a preview of the data to be recorded.

In the playback mode, the Playback Element is used to review and analyze recorded tapes. In this mode, it is capable of reading the recorded data from two PVDs and displaying this data on two monitor PVDs simultaneously.

In the duplication mode, two recorders are used. One recorder is used to playback the data to be duplicated while the other is used to record the data. The balance of the Playback Element is not used for duplicating tpaes unless the operator wishes to visually monitor the operation.

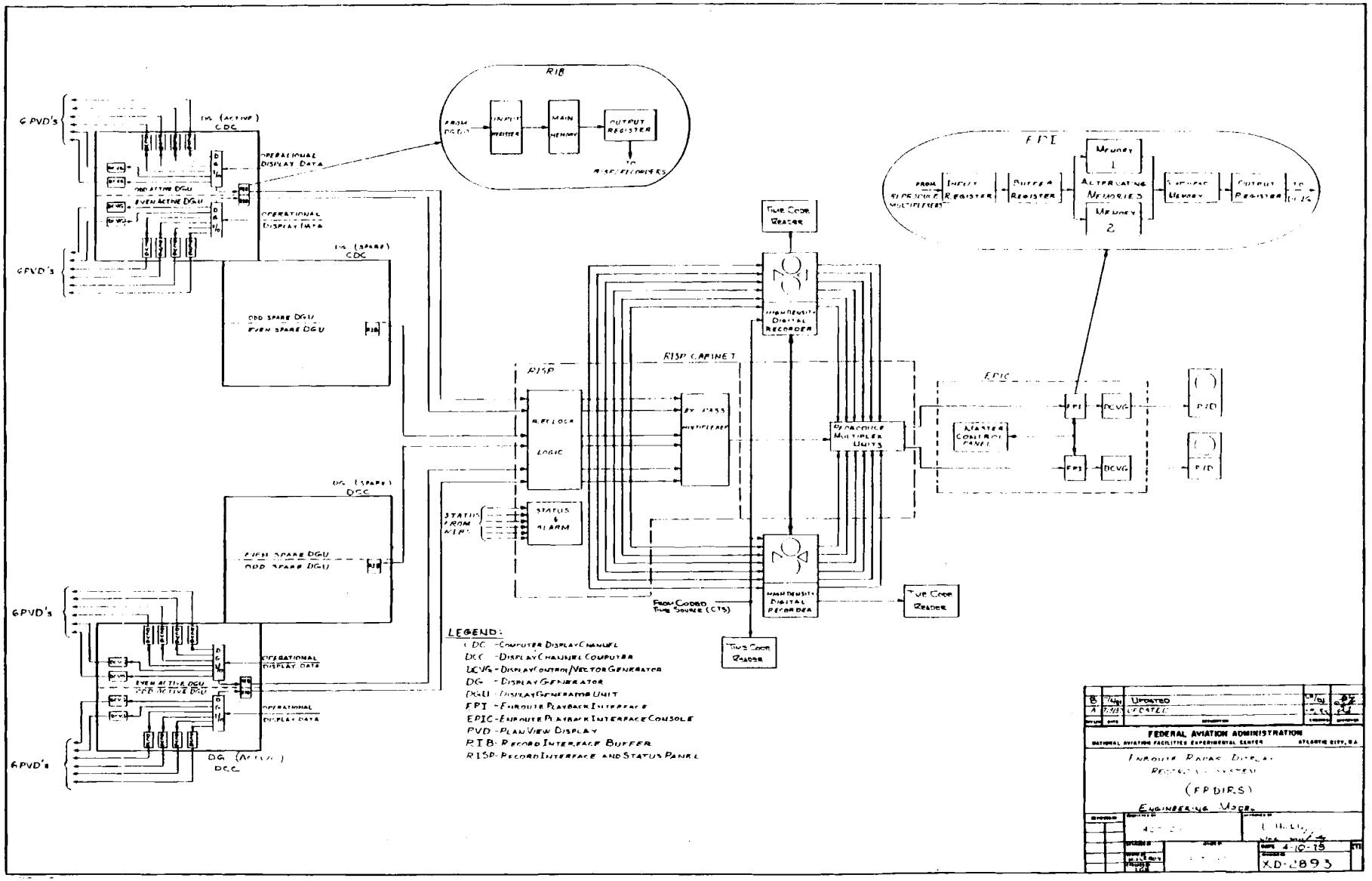


FIGURE 2-1. ERDIRS ENGINEERING MODEL BLOCK DIAGRAM

SECTION 3

RECORD ELEMENT

3.1 General Description. - The Record Element encompasses the equipment and interfaces between the DGI/O and the writing of the display data on magnetic tape. In the data flow sequence, this equipment and interfaces are: the DGI/O-RIB Interface, the RIB, the RISP, and the Recorder record electronics The Record Element consists of six RIB's, a RISP, and two sequentially operated HDD Recorders. Three RIB's are associated with the CDC system and three RIB's are associated with the DCC system. All active sectors in the Technical Center System Support Facility consisting of 12 PVD's in the CDC system and 12 PVD's in the DCC system can be recorded along with one spare DGU (six DCVG's each) from each system as shown in figure 3-1.

Each RIB samples refresh frames from up to six DCVG's. These frames are sent to the RISP where they are reclocked for proper timing and then sent to the Recorder electronics. At this point, the display data has deskewing information added and it is encoded to better match the spectral characteristics of the head and tapes. The data is then written onto tape at a packing density of 29,000 bits/inch/track.

In addition to the sampled display data, the RISP receives status and alarm data from each RIB and displays it on a panel for monitoring and troubleshooting.

In order to minimize noise interference and signal degradation, the RIB's are installed inside the DG Cabinets. A NAS Change Proposal (NCP) was generated and approved for this installation. Due to limited space, the EM was designed so that two RIB's share a single card cage. This is referred to as a dual RIB installation and in the Technical Center EM, dual RIB's are installed in each of the two active DG Cabinets with a single RIB installed in each of the two spare DG Cabinets. In a single RIB installation, the same dual card cage is utilized but the cage contains only those printed circuit boards required for one RIB. In a dual RIB, each RIB remains functionally independent except for sharing a common output clock and a common status line.

3.2 DGI/O-RIB Interface. - Each DGU consists of a DGI/O assembly and six DCVG's. The DGI/O contains data reclocking logic, parity check logic, a DCVG address decoder, a blink clock generator, and the DCVG output multiplexers and drivers. The 16-line parallel data bus from the DGI/O is common to all six DCVG's and terminates in six sets of gated drivers, one set for each DCVG which activates the proper driver and allows data to be gated to the DCVG that is being addressed. Additional details concerning this interface are contained in appendix A.

The RIB obtains the necessary data and control signals from this interface via two connectors mounted on the front of the A6 Driver board. This is a new board that fits in the XA06 slot (previously unused) of the DGI/O assembly. Along with backplane wiring changes to the DGI/O, this board is a part of the required DGU modification which is described in detail in appendix B.

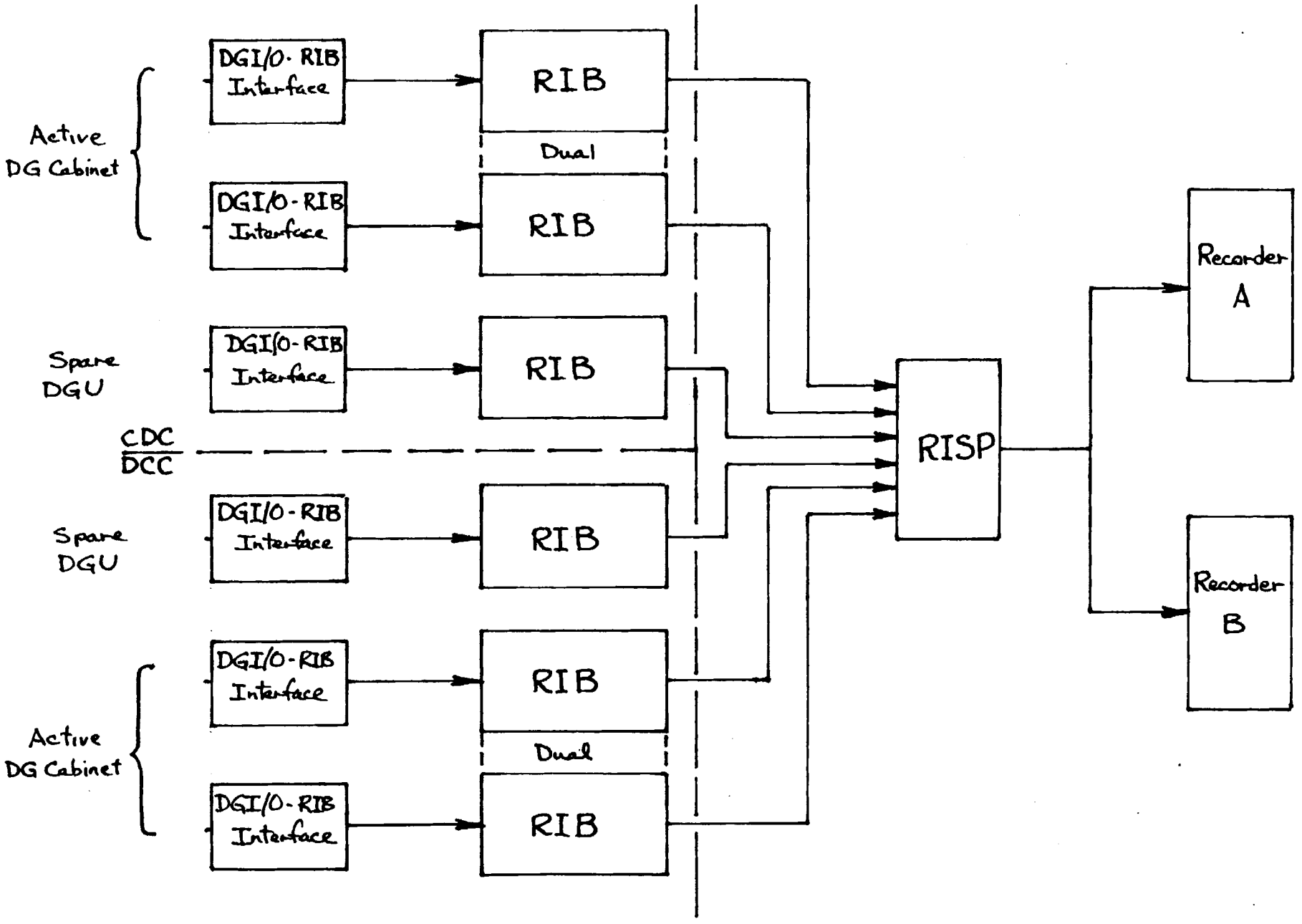


FIGURE 3-1. ENGINEERING MODEL RECORD ELEMENT

3.3 Record Interface Buffer. - Each RIB is designed to sample a complete frame of data from up to six DCVG's in a cyclical manner, store a refresh frame from each DCVG, and transmit that frame of data to a recorder via the RISP. The RIB starts by sampling DCVG-1, and then sending that data at a reduced rate acceptable to the recorder. The RIB will automatically skip inactive DCVG's. Since the EM has no set sample period, the time between samples of a given DCVG is dependent upon the data load, the number of active DCVG's, and the output clock rate. While sampling six DCVG's, each with an average DCVG word data base of 600 words, the sample interval will normally be 0.32 seconds.

As the RIB is acquiring a refresh frame from a selected DCVG, its output logic is reading the first words of the frame from memory and sending this data to the recorder via the RISP logic as shown in figure 3-2. This is performed via a memory write/read interleave to make maximum utilization of the tape. The interleave timing is such that there are no read/write conflicts.

The following subparagraphs describe in detail the various parts of the RIB. Figure 3-3 show a block diagram of the RIB.

3.3.1 Input Logic. - The interface between the RIB and the A6 board (see appendix B) in the DGI/O consists of 16 parallel data lines, six "Valid Address" (VAD) lines, one 4.4 MHz clock line, two "Words per Bank" (W/B) lines, and one master reset line. All input lines are reclocked to reduce line noise problems and to bring the data, VAD, and clock signals in phase with each other. Odd parity is generated on each 16-bit data byte received by the RIB prior to the reclocking registers and becomes the seventeenth bit accompanying the corresponding byte through the RIB.

In addition, the input logic checks each 64-bit work (four 16-bit bytes) for odd parity and, when bad parity is detected, sets an indicator on the front of the logic card and sets a bit in the RIB status sent to the RISP.

The 4.4 MHz input clock is delayed and used to reclock the remaining input lines. The delayed clock is then run through a tapped delay line to generate a five phase clock for internal timing and control.

3.3.2 Input Control Logic. - The RIB input control logic performs two tasks: the selecting of active DCVG's and the writing of the refresh frame sampled from the selected DCVG into the RIB memory. It also controls the write/read interleave operation of the RIB memory.

The DCVG select logic determines which DCVG's are active in a DGU by monitoring the VAD line for each DCVG sequentially. This applies to both the active and spare DGU's. When the select logic finds an active DCVG, it signals the input control logic that data is available for sampling. A counter is used to keep track of which DCVG within the DGU is being sampled. This counter is incremented each time the RIB has finished reading a refresh frame from memory or whenever it is determined that the DCVG, designated by the count, is not active, The contents of the counter become the address code which the output control logic inserts into the output data stream as

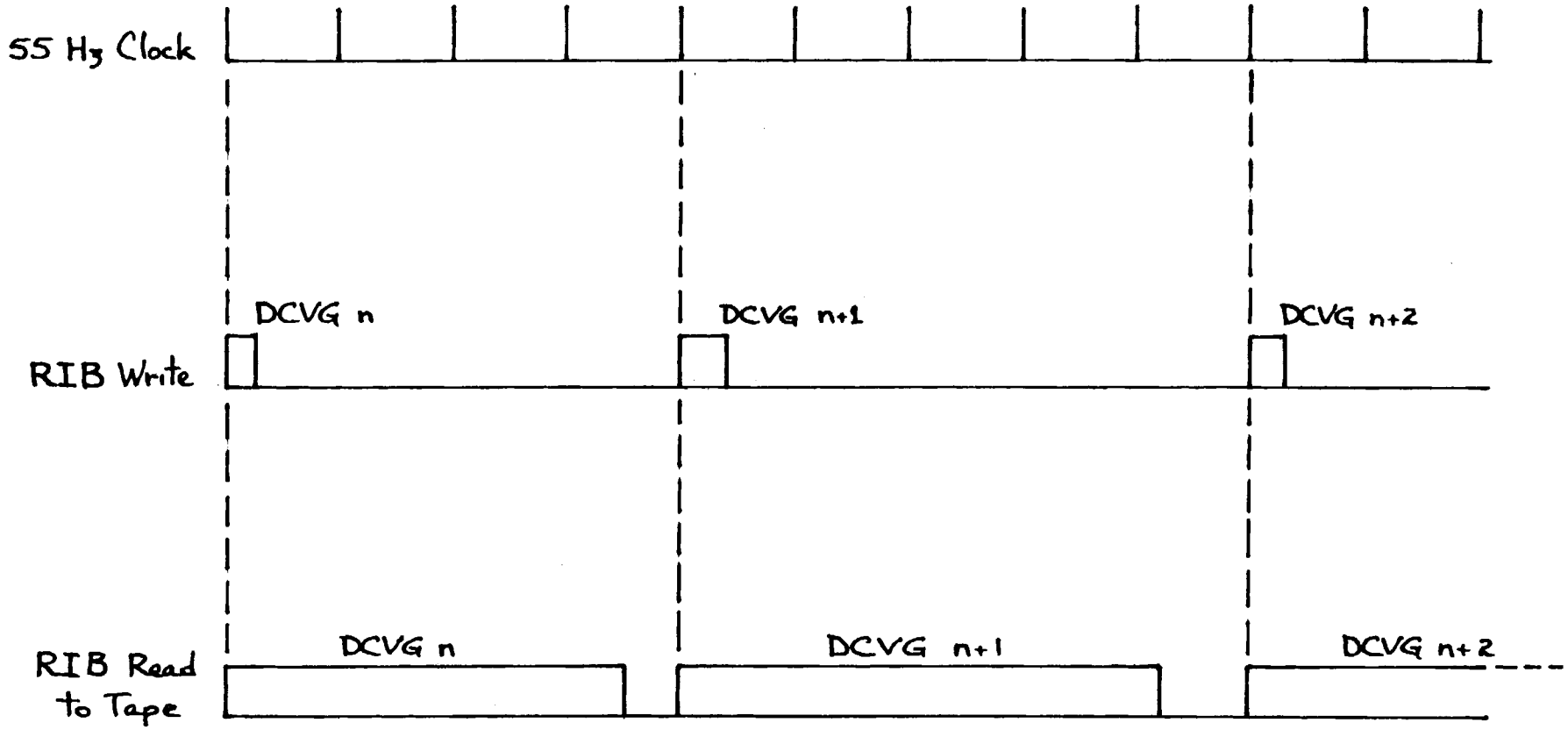


FIGURE 3-2. RIB MEMORY WRITE/READ SEQUENCE

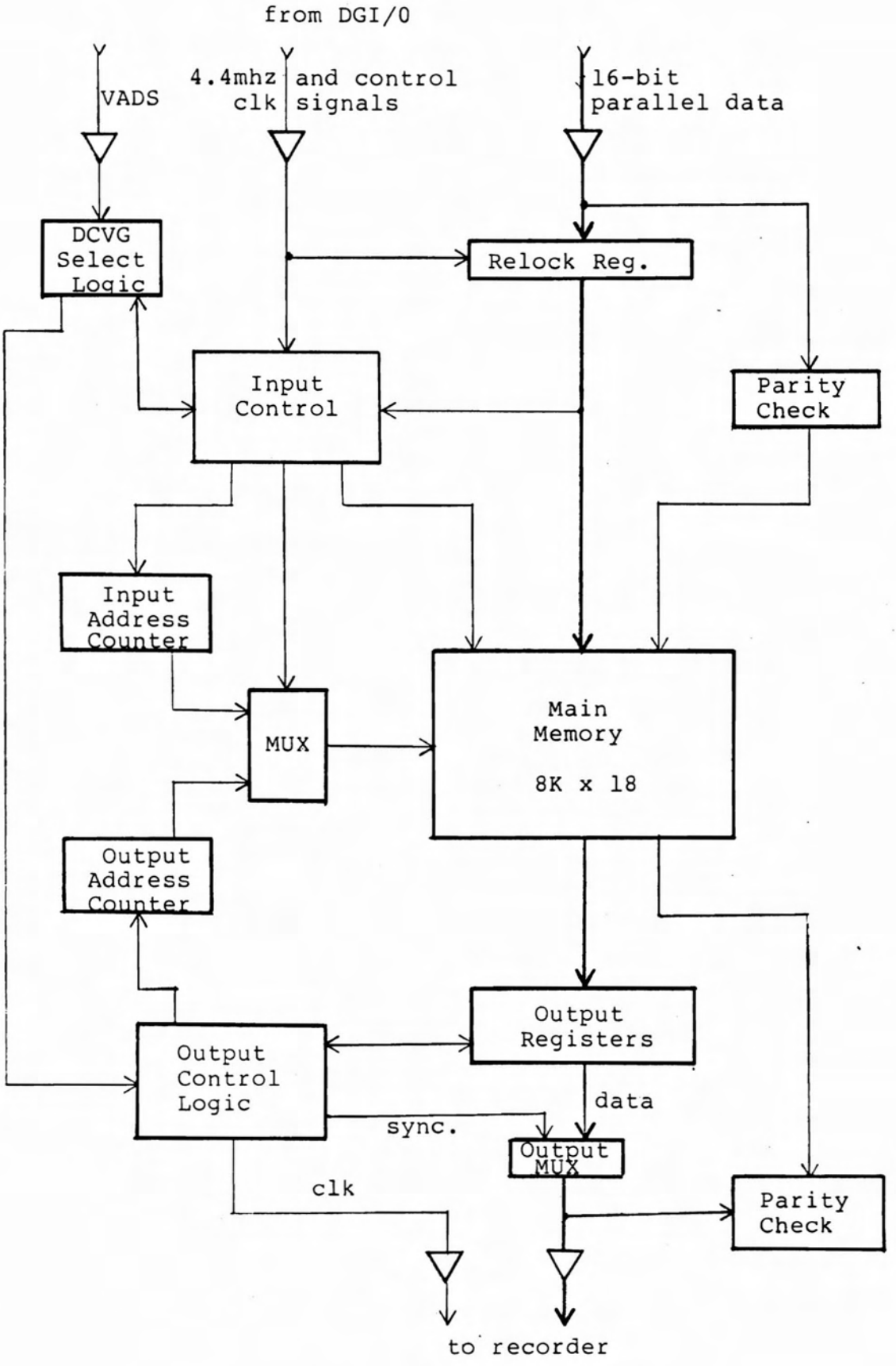


FIGURE 3-3. RIB BLOCK DIAGRAM

byte three of the sync word. See paragraph 3.3.4 for details on the sync word. Counter states 0000 through 0101 represent DCVG's one through six respectively. After state 0101 is reached and acted upon, the counter is cycled to 0000 and the sampling sequence is repeated. When a selected DCVG is determined to be active, its associated VAD signal is steered to the input control logic for word control use.

Once a DCVG has been selected, the RIB input control logic must wait until the output control logic has finished sending the previous frame to tape. Then the input control logic monitors those data lines which contain the 4-bit op-code of each word to detect the last word of a refresh frame, which is the End-of-Display (EOD) word. It then looks for the first word of the next refresh frame so that sampling can begin. This insures that a complete, rather than a partial, frame will be sampled. In the DCC system, each refresh frame begins with a Start-of-Data (SOD) word. Therefore, the RIB looks for an SOD word before it begins sampling data from a DCVG which is part of the DCC system. The CDC system uses a Major Position/Single Symbol (MPSS) word, which contains trackball data, to start a refresh frame. This word is then followed by an SOD word. In order to sample the trackball data which comes before the SOD word, the RIB does not start the sampling upon detecting an SOD word. Instead it starts sampling when it detects the first MPSS word after an EOD word. A wire jumper on the RIB backplane allows easy conversion between the two systems. In either case, each frame ends with an EOD word.

The VAD signal is used to determine the start of each memory write operation, since it occurs during the first byte of a bank of data words. See appendix A for details of the timing relationship between the data, the VAD, and the 4.4 MHz clock signals. A byte counter is used to determine when a full data word (4 bytes) has been written into memory and a word counter is used to count the number of words written into memory for each VAD signal received. When the word count is equal to the number of words designated by the state of the W/B signals obtained from the A6 board, the write operation is ceased until the next VAD signal is received. During the time between the end of one write operation and the beginning of the next (a minimum of 9.9 microseconds), the output control logic is permitted to access the memory and read out a data word for storage in its output registers. This read operation is explained in detail in paragraph 3.3.4. The operation by which the output logic is given access to the memory during the time when the input control logic is waiting for the next VAD signal is called the memory write/read interleave operation.

3.3.3 Memory. - The RIB memory consists of a solid state memory array used to temporarily store the refresh frame being sampled by the RIB. Display data is written into memory in groups or banks of one to four words (depending on the states of the W/B signals) during the RM access time for the selected DCVG. The read/write operations of the memory are interleaved during the frame sample time. The output logic can access memory to read out a data word during the time period between accesses by the input control logic. This interleaving operation exists only while the input logic is loading a frame into memory. When a complete frame is loaded, the input control logic no longer needs to access memory until the frame is stored in memory is completely unloaded by the output logic. During the time between the completions of the loading and unloading processes, the output logic has continuous access to the memory.

The memory is operated in a first-in-first-out mode, that is, the first data word written into memory is the first work read out. In this manner, the sampled refresh frame is written onto tape in the same word sequence as it is sent to the on-line DCVG. Two 13-stage binary counters are used to address locations in memory - one for the input (write) address and one for the output (read) address. Both counters are reset to zero at the start of a refresh frame sampling operation. The input address counter is incremented whenever a 16-bit byte is written into memory and the output address coutner is incremented whenever a byte is read out of memory. A 2-to-1 multiplexer is used to select the address from either coutner for use in accessing the memory. This multiplexer is controlled by the input control logic which has priority over the access of memory. The address from the input address counter is applied to the memory address lines only during the writing of a sampled bank of words into memory by the input control logic. At all other times, the address from the output address coutner is applied to the memory address lines. When the output logic has completed transferring a frame from memory to tape, the addresses in both the input and output address counters should be equal. There is address comparison logic which checks for this condition at the end of each frame transfer. If both addresses match, a good write/read operation occurred; if there is no match, an error has occurred. In the latter case, an alarm bit is set in the status word sent to the RISP where an indicator is lit.

The memory consists of a single 4.5" x 7" printed circuit board containing 36 memory coponents connected in a 2 x 18 array. Each component consists of a 4096 x 1 bit random access memory (RAM) IC with a tri-state output structure. Thus when arranged in the array these 36 IC;s rpovide a total memory capacity of8192 18-bit bytes. This board is identical to the board sued int eh Playback Element as described in paragraph 4.2.3.1.3. Sixteen bits of each byte are used for data. One bit of each byte is used to store a parity bit for the byte. The remaining bit is set to "one" if the byte is the first byte of a word; otherwise it is set to zero. This last bit which is called the index bit is used by the output logic.

The 8192 byte capacity translates into 2048 64-bit DCVG data words. The average ATC refresh frame is estimated to be 600 data words and the PVD will operate asynchronously with a maximum of 1680 data words. (See Appendix B.) The capacity of the memory is extended beyond 2048 DCVG words by using a "wrap-around" type operation. It will take a minimum of 22.1 milliseconds to store the first 2048 DCVG words of a refresh fram (2048 words x 10.8 microseconds/word, minimum). As the normal output clock rate of 222 kHz (4.5 microseconds) and a tape word time of 90 microseconds, a minimum of 245 data words will have been transferred out of memory and onto tape. The locations used to store these 245 words are now available for use is storing data beyond the 2048 already stored. It has been calculated that the minimum capacity of the memory using this wrap-around mode is approximately 2300 DCVG data words. Since the data is written into memory faster than it is read out, there is a remote possibility that the input address counter could catch up to the output address counter in the wrap-around mode in which case new data would be written into locations containing dtat not yet sent to tape. The address comparison logic is used to detect the "overwrite" condition and, when this condition exists, a bit is set in a RIB status word that is sent to the RISP. The address comparison logic is also used to detect when the memory is operating in the wrap-around mode and, if so, a bit is set in the status word. At present, no logic has been incorporated in the RIB to truncate a frame in order to avoid an overwrite

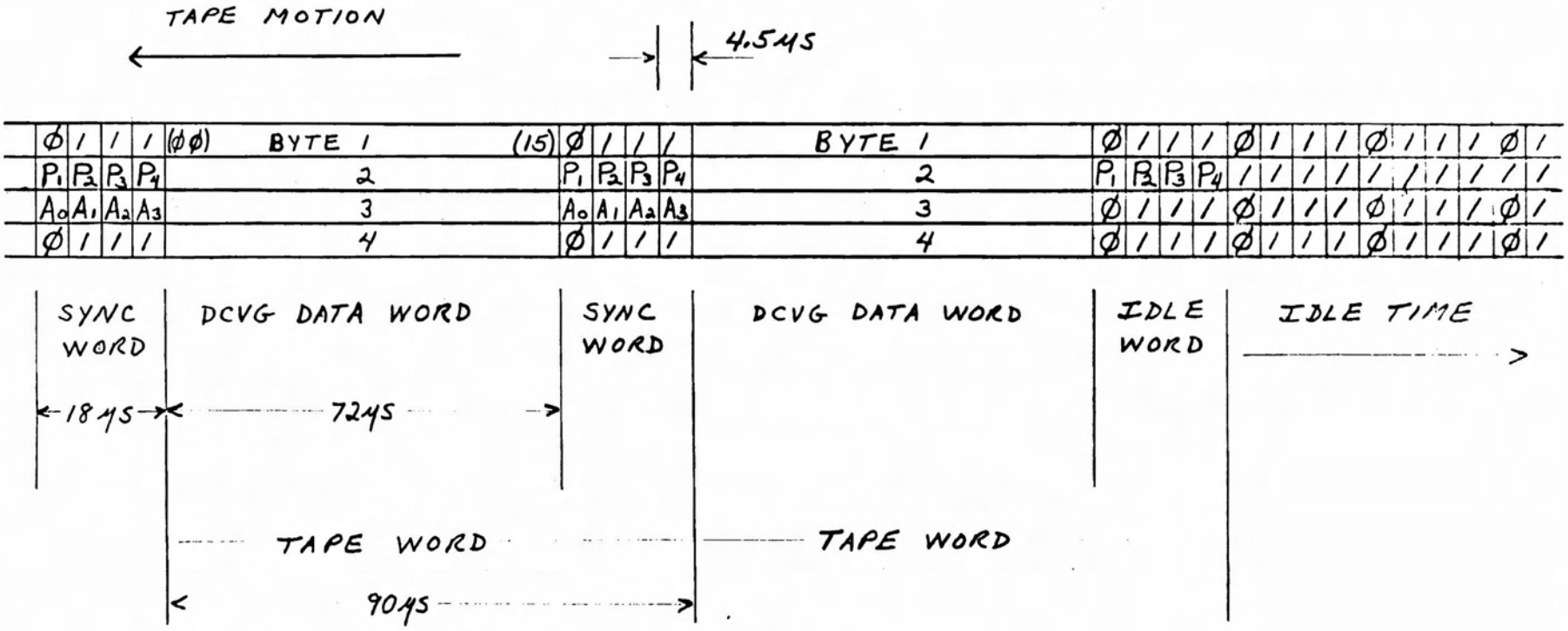
condition. However, the probability of an overwrite condition occurring is extremely low since the amount of data required to cause this situation would be so large it would render the display presentation useless for normal ATC purposes.

3.3.4 Output Logic. - The 64-bit DCVG data words, which are stored in the RIB memory as four 16-bit bytes, are turned 90 degrees by four parallel-in, serial-out shift registers called the output registers. The 90-degree terminology is used to designate the process of converting the DCVG data words from a 16-bit paralled, 4-byte serial format to a 4-byte parallel, 16-bit serial format. This is theformat is which the data is sent to the recorders. A 16-bit sync word is inserted between the data words sent to the recorder to enable the playback element to separate the data words and to provide display address information and parity information. These sync words are organized in four 4-bit bytes with each byte being recorded along with a data byte serially on a separate track.

The sync bytes on tracks 1 and 4 are set to the sync code (Ø111); the byte on track 2 consists of four parity bits, one for each byte of the preceding data word. The byte on track 3 consists of a address code which is used to indicate from which DCVG the data was sampled. Only three bits are required to address six DCVG's; the most significant bit of this byte is presently unused. The address codes for DCVG's 1 through 6 are (ØØØ) through (1Ø1), respectively. The sync code is used in place of the address code whenever there is no data available to be sent to the recorder. The time period during which the sync code is sent in place of the address code is called idle time. Figure 3-4 shows the tape data format.

When the output logic receives a Start-of-Frame (SOF) signal from the input logic, indicating a new frame is being sampled, the output logic terminates the idle period by completing the transmission of the last idle sync word. The "output" flip-flop is now set to start the output operation. The SOF also initiates theloading of a new display address, derived from the counter used by the DCVG select logic, into the output address register. The output logic now sends an sync word, which contains the new display address in byte 3, to the recorder. This sync word must be sent before any data word is sent because a sync word with the appropriate display address in byte 3 must precede each data word sent to the recorder in order for the Playback Element to determine from which display a data word was sampled.

By the time the first sync word is sent to the recorder, the input logic will have loaded one to four words into memory. While the input logic is waiting to receive the next VAD and its associated data word(s), it sends a signal to the output logic which enables the output register load logic to read a data word from a location in memory specified by the output address counter. Each byte of this word is loaded into a separate 16-bit shift register. As this point the index bit of the first byte read out of memory is checked to verify that this byte is the first byte of a data word. If it is not, an indicator is set on the front edge of the logic card and a bit is set in the status word sent to the RISP. The total time needed to transfer data word from memory to the output register is 3.6 microseconds. This transfer is accomplished during the 18 microseconds used to send the sync word to the recorder. Figure 3-5 shows the basic RIB timing.



TIMES GIVEN ARE FOR A 220KHZ DATA RATE.

FIGURE 3-4. TAPE DATA FORMAT

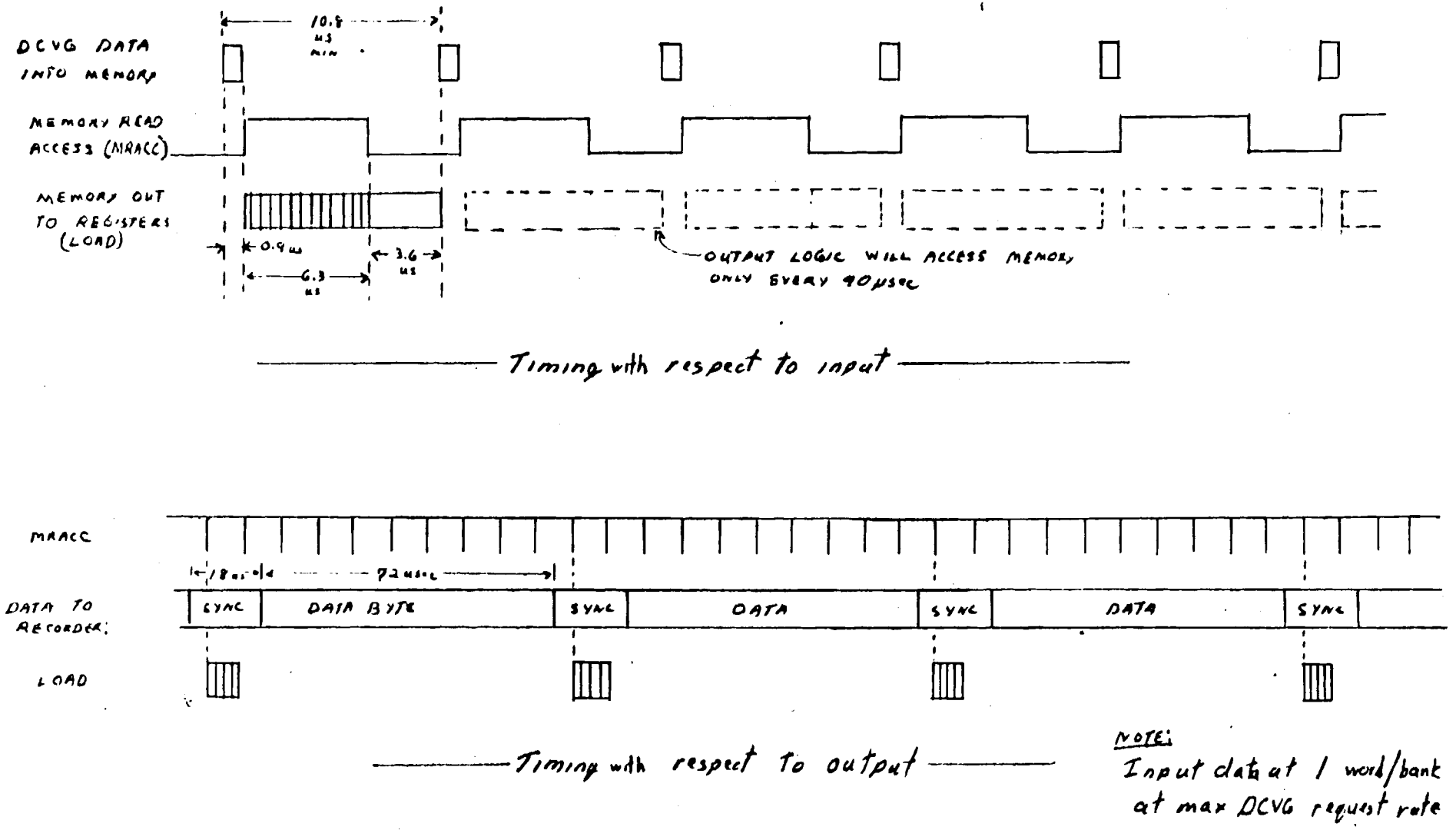


FIGURE 3-5. BASIC RIB TIMING

Each data word is read from memory during the preceding sync word time. When the sync word is completed, the data word is sent to the recorder with each byte of the word clocked out serially on a separate line for recording on a separate tape track. The parity of each byte is generated just prior to the line drivers and this parity is checked against the input byte parity which was stored in memory with the data. If bad parity is detected, an indicator is set on the card edge for the byte which contained the error. Each RIB has four output data lines (one port), but the two RIB's within a dual RIB share a common output clock line. This clock line carries a 222 kHz clock under normal operation (at a recorder tape speed of 7 1/2 inches per second (IPS). A common status line is also shared between the two RIB's (see figure 3-6).

3.3.5 Clock and Status Logic. - The clock and status logic consists of circuitry which is common to both RIB's in a dual RIB cage. It also can be used by a single RIB. Its purpose is to derive the output clocks, to assemble the status word, which contains status and alarm information on both RIB's, and to transmit this work to the RISP. The output clock for the RIB can be derived in one of two ways: either from a reference clock sent from the RISP or by dividing down the 4.4 MHz display system clock. Since the EM must operate with two different display computer systems simultaneously at the Technical Center, and the slight differences between the two system clocks can cause reclocking difficulties at the RISP, the EM presently configured to use the reference clock from the RISP in deriving the output clock. This reference clock is at a frequency twice that of the actual output clock. It is used by the RIB output logic and is also divided by 2 to generate the actual output clock. When only one display computer system is being recorded by the ERDIRS, the RIB could use the 4.4 MHz clock to derive a clock internal to the RIB to replace the reference clock from the RISP. The internal clock is derived by dividing the 4.4 MHz clock by 10 they by 2 to produce two clocks: one at a frequency of 444 kHz and the other at 222 kHz. A multiplier is used to select one of the two frequencies to be used by the output logic. This signal is then divided by 2 to form the final output clock. Regardless of whether it is derived from the RISP reference clock or from the 4.4 MHz clock, the final output clock must be 222 kHz for a recorder tape speed of 7 1/2 IPS and 111 kHz for a tape speed of 3 3/4 IPS. The clock control line between the RIB and RISP can carry either the reference clock from the RISP or a control signal to control the multiplexer selecting between the 444 kHz and 222 kHz internal clocks. A simple change on the RIB clock and status card will allow the use of the 4.4 MHz clock in place of the RISP reference clock for deriving the final output clock.

The status and alarm data is assembled and loaded into a parallel-in, serial-out shift register and transmitted to the RISP as a serial data stream. The status word consists of 28 data bits and 4 sync bits and is sent at the same clock rate as the display data. The following status is sent for display at the RISP:

1) Frame - RIB input logic is loading a sampled frame into memory.

2) Output - RIB output logic is unloading a frame from memory and is sending it to the recorder.

3) PVD Address - Address of the DCVG from which the data was sampled. (4 bits from byte 3 of sync word)

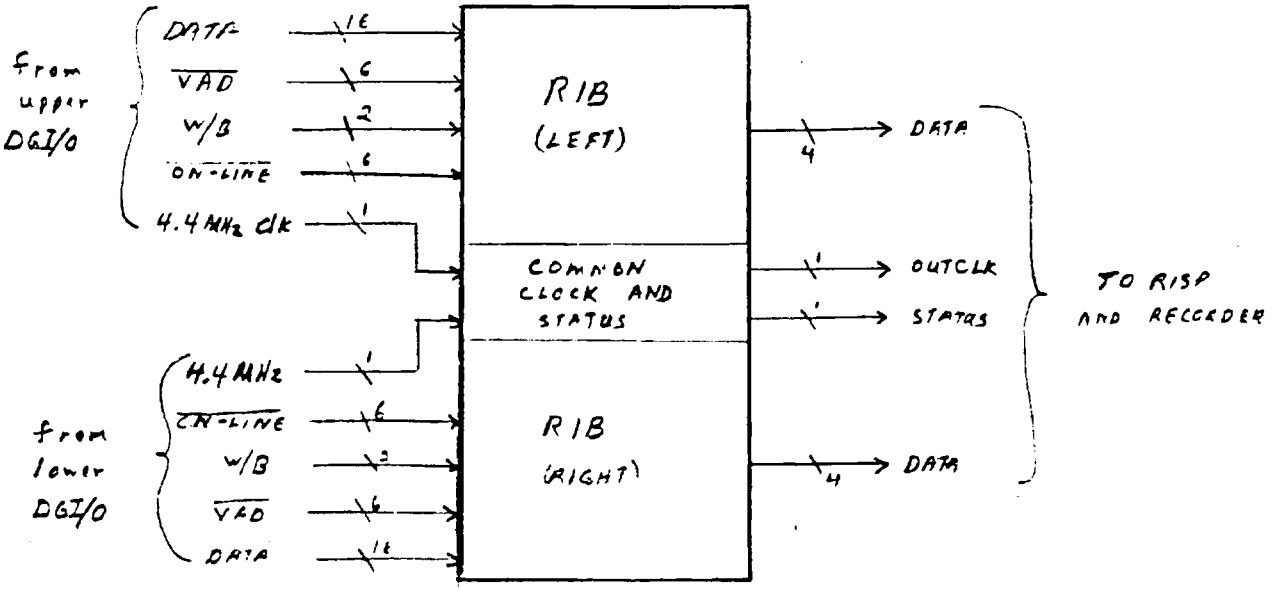


FIGURE 3-6. DUAL RIB INPUT/OUTPUT

4) Wrap-around - 2048 data words of a given frame have been written into memory and the input logic is using the first part of memory to store additional words.

The following alarms are transmitted for display at the RISP:

1) Input Parity Error - The byte parity generated at the input does not match the word parity.

2) Output Parity Error - The byte parity generated at the RIB output does not match the byte parity generated at the RIB input.

3) First Byte Slip - The first byte of a word unloaded from memory is not the first byte of a data word.

4) Memory Overflow - Data is being written into locations in memory which contain data not yet sent to the recorder.

5) Addresses Not Equal - The input and output address counters are not equal after a frame is sent to tape.

Those alarms which occur too fast to be loaded into the status/alarm register are stored in interim flip-flops which are cleared after the information is loaded into the status/alarm register.

3.4 Record Interface and Status Panel. - The Record Interface and Status Panel (RISP) is functionally located between the RIB's and the HDD Recorders. The first major function of the RISP is to act as an interface between the RIB's and the Recorders. The RISP contains line receivers for receiving the data, clock and status signals from the RIB's. The Recorder configuration requires a single master clock associated with all the data lines, with the data in phase with this clock. Reclocking of the data is necessary to synchronize the data with the master clock generated by the RISP. This reclocked data and master clock are sent to the Recorders and to a multiplexer, within the RISP, which is controlled by the EPIC. This multiplexer enables the EPIC to receive data directly from the output of the RIB's thereby by-passing the Recorders. A block diagram of the RISP is shown in Figure 3-7.

The second major function of the RISP is to display the operating status of each RIB. This status information is remoted to the RISP because the RIB's are located inside the DG Cabinets. Status and alarm conditions from each RIB in a dual RIB cage time share a common status line to the RISP. The status and alarm information is contained in a 32-bit word which is sent serially to the RISP at the 222 kHz data rate. This serial data is decoded and displayed on the RISP front panel. Red indicators show failure conditions, such as parity errors (input and output), byte slip, memory overflow, and address not equal. Yellow indicators are used to show degraded conditions such as RIB memory wrap-around. Information on which DCVG's are on-line and are being recorded, frame status, output status and sync status are all indicated using green indicators. The status logic is discussed in paragraph 3.3.5 and is expandable to accommodate the maximum capacity ERDIRS.

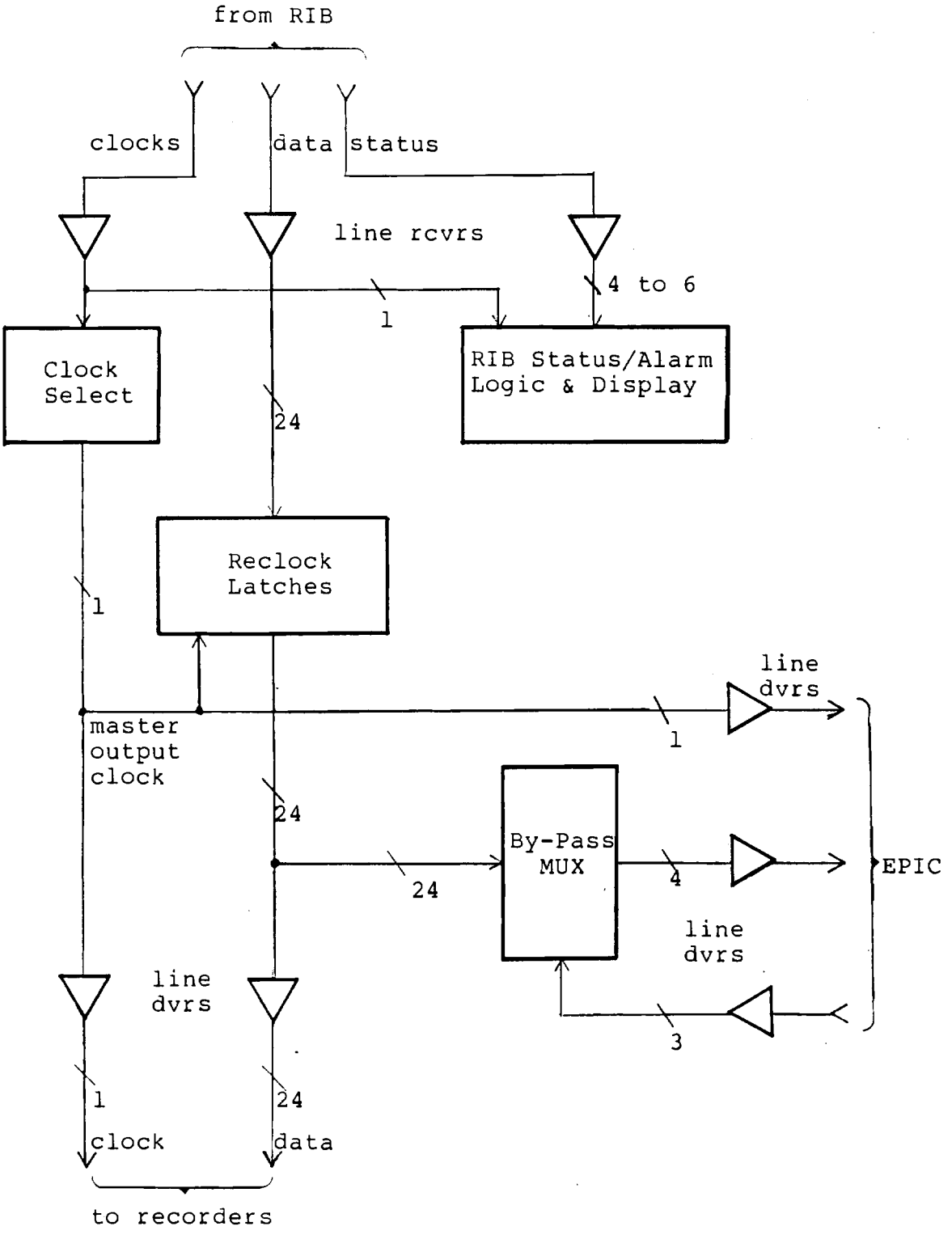


FIGURE 3-7. RECORD INTERFACE AND STATUS PANEL (RISP)

3.5 High Density Digital Recorder. - The Record Element utilizes two standard Ampex HBR-3000 28 track High Density Digital Instrumentation Recorders, capable of operating in an alternating or sequential mode in order to provide for continuous recording. They have been modified to generate and record parity information based on the user data, and check user data on a per track basis for parity errors during playback.

The record electronics contained within the Recorder performs several operations on the data sent to the Recorder before the data is actually written on tape. For each set of twelve (12) data channels a master channel is set aside for use in the deskew operation. Therefore, based upon a 28 track machine, two tracks are reserved for this purpose. Deskew words are inserted into the data stream of each data channel every 512 data bits. This insertion is accomplished by transferring a small block of data the size of the deskew word sequentially from each data channel to the appropriate master channel, thus providing enough space in the data channel to insert the deskew word. The deskew word is 32 bits in length and consists of a distinct pattern recognizable by the reproduce electronics within the Recorder. After deskew information has been added all channels are encoded into a Miller Squared code and the encoded data is recorded on tape.

Both record and reproduce head assemblies consist of two head stacks each. The two head stacks are track-interleaved, i.e., all odd tracks are on one head stack and all even tracks are on the other head stack. On the 28-track machine used in the ERDIRS, the tape is one-inch wide and each track is 25-mils wide with a 10 mil guard band between each track as per Inter Range Instrumentation Group (IRIG) standards. Of the 28 tracks, 24 are used for recording digital display data, arranged as six-ports of four tracks each. The four tracks of each port consist of either all odd or all even tracks. This minimizes the effects of mechanical misalignments which may exist between odd and even head stacks of both the record and reproduce head assemblies. Two of the remaining four tracks are used by the recorder electronics to record user data that was displaced to allow for the insertion of deskew words as previously described. One of the remaining two tracks is used to record the IRIG-E serial time code generated by the Coded Time Source (CTS). This time code is conveyed as amplitude modulation of a 600 Hz sine wave and is recorded using direct record electronics. The tape speed used in recording data is 7 1/2 IPS in normal operation.

The weak point in any recording system is the tape-to-head interface. Dust, smoke, and other particles in the air can attach themselves to the tape surface and become the single largest source of errors. Improper handling of the tape can damage the tape edges causing a misalignment between the recorded tracks on tape and the reproduce head stacks. Environmental conditions such as humidity and temperature can cause signal degradation if these factors are not kept within limits. Because of these facts, proper handling of the tape and appropriate preventative maintenance techniques is essential to ensure reliable system performance. Every attempt is made to keep the relative humidity between 40 and 60 percent and the temperature between 16° and 30°.

3.6 Mechanical and Electrical Data. - The dual RIB card cage is shown in Figure 3-8. In the DG Cabinet both the existing upper and lower DGI/0 card cages were lowered approximately three to five inches to provide space for the dual RIB card cage to be installed above these two cages as shown in Figure 3-9. The dual RIB is 5.5 inches (14 cm) high, has a depth of 13 inches (33 cm), and fits in a standard 19 inch (48.3 cm) rack space within the DG Cabinet. All logic cards and power supplies are accessible from the front.

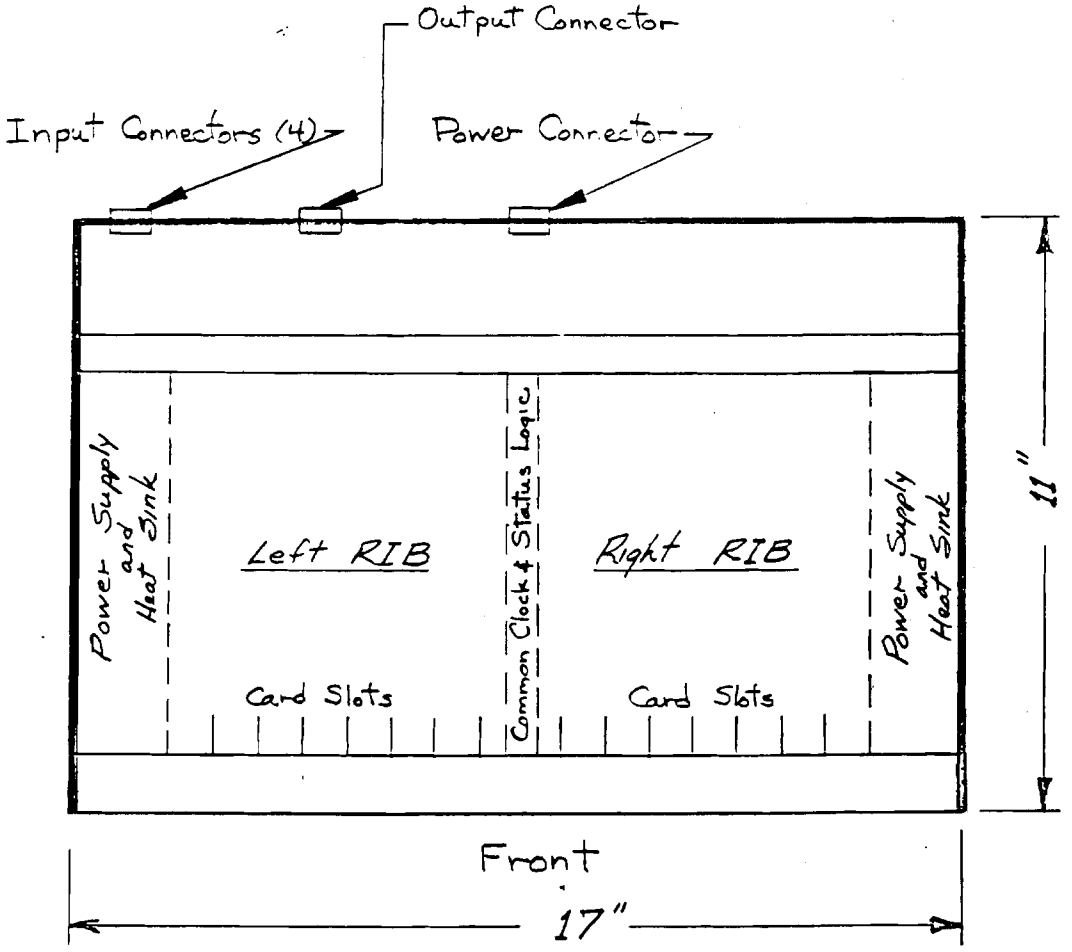


FIGURE 3-8. DUAL RIB CARD CAGE PHYSICAL LAYOUT (TOP VIEW)

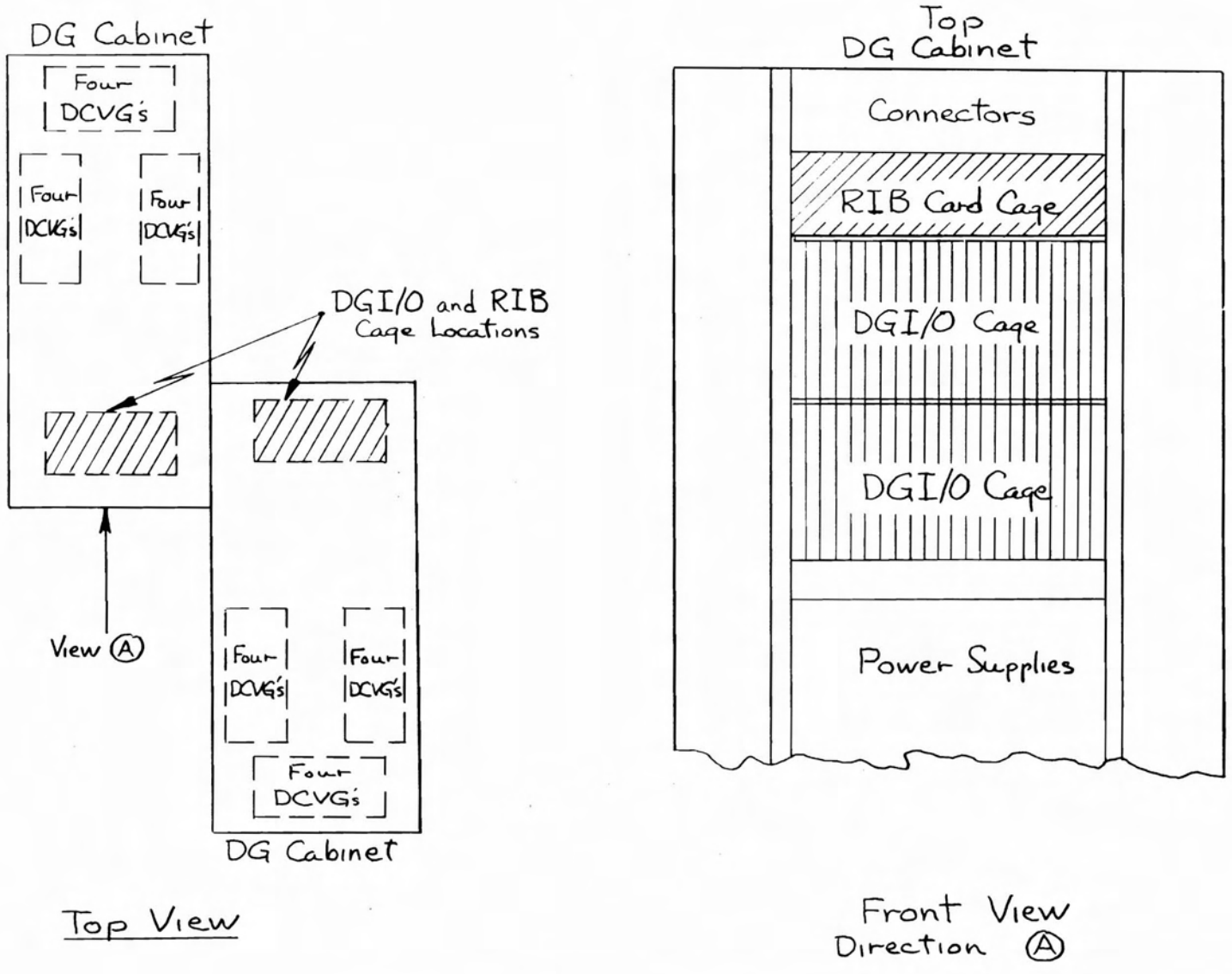


FIGURE 3-9. LOCATION OF DUAL RIB CARD CAGE IN DG CABINET

Two cables from the new XA06 Driver board in the DGI/O card cage, provide the interface between the DGU and the input to its respective RIB. A single 12 pair cable is used to convey the data from the output of the dual RIB card cage to a connector at the top of the DG Cabinet. Another 12 pair cable is used to convey the data from the DG Cabinet to the RISP.

The RIB power supplies are mounted on heat sinks and located at the extreme ends of the card cage as shown in Figure 3-8. Redundancy is provided in the power supply area. In a dual RIB installation either power supply can and will handle the complete load for both RIB's should one power supply fail. A switching regulator type power supply was used because of its high efficiency (approximately 75%) and reduced size. Each power supply provides 5 volts DC at 20 amps. To minimize the heat dissipation of the RIB assembly, low power logic and low power Schottky logic IC's were used wherever possible. It is estimated that the total heat dissipated by a dual RIB assembly including both power supplies is approximately 105 watts or 330 BTU/hr.

The RISP is mounted in the upper section of a standard equipment cabinet adjacent to the HDD Recorders. The front panel of the RISP has Light Emitting Diode (LED) indicators to display the status and alarm conditions of the recording system. The cables between the RIB's and the RISP have a nominal length of 150 feet with a maximum design length of 300 feet.

SECTION 4

PLAYBACK ELEMENT

4.1 General Description. - The Playback Element consists of the following:

1 - High Density Digital Recorder *

1 - Data Multiplexing Subunit in RISP

1 - Enroute Playback Interface Console (EPIC)

2 - Off-Line Plan View Displays (PVD)

4 - Time Code Readers

The EPIC contains two units called Enroute Playback Interfaces (EPI) which are used in accepting data from a recorder to drive two DCVG's. These two DCVG's are also located within the EPIC and are used to drive the playback PVD's. Each EPI is designed to emulate the part of the NAS refresh subsystem that supplies data to the DCVG. The EPI stores data from the recorder alternating in one of two semiconductor memories. The EPI contains two interfacing sections--one between the recorder and the memories and the other between the memories and the DCVG. (See Figure 4-1.)

There are three basic modes of operation for the Playback Element. The first is the playback mode in which the Playback Element is used to review and analyze recorded tapes. The second is the monitor mode in which the Playback Element is used to visually monitor on a PVD the function of the Record Element. The third is tape duplication.

In the playback mode, the Playback Element is capable of playing back data from two sectors simultaneously, as in the case of examining a hand-off situation. If the Record Element is recording data on one of the two recorders, the Playback Element will utilize the stand-by recorder for playback. Otherwise, either recorder can be used for playback. When the stand-by recorder is taken off-line, the normal sequential operation of the record group is interrupted. As a result, when the active recorder reaches end-of-tape it will either automatically rewind and continue recording or it will stop and wait for an operator to change the tape before it continues recording. The choice of these two options will be made by the operator of the system.

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* The term recorder is intended to mean a recorder/reproducer. It is assumed that the reader can determine from the context of the material whether the recorder in question is being used to record or reproduce data.

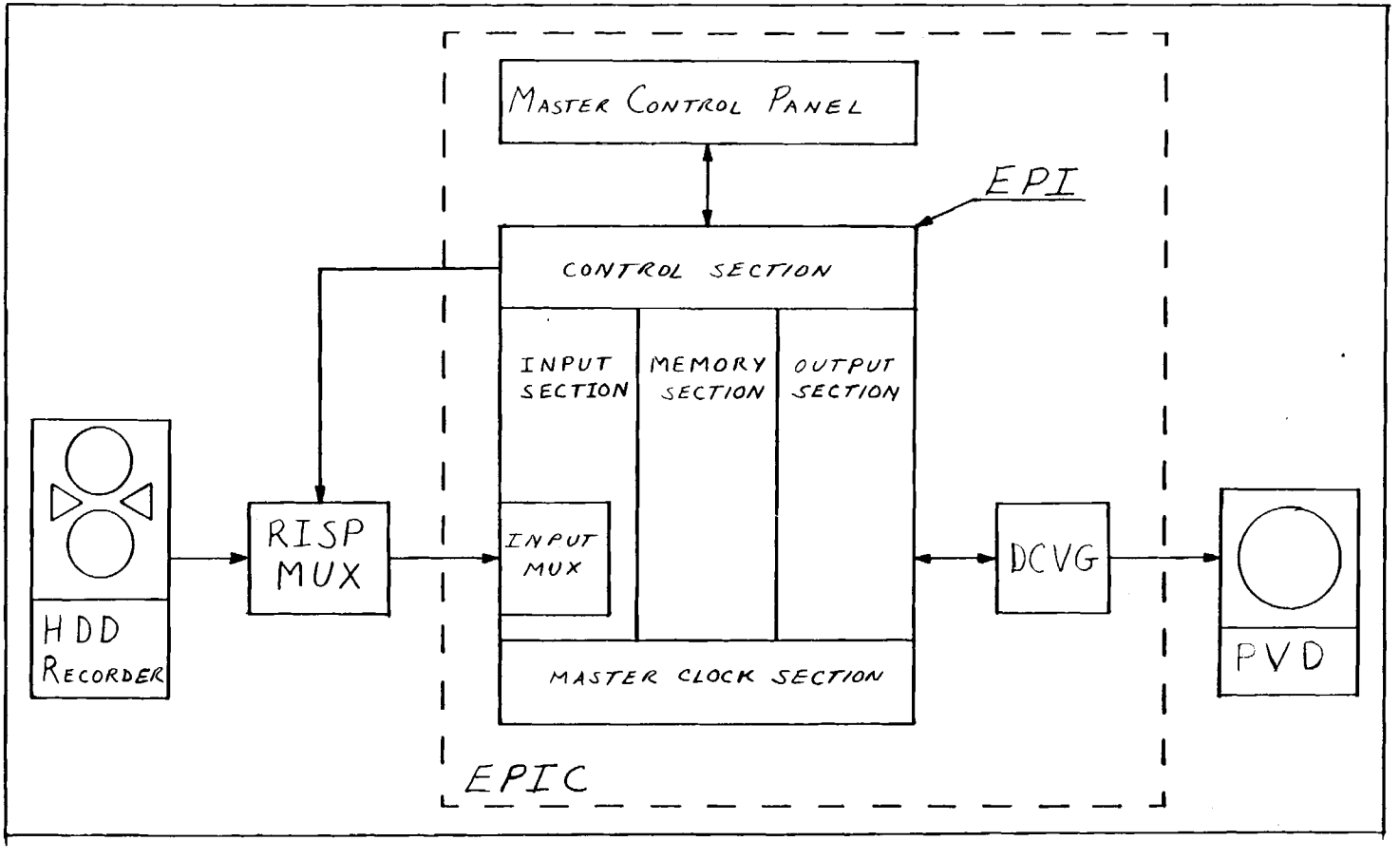


FIGURE 4-1. GENERAL BLOCK DIAGRAM — EPI AND INTERFACES

The RISP cage contains multiplexing circuits which enable each EPI to select data on a port basis. Each port contains data from one DGU (six DCVG's). The multiplexer allows EPI-1 to access data from any of six ports either at the inputs to both recorders or the outputs of each recorder. It also allows EPI-2 to access data at the outputs of each recorder only. Each EPI has a multiplexer card which enables it to select between its normal input, as described above, and a parallel auxiliary input. This auxiliary input allows the EPI to monitor the data being processed by the other EPI. The multiplexer card in each EPI supplies the monitor output to the other unit.

In the monitor mode, EPI-1 is used to monitor sampled display data as it is recorded by the Record Element. If the multiplexing circuit in the RISP is used in the by-pass mode, which enables it to access the data at the inputs to the recorders, errors can be localized by comparing the sampled data both before and after the recording takes place. EPI-2 can be used to monitor data at the outputs of the recorders or at the input to EPI-1; thus it can be used to monitor the performance of EPI-1. In addition to this monitoring function, which is basically a visual check of the display presentation, certain error and status conditions are indicated on panels in the RISP, EPIC and recorders.

In the tape duplication mode, both recorders are used but no RIB's or EPI's are needed. However, EPI-1 can be used to monitor the duplication operation. In this situation, the multiplexing circuits in the RISP will also be needed. The Playback Element is configured for duplication by physically reconnecting the cables to the recorders so that the output of one recorder is connected to the input of the other.

Figure 4-2 is a block diagram showing the basic relationships and data flows between the various units as described above. Part A shows the units in the playback mode; Part B shows the monitor mode; Part C shows the duplication mode.

4.1.1 Tape Data Format. - The EPI is designed to accept data from one recorder port at a time. A recorder port consists of four data lines corresponding to four tape tracks used by a single RIB to record display data for six PVD's. The port shares a common clock signal which is derived from the data by the recorder. The format of the data on these four data lines is shown in Figure 4-3. Each line carries data corresponding to one of the four 16-bit bytes that comprise a 64-bit DCVG data word. Each byte is transmitted to the EPI serially starting with bit ØØ and ending with bit 15. Each data line also carries one of the four 4-bit bytes that comprise a 16-bit sync word. These sync words are used to separate DCVG data words at the input to the EPI and to provide display address information and parity information for the data.

A sync word will precede each DCVG data word. The display address information in this sync word is used by the EPI to determine with which display the DCVG word is to be associated. The EPI is designed to allow the operator to designate the address of the display to be reviewed. The EPI compares the incoming address with the selected address and accepts data only when the addresses are equal. This address information is actually used to designate one of the DCVG's within a DGU. The DGU is designated by selecting the proper port using the multiplexing scheme previously described. Each port corresponds to one DGU. The display

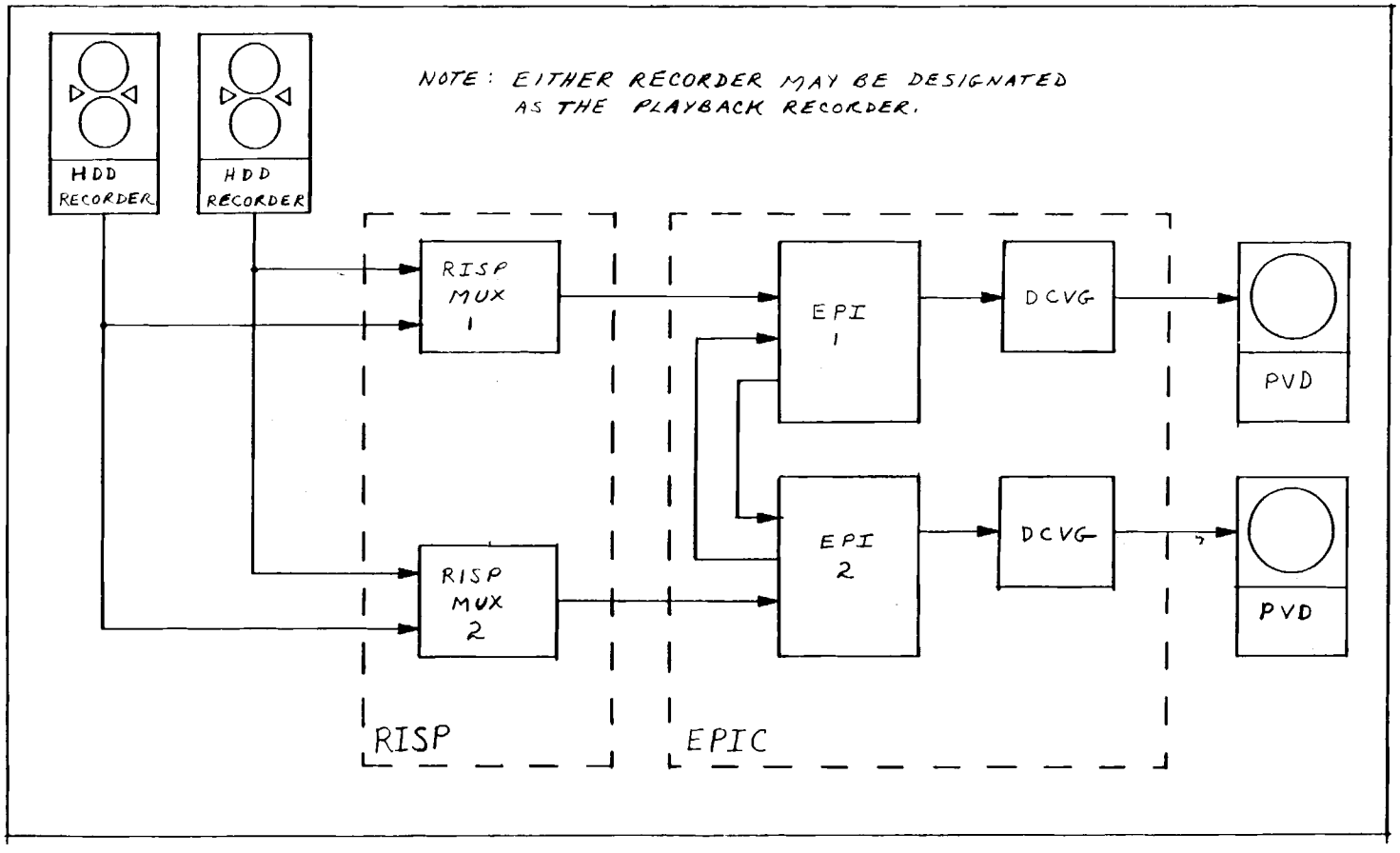


FIGURE 4-2A. PLAYBACK ELEMENT OPERATION — PLAYBACK MODE

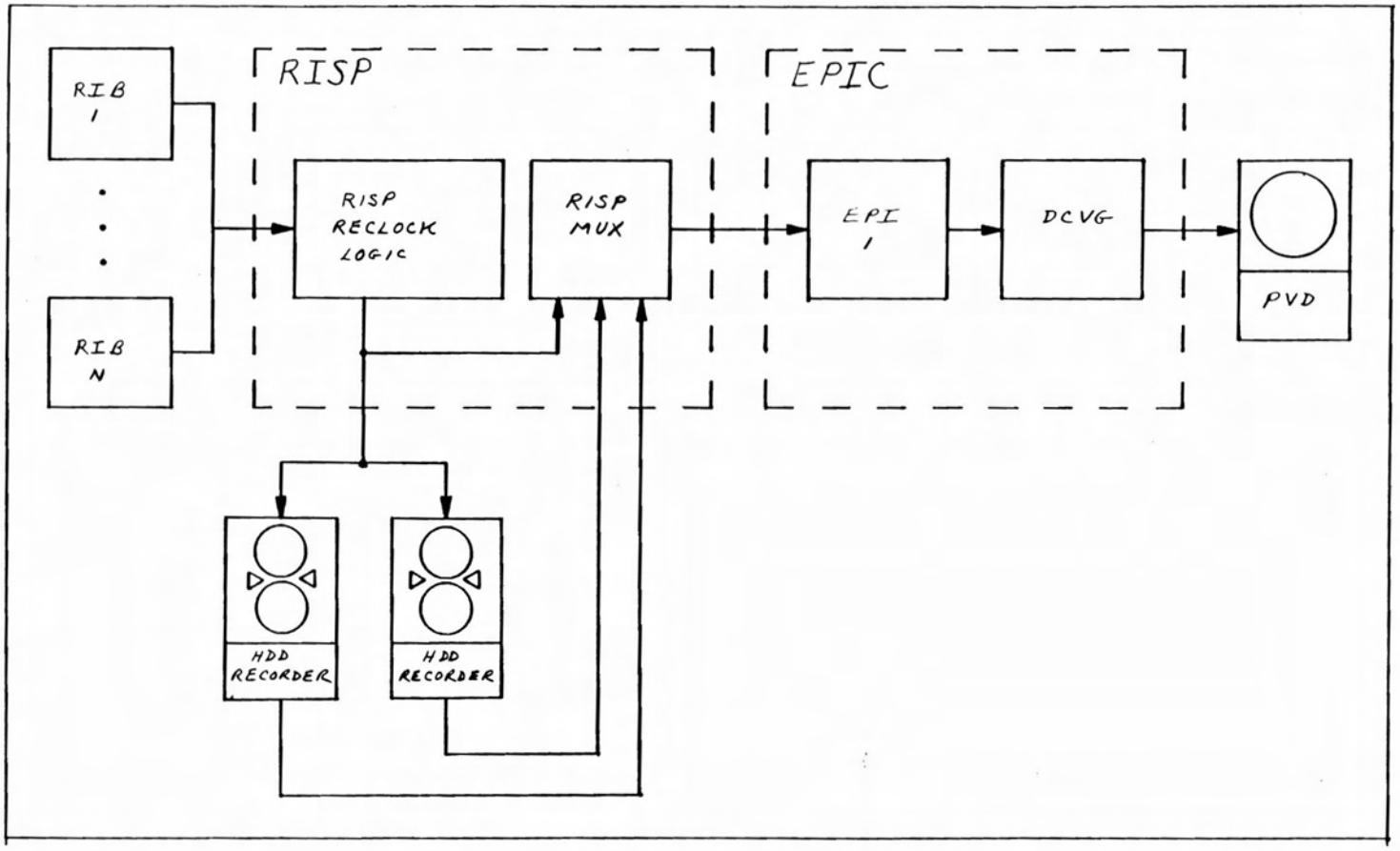


FIGURE 4-2B. PLAYBACK ELEMENT OPERATION — MONITOR MODE

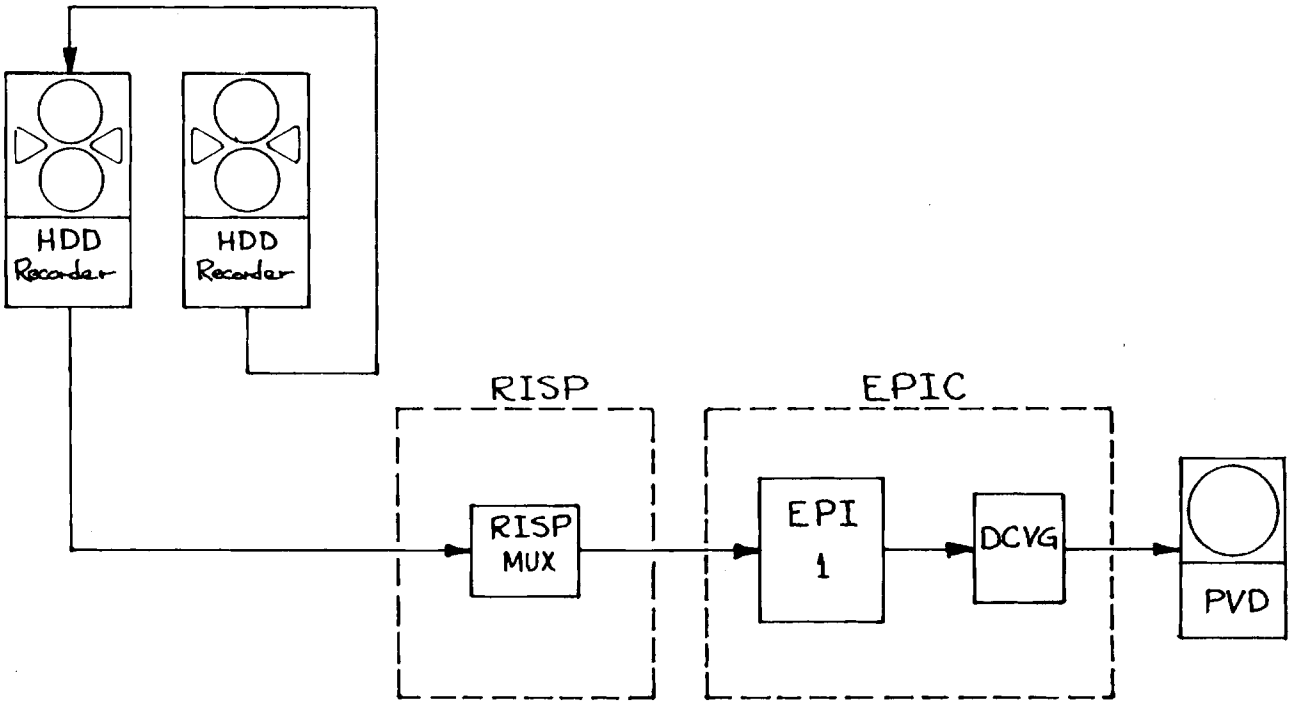


FIGURE 4-2C. PLAYBACK ELEMENT OPERATION --- DUPLICATION MODE

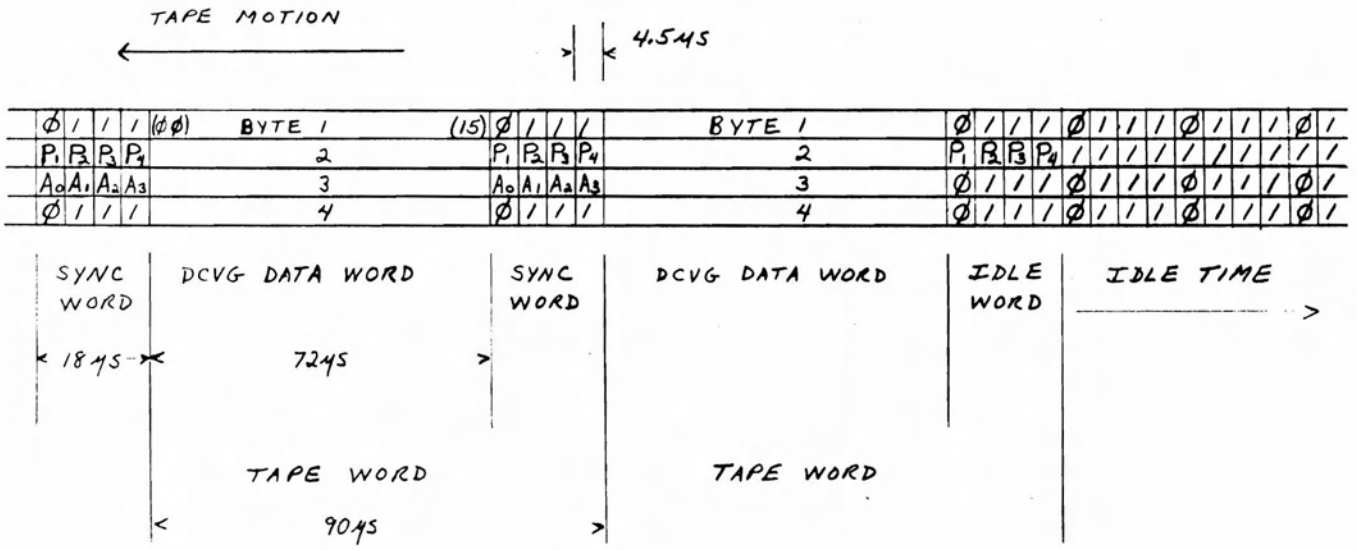


FIGURE 4-3. TAPE DATA FORMAT

address code is received on data line 3 in a serial manner with the least significant bit arriving first. The bits are labeled AØ through A3 starting with the least significant bit (LSB) and ending with the most significant bit (MSB). Bits AØ through A2 will be used to address one of six displays using codes ØØØ through 1Ø1. Bit A3 will be used for possible future expansion and for the present is set to zero. Data lines 1 and 4 carry sync code information. The sync code is a four bit code which is used to designate the presence of a sync word. The sync code is Ø111 (LSB through MSB), with the least significant bit sent first. The idle time is defined as periods of time when no DCVG data is available to be recorded. During idle time, the address bits AØ through A3 in the sync word will be set to the sync code Ø111. Data line 2 carries parity information for the previously received DCVG word. The four bits are labeled P1 through P4 and represent parity for each of the four DCVG data bytes on data line 1 through 4 respectively. The parity for a particular DCVG word is presented in the sync word immediately following each DCVG data word.

4.1.2 Data Selection. - The selection of signal sources to be monitored or displayed by the playback element is accomplished using an array of multiplexers. The multiplexers are controlled by address selection logic within the EPIC. Each source consists of four data lines comprising a Port as defined earlier. There are eighteen distinct primary sources of data. These are grouped into three groups of six. Group A constitutes the output bus from Recorder A; Group B forms the output bus from Recorder B. Group C is the common input bus to both recorders. Each of these groups has a single common clock for all the ports in the group.

For each EPI there are three levels of multiplexing. Figure 4-4 shows the data flow through these three levels of multiplexing. For EPI-1, the first level consists of three multiplexing circuits - MUX-A1, MUX-B1, and MUX C. MUX-A1 is used to select one out of six ports in Group A, which is the output of Recorder A. MUX-B1 is used to select one out of six ports in Group B, which is the output of Recorder B. MUX-C is used only in the monitor mode, when by-passing of the recorders is desired. It enables selection of one out of six ports in Group C, which is the input to both recorders. The outputs of these three multiplexers feed the next multiplexing level consisting of a single circuit called MUX-D1. This multiplexer is used to select between the three sources of data - the outputs of MUX-A1, MUX-B1, and MUX-C. The same functions performed by MUX-A1, MUX-B1, and MUX-D1, are performed for EPI-2 by MUX-A2, MUX-B2, and MUX-D2, respectively. There is no multiplexer associated with Group C for EPI-2, hence EPI-2 does not have direct access to the data sources at the inputs to the recorders. All of these multiplexers (MUX-A1, B1, C, D1, A2, B2, and D2), which comprise the first two levels of multiplexing, are contained in the RISP cage.

The third level of multiplexing consists of two circuits, MUX-E1 and MUX-E2, which are contained in EPI-1 and EPI-2 respectively. MUX-E1 is used by EPI-1 to select between a primary input, which is the output of MUX-D1, and an auxiliary input, which is the output of MUX-E2 in EPI-2. The primary input is used for playback and the monitoring of the record operation. The auxiliary input is used to monitor the functional performance of the data channel associated with EPI-2. MUX-E2 performs this same function for EPI-2.

Multiplexing levels 1 and 2 are described in more detail in paragraph 4.2.2. Level 3 is described in paragraph 4.2.3.1.2.

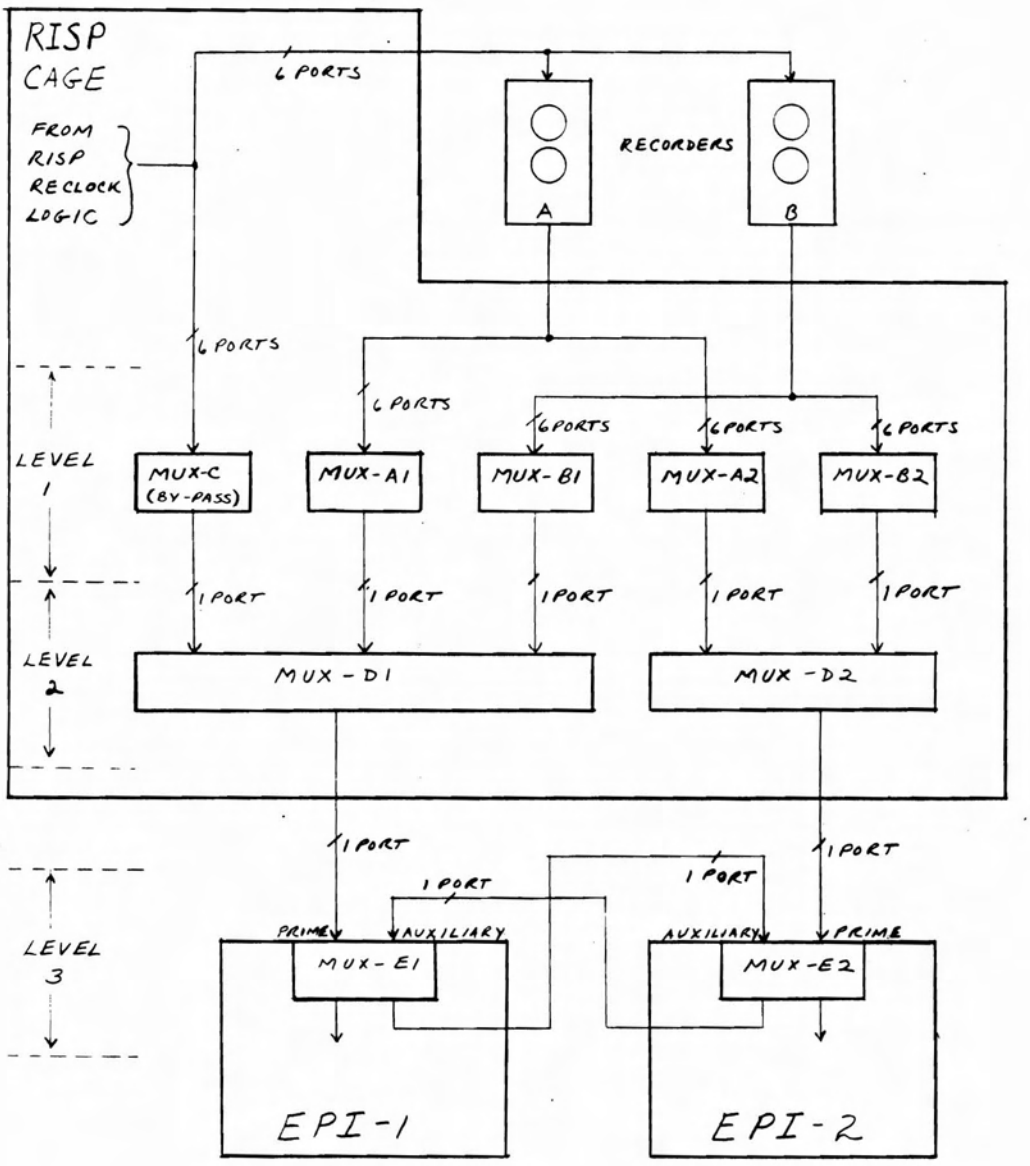


FIGURE 4-4. DATA SELECTION

4.1.3 Alternating Memories. - The data received from tape by the EPI is stored in one of two semiconductor memories. When this memory has received a complete frame of data, the EPI will use this data to refresh the playback PVD via a DCVG. While the EPI is refreshing the display with data from the first memory (M1), it will simultaneously be storing the next frame of data from tape in the second memory (M2). When M2 has received a complete frame of data, the EPI will switch over to M2 for refreshing the display, and then proceed to load the next frame into M1. The EPI alternates between M1 and M2 in this manner as long as data is being received from the recorder or until operator intervention. A memory is considered full when it has received a complete frame of data, even though the memory may not be actually filled to capacity. The EPI alternates between memories (and between frames) at a rate which is equal to the sample rate used by the Record Element.

4.1.4 Playback Update Modes. - The EPI is designed to operate in three time modes: real-time, freeze, and twice-real-time. In the real-time mode, the playback tape speed is the same as the record tape speed, and the data is read from tape at the same rate at which it was recorded. Therefore, the playback display data is updated at the same rate as the data was sampled by the RIB.

In the freeze mode the EPI is continuously refreshing the display from a single memory without alternating. When the operator initiates the freeze mode, the EPI will freeze the frame that is currently being used to refresh the display while it continues to load the other memory with the next frame sent by the recorder. When the second memory is full, the EPI will ignore any further data sent by the recorder. The recorder is not automatically halted. Once an EPI is placed in the freeze mode, the operator may manually switch between the two memories and view each of the two frames stored for any length of time. Each EPI can be placed in the freeze mode independently via individual freeze controls or both can be placed in the freeze mode simultaneoulsy via a master freeze control. When released from the freeze mode, the EPI will switch to refresh the display from the alternate memory. It will then proceed to load the next frame of data coming from the recorder into the memory from which it had been refreshing prior to the release.

In order to place the EPI in the twice-real-time mode, the tape speed is changed to twice the speed of the real-time mode. At this speed the data will be received by the EPI at twice the rate of the real-time mode and the display will be updated at twice the rate at which the data was sampled. When a speed change is made to place one EPI in the twice-real-time mode, the other EPI will automatically be placed in the twice-real-time mode if it is receiving data from the same recorder.

4.1.5 DCVG Interface. - In refreshing the PVD, the EPI is designed to emulate the refresh subsystems of the CDC, DCC, and DARC systems. The output section of the EPI emulates the interface between the memory containing the refresh data and the DCVG in the refresh subsystem. The operation of the refresh subsystem is discussed in Appendix A. As part of the emulation of the refresh subsystem, the EPI is designed to provide the following:

> Refresh Rate - Each EPI contains a circuit which is designed to provide a refresh rate clock with a period adjustable in 21.6 microsecond steps. The range of the clock will be 11.3 Hz to 55.1146 Hz. Variations in the clock frequency are available for maintenance purposes only. The nominal clock rate is fixed and not adjustable by the operator. The EPI uses the

basic 4.444 MHz clock to generate the refresh clock. The actual refresh rate used by the EPI in normal operations depends on the W/B setting and is automatically adjusted to match the characteristics of both the CDC and DCC systems. The EPI is also capable of refreshing in the asynchronous mode as described in Appendix A.

Access Assignment Table.- The EPI contains a circuit which is designed to emulate the access assignment table. This circuit is used by the EPI to determine when its associated DCVG can access the memories in the EPI. The circuit is designed to provide timing as close to the refresh subsystem timing as possible.

Blink Clock. - Since the blink clock in each DGU can be varied from 0.25 Hz to 12.5 Hz independently of the other DGU's, each EPI is designed with its own variable blink clock. The range of frequencies for each of these blink clocks is 0.22 Hz to 25 Hz. The EPIC is designed with a master/slave option which allows the flexibility of having either an independent blink clock generated for each EPI or having one EPI use the blink clock generated for the other. In either case the blink clock can be manually adjusted to match the blink rate in the DGU from which the data was recorded.

Data Transfer. - The EPI is also designed to transfer 16-bit bytes at a 4.444 MHz rate. It also supplies the VAD signal to the DCVG during the first byte time of a data transfer.

Parity Error. - The EPI is designed to examine the parity of each 64-bit word transferred between the alternating memories and the DCVG. If a parity error exists, it will generate the error signal at the proper time.

4.2 Detailed Description.

4.2.1 High Density Digital Recorders. - For a description of the recorders see paragraph 3.5.

4.2.2 RISP Multiplexing Circuits. - As described in paragraph 4.1.2, the first two levels of multiplexing used in the selection of data for the EPI are contained in the RISP. This multiplexing is shown in Figure 4-5. As shown, there are two boards in the RISP called RISP Data Multiplexer-1 (RDM-1) and the RISP Data Multiplexer-2 (RDM-2). RDM-1 contains three multiplexing circuits - MUX-A1, MUX-B1, and MUX-D1. MUX-A1 and MUX-B1 are both 6-to-1 multiplexers and each consists of four 8-to-1 multiplexing circuits, with two inputs unused in each circuit. The output of each circuit represents one of the four data lines of the selected port. This is shown in Figure 4-6 for MUX-A1. MUX-B1 is identical to MUX-A1. MUX-D1 is a 3-to-1 multiplexer consisting of five 4-to-1 multiplexing circuits, with one input unused in each circuit. Four of these circuits are used to select between the outputs of MUX-A1, MUX-B1, and MUX-C. These multiplexers carry data only. The fifth circuit in MUX-D1 is used to select between the common clocks which come from either Recorder A, Recorder B, or the RISP Reclock Logic, which supplies the inputs to both recorders. This multiplexing operation is shown in Figure 4-7. The output of RDM-1 is sent to the Input Data Multiplexer board in the EPI (see paragraph 4.2.3.1.2).

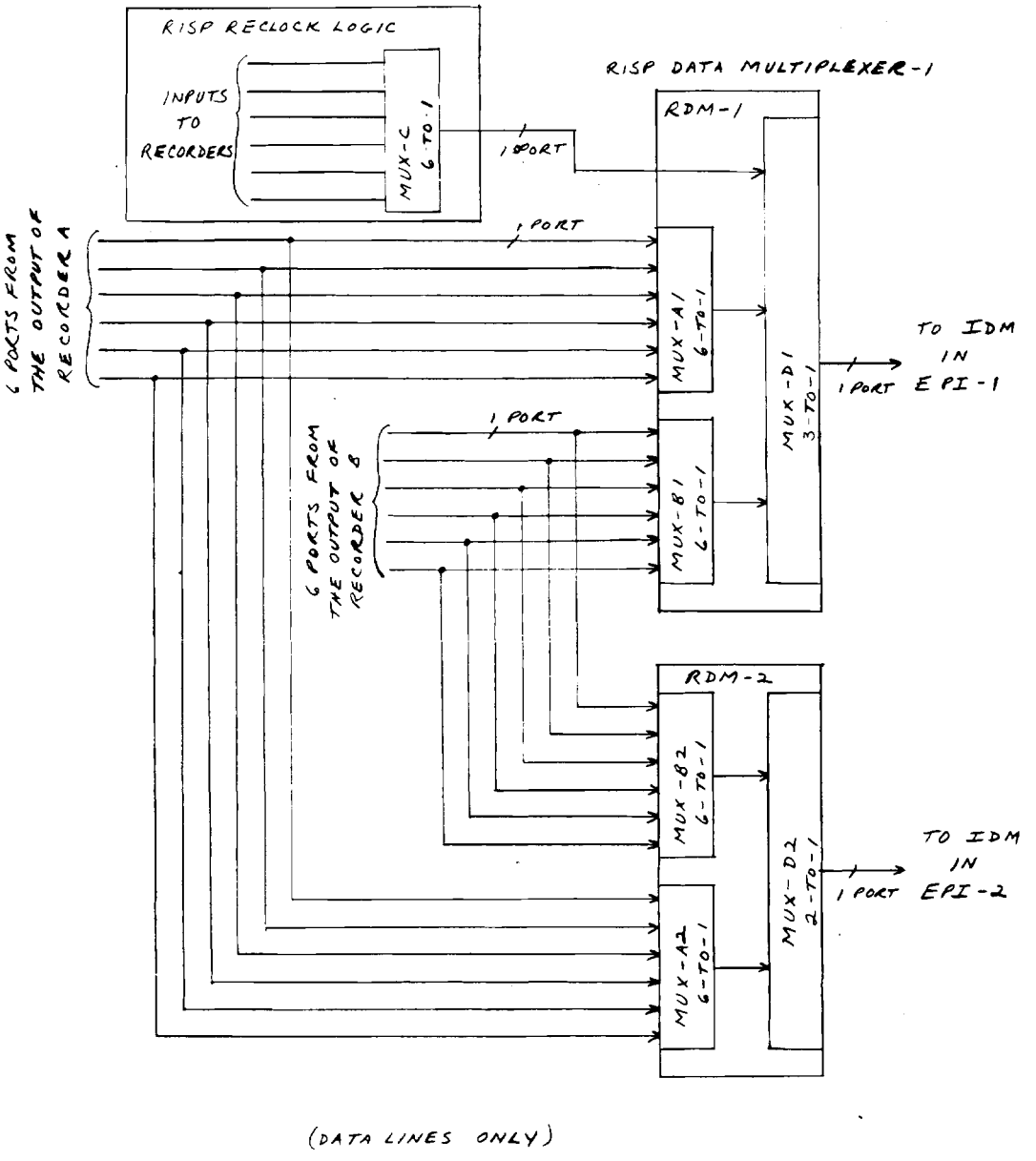
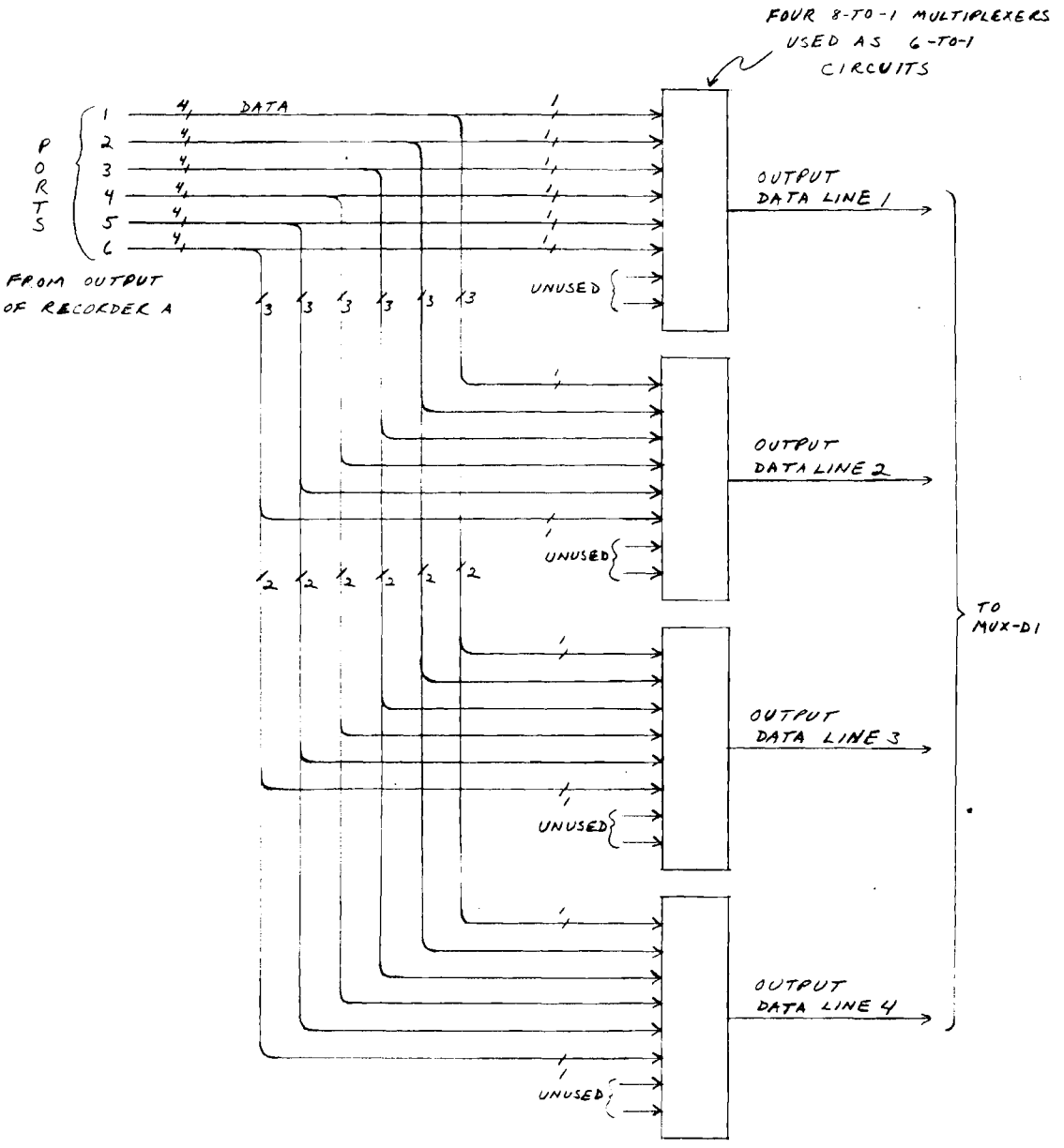
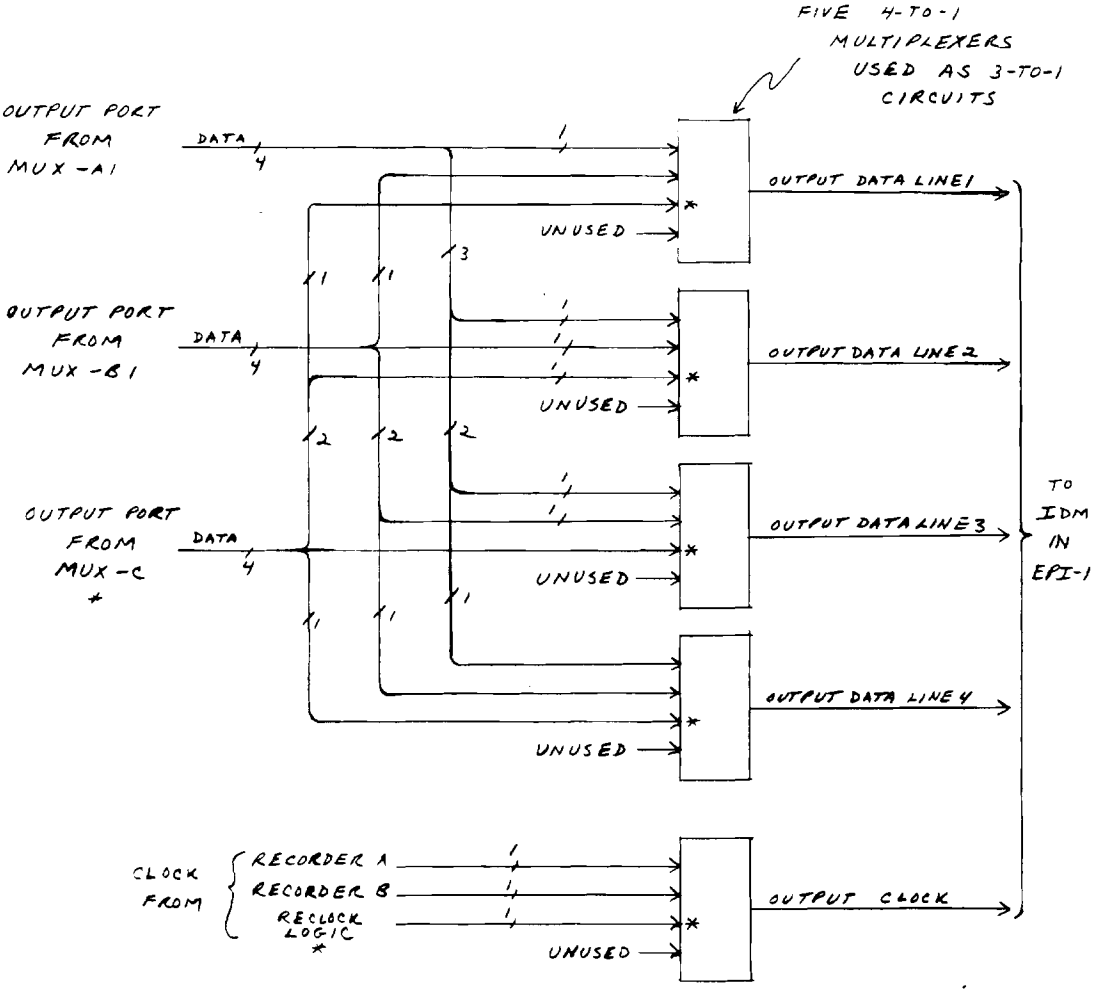


FIGURE 4-5. RISP MULTIPLEXING CIRCUITS



(TYPICAL OF TYPES A AND B MUX CIRCUITS)

FIGURE 4-6. MUX-A1



* THESE INPUTS ARE UNUSED FOR MUX-D2. OTHERWISE MUX-D2 IS IDENTICAL TO MUX-D1

FIGURE 4-7. MUX-D1

RDM -2 performs the same function for EPI-2, except that MUX-D2 is used as a 2-to-1 multiplexer with no input from MUX-C. Like MUX-D1, MUX-D2 uses five 4-to-1 multiplexing circuits, hence two inputs are unused in each circuit. However, one of the unused inputs in each circuit is brought to the card edge connection so that these circuits can be used as 3-to-1 multiplexers. This allows the use of a common type board for both RDM-1 and RDM-2, thus making these boards identical and interchangeable.

MUX-C is contained within the reclock logic portion of the RISP. It operates as a 6-to-1 multiplexer and consists of eight 4-to-1 tri-state multiplexing circuits, each operating as a 3-to-1 multiplexer. These circuits are grouped into two groups of four, with each group used to select data from one of three ports. Each of the four circuits within a group provides one of the four data lines of the output port of that group. Corresponding output lines of the two groups are tied together and the tri-state operation of the circuits is used to perform a 2-to-1 multiplexing operation in order to complete the required 6-to-1 multiplexing function. This is shown in Figure 4-8. MUX-C is used to select one of the six ports used as inputs to the recorders.

There are five control lines sent by each EPI to control the multiplexing in the RISP. Three lines (the Port Select lines) from EPI-1 are used to control MUX-A1, MUX-B1, and MUX-C, as shown in Figure 4-9. Using this configuration, the same port is selected on all three multiplexers simultaneously. The remaining two lines (the Source Select lines) are used to control MUX-D1. The same type of configuration is used for EPI-2 except that the Port Select lines are used to control MUX-A2 and MUX-B2 only. There is no connection to MUX-C.

4.2.3 Enroute Playback Interface Console. - The EPIC contains the following units:

2-Enroute Playback Interfaces

1-Master Control Panel with State/Fault Indicators

2-Display Control/Vector Generators

The description of these items is as follows:

4.2.3.1 Enroute Playback Interface. - Each EPI is divided into five sections:

1. Master Clock Section
2. Input Section
3. Memory Section
4. Output Section
5. Control Section

All five sections are interactive. Figure 4-10 is a detailed block diagram of the EPI. The following paragraphs describe this figure.

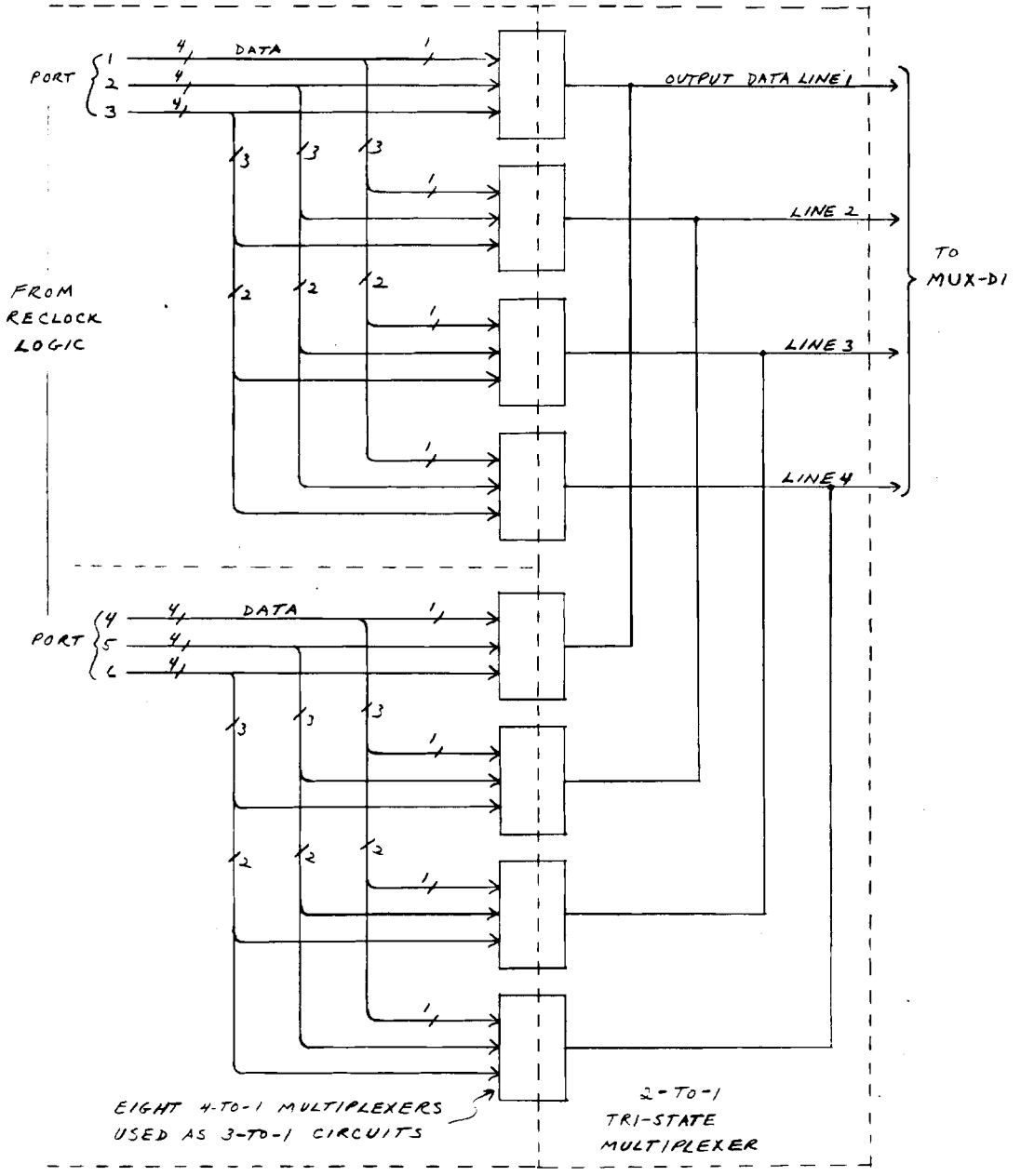


FIGURE 4-8. MUX-C

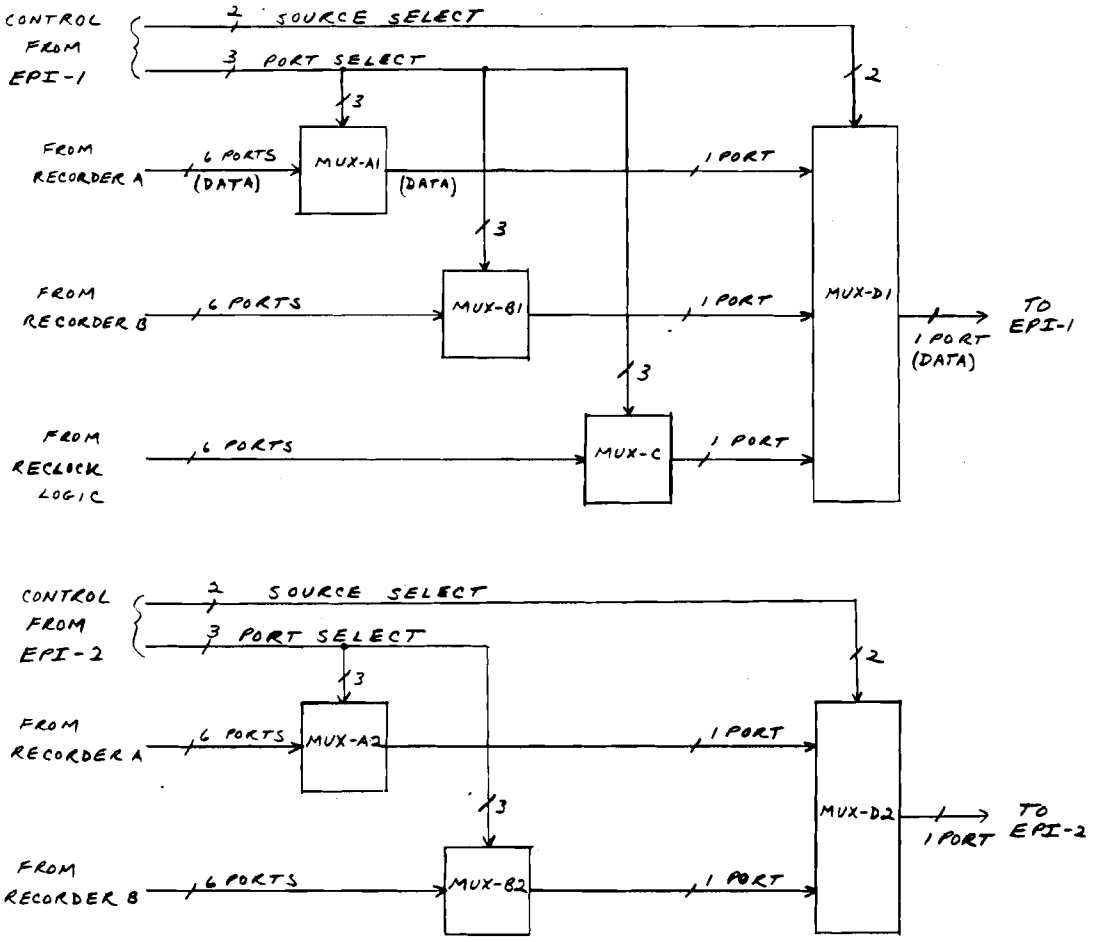


FIGURE 4-9. RISP MUX CONTROL

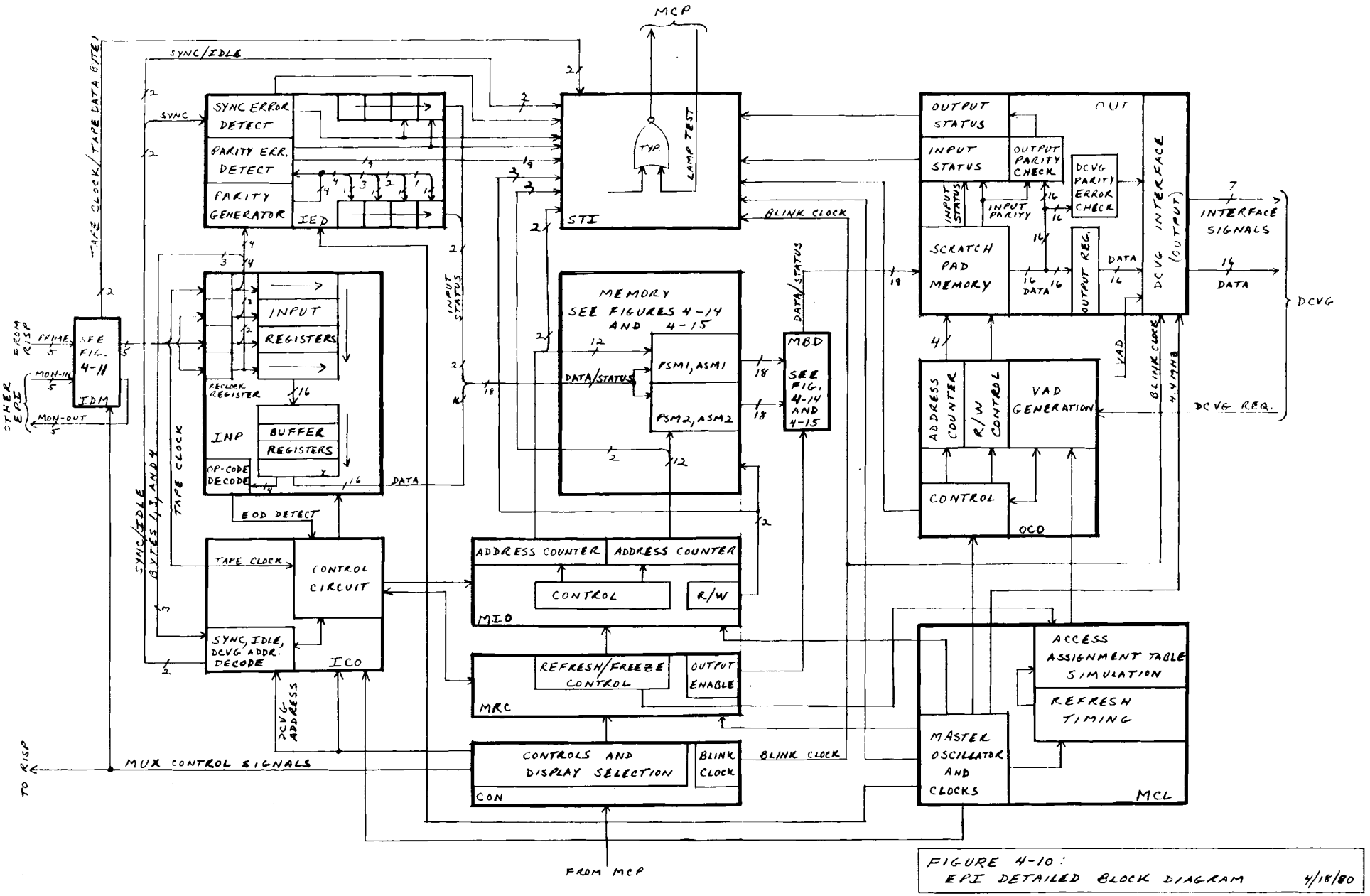


FIGURE 4-10:
EPI DETAILED BLOCK DIAGRAM 4/18/80

4.2.3.1.1 - Master Clock Section. - The master clock section consists of one board - the Master Clock (MCL) board. This board contains the master oscillator from which all internal clock signals with the exception of the blink clock, are derived. The clock signals generated on this board are as follows:

Signal Name	Frequency	Period (nsec)	Note
C56.25N	17.777 MHz	56.25	
C112.5N	8.888 MHz	112.5	
C225N	4.444 MHz	225	
C450N	2.222 MHz	450	
C900N	1.111 MHz	900	
C1800N	555.5 kHz	1800	
PC225ND1	4.444 MHz	225	Delay 1
PC225ND2	4.444 MHz	225	Delay 2

The two clock signals, PC225ND1 and PC225ND2 are pulsed clocks with their leading edges 180° out of phase with each other, and are used to drive the interface to the DCVG in the output section. The duty cycle of these pulsed clocks is 25%. The final output clock is derived from PC225ND1 after it is delayed and reshaped. The clock signal C56.25N is generated by a 17.777 MHz crystal oscillator. All other clock signals listed are derived from C56.25N. Also generated on this board is the refresh clock and the simulated access assignment table signals. These signals are also derived from C56.25N.

4.2.3.1.2 - Input Section. - The input section consists of four circuit boards--The Input Data Multiplexer (IDM) board, the Input (INP) board, the Input Control (ICO) board and the Input Error Detection (IED) board.

Input Data Multiplexer Board - The IDM board corresponds to MUX-E1 or E2 described in paragraph 4.1.2. It is used by the EPI to select data from one of two sources. The primary data source is the RISP cage which contains multiplex circuits which channel data from the recorders. (See paragraph 4.2.2). The secondary data source is the monitor output of the other EPI in the EPIC. Each of these data sources provides four data lines and one clock line (one port). The IDM board contains five 4-to-1 multiplexing circuits - one for each data line and clock line of the port. Since the IDM must act as a 2-to-1 multiplexer, two inputs to each multiplex circuit will be unused. Figure 4-11 shows the data paths connected with the IDM board.

Input Board - The INP board contains a 4-bit parallel reclocking register, a group of four 16-bit serial-in, parallel-out (SIPO) shift registers called the input registers, and a group of four 16-bit parallel-in, parallel-out (PIPO) shift registers called the buffer registers.

Incoming data from the recorder is first synchronized with C900N clock signal generated by the MCL board by shifting the data through the 4-bit

wide reclocking register. Data on each data line will be shifted through a separate stage of this register. Transitions in the reclocked data appear approximately 112.5 nsec after the rising edge of the reclocked tape clock generated by the ICO board. This reclocking will be described in more detail in later paragraphs.

After the reclocking, data from each of the four lines is shifted serially into one of the four input registers. When 16 bits of data have been shifted into each register, the data is shifted in parallel to the buffer registers. The buffer registers hold the data while circuits on the ICO and IED boards check for sync and error conditions. Under the control of the ICO board, this data is shifted in parallel through the buffer registers to one of the alternating memories in 16-bit bytes. A diagram of the data flow is given in Figure 4-12. A description of the data flow from the memories to the DCVG will be given later.

The INP board also has a circuit which detects the "End of Data" (EOD) word in the incoming data. This detection is done at the output of the buffer registers and a signal is sent to the memory section to designate when a memory is full.

Input Control Board - The ICO board controls the data flow from the IDM board, through the INP board, to the memory section. It uses a combination of clock signals sent by the recorder and the MCL board to generate the clock signals needed to shift data through the input section. A clock signal derived from the tape clock is used to shift data into the input registers. All other clock signals are derived from the output of the MCL board.

The ICO board contains a circuit which synchronizes the rising and falling edges of the tape clock with the rising edge of the C900N clock signal. Transitions in the reclocked data are made to occur approximately 112.5 nsec after the rising edge of the relocked tape clock. The reclocking of the tape clock and data is done to provide a fixed relationship between all signals present in the EPI. Figure 4-13 shows the relationship between the various signals involved in this reclocking operation. CTC is the signal name for the clock "tape clock." GCSTC is the signal name for the gated clock "synchronized tape clock" which is the signal derived by reclocking the tape clock to coincide with the timing of the C900N clock. The GCSTC is gated off when the EPIC is placed in the freeze mode. CDSC is the clock "data synchronization clock" which is used to reclock the tape data to synchronize the data with the timing of the C900N clock. STDX is the signal "tape data X" which is the tape data received on data line X of a port(where X ranges from 1 to 4); SSTDX is the signal "synchronized tape data X" which is the reclocked tape data. GCIRWC is the gated clock "input register write clock" which is used to shift data into the input registers. It is gated on and off at the appropriate time by signals generated by the ICO and IED boards. The arrows in Figure 4-13 are used to show which events trigger changes in the various signals.

Besides providing clock signals to shift data through the input and buffer registers, the ICO board generates signals used by the memory section to increment the memory address counter. This address counter is used to designate where each data byte is to be stored in memory.

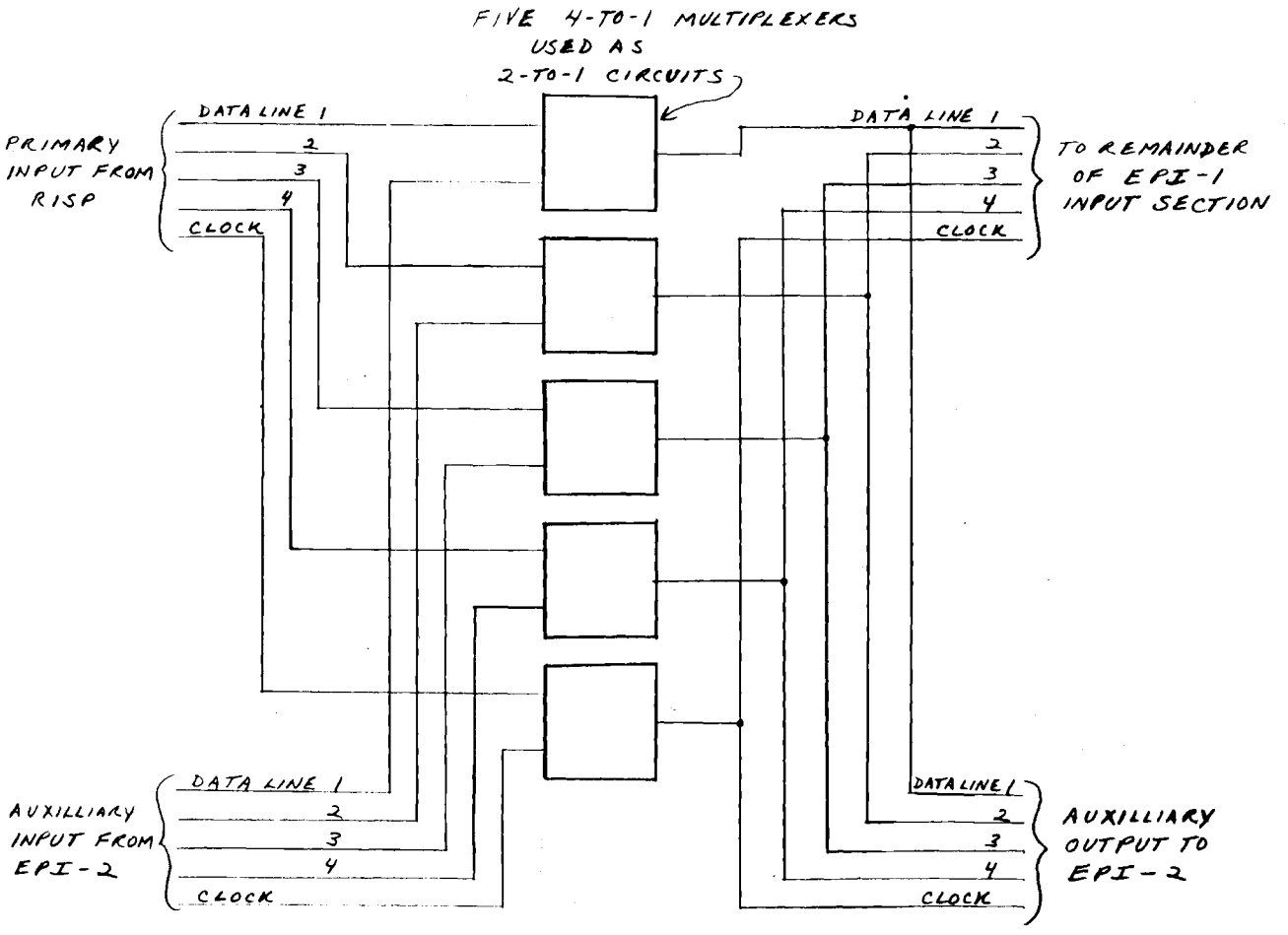


FIGURE 4-11. INPUT DATA MULTIPLEXER FOR EPI-1

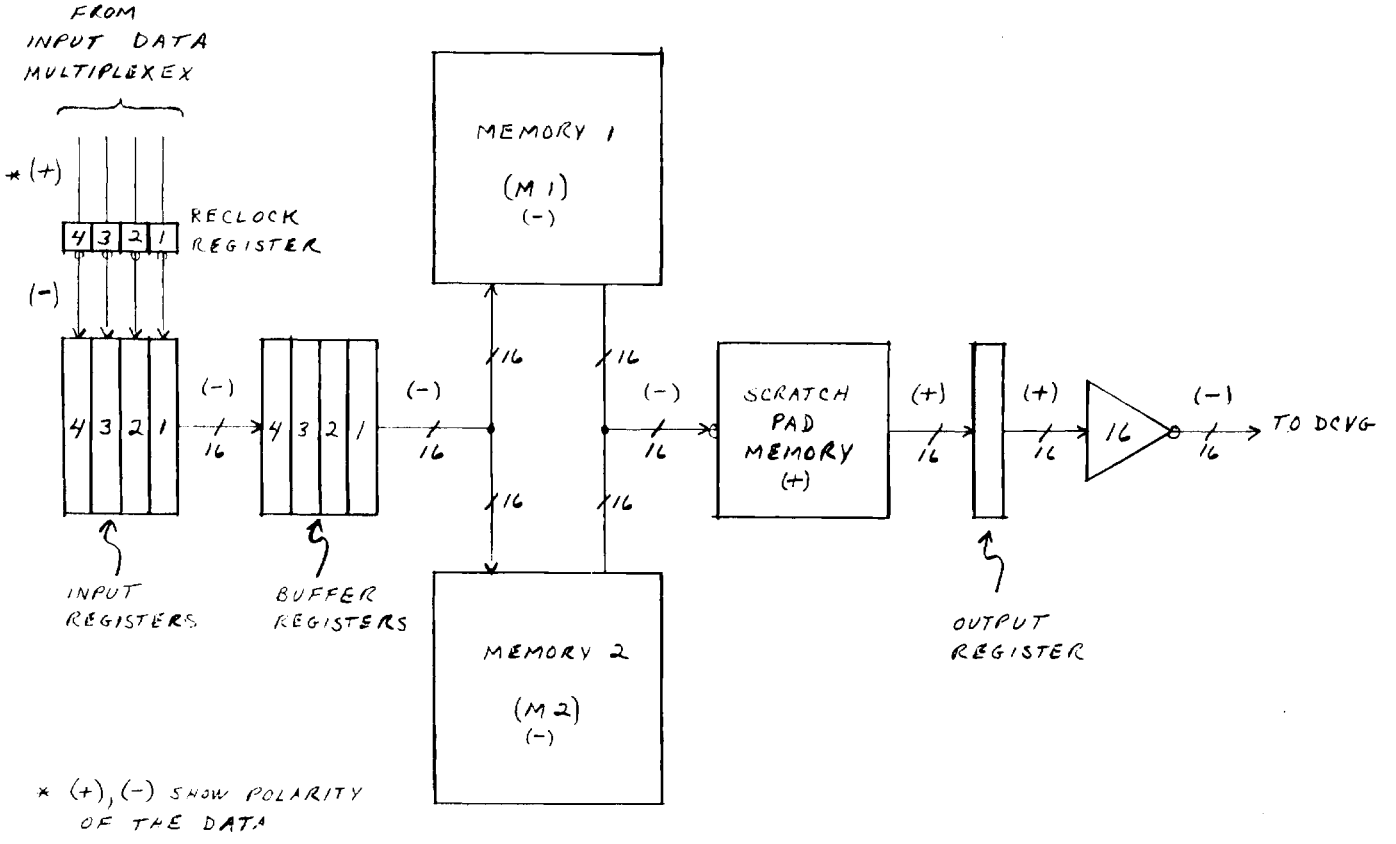
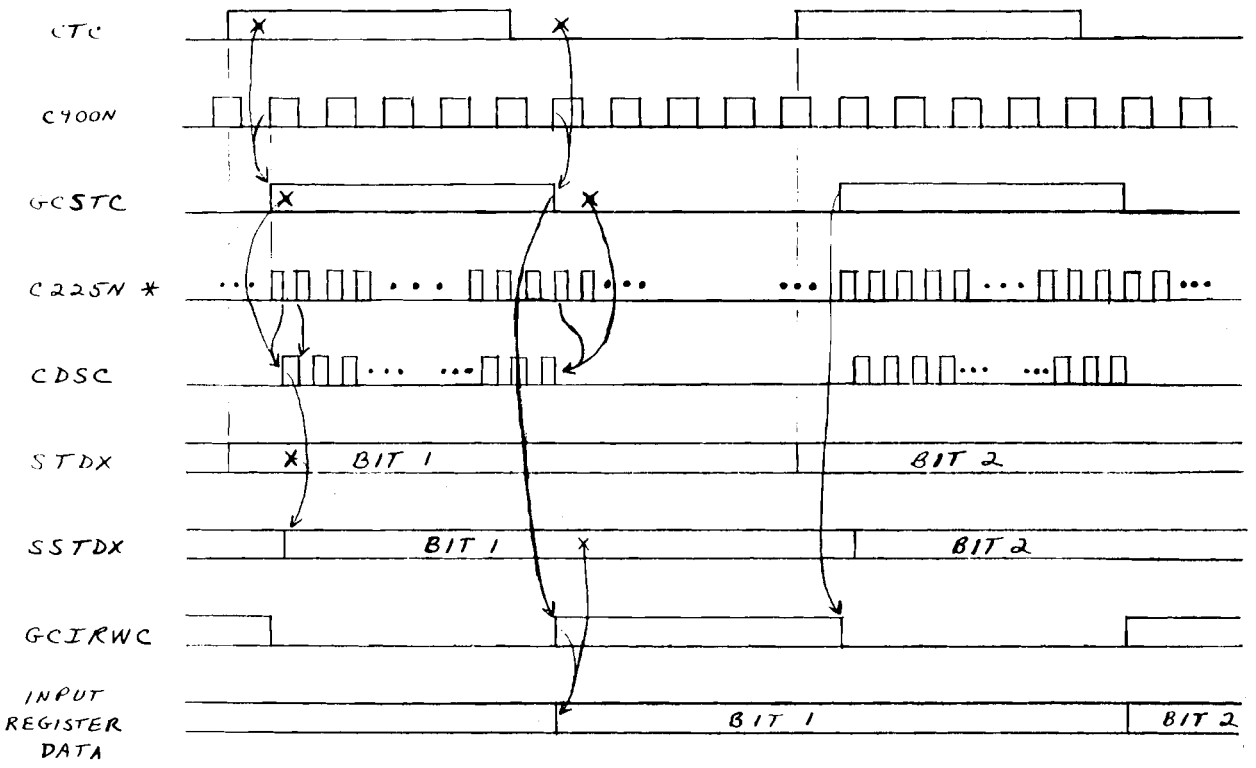


FIGURE 4-12. DATA FLOW THROUGH THE EPI



* PULSE WIDTHS ARE EXAGGERATED

FIGURE 4-13. INPUT RECLOCKING

The ICO board also contains circuits used to count the number of bits received by the input register and the number of bytes transferred between the input and buffer registers, and between the buffer registers and the memories.

Finally, there are circuits which are used to detect and decode the sync words present in the incoming data. These circuits enable the ICO board to determine when to start shifting data into the input registers. Part of the decoding will be to determine if the DCVG address code matches the code selected by the operator.

The input registers are loaded immediately following a sync word. After 16 bits are loaded into the input registers, the data bits are shifted into the buffer registers. When another sync word is detected, the data bits are then transferred from the buffer registers to the memory.

The sync decoding circuit is designed to detect multiple sync words to ensure that sync data is not mistaken for DCVG data. If two sync words are sent before a data word, the loading of the input registers will be initiated after the first is detected and reinitiated after the second is detected. The data in the buffer registers is transferred to memory only on the detection of the first sync word received after the buffer registers have been loaded. There is also a sync inhibit circuit which guards against falsely decoding sync if the sync pattern happens to appear in the DCVG data. The sync code was selected to insure against the possibility of its appearing as valid data in the first 4-bit position of the first byte of the DCVG word. This byte contains the DCVG op-code and there is a limited number of combinations that the first four bits can take.

Input Error Detection Board - The IED board contains circuits which generate and store parity for the input data and detect and store parity and sync errors. The parity information generated consists of four parity bits, one for each DCVG data byte loaded into the input registers. This parity information is stored in a shift register and sent to the memory section along with the data to enable a parity check on each byte at the output section of the EPI. There is also a circuit to compare this parity with the parity information found in byte two of the sync word which immediately follows the DCVG data word.

As the input parity is checked, any errors are stored in a 6-bit error register. There is a bit position in the register to store an error condition for each of the four data bytes. The fifth bit position is used to store a common error condition and is set whenever any of the first four bit positions are set. The sixth position is used to store a sync error condition. This condition occurs whenever the IED board determines that a sync word was detected at the wrong time. The state of this register changes with each word that is received by the input registers. In order to present a visual indication of these six error conditions, a second register is used which holds each error condition from the time it first occurs in an input frame until the EPI switches memories after the input frame is completely stored. The reason for using this register is because the original error conditions are momentary and occur too fast to be visible. The second register gives persistance to the error indication. It should be noted however, that the

error indicator does not give a quantitative account of the errors but only indicates that the EPI has detected at least one of a particular error condition in a frame. In order to measure the quantity of errors, a counter must be attached to the pin on the backplane connectors which carries the desired instantaneous error condition signal which is an output of the first register. All error conditions stored in the second register are sent to indicators on the Master Control Panel via the control section of the EPI which contains the indicator drivers.

The EPI is designed to store two error bits along with each data word in memory. This is to allow an indication of the errors at the output. One error bit is derived from the common instantaneous parity error signal (reflecting an error in any of the four bytes of the word) and the other is derived from the instantaneous sync error signal.

4.2.3.1.3 - Memory Section. - The memory section consists of two parts: The memory portion and the control portion. The memory portion consists of two semiconductor memories (2 boards each), each containing 12,288 eighteen-bit bytes. The memory boards use the TMS-4044-20, which is a 4k x 1 bit, N-channel MOS memory IC with a typical read (write) cycle time of 200 nsec. and a tri-state output structure. One board in each memory, called the Primary Storage Memory (PSM) board, contains 36 memory IC's with a total capacity of 8192 eighteen-bit bytes or 2048 DCVG words with parity and error bits. The second board, called the Auxiliary Storage Memory (ASM) board, contains 18 memory IC's with a total capacity of 4096 bytes or 1024 words. The PSM board has enough capacity to handle the normal data load for the DCVG. The ASM board is used only when this capacity is exceeded, as in the case when the RIB is operating in the "wrap-around" mode (see paragraph 3.3.3). Each memory board is partitioned into two sections, each containing 2048 bytes. One section is unused on the ASM board. The capacity of the ASM can be increased to match that of the PSM in order to make the two boards interchangeable, but the EPI is designed to use a memory with a total capacity not exceeding 12,288 bytes. Each board also contains address decoding circuits which enable each section of memory to operate at the appropriate time. Data bits are read from memory in the same logic sense as they were written, and the read-out operation is non-destructive. These two memories operate in an alternating manner as previously described.

The control portion of the memory section consists of three boards - the Memory Input/Output Control (MIO) board, the Memory Refresh Control (MRC) board, and the Memory Bus Driver (MBD) board.

Memory Input/Output Control Board - This board contains circuits which generate all the clock signals needed to write and read data and increment the address counters. It also contains an address counter for each memory. A memory address counter can be controlled by either the input or the output section depending on whether the associated memory is being used to store data coming from the tape or to refresh the display. Circuits on the MIO board determine which section controls a particular counter.

Memory Refresh Control Board - This board contains circuits which monitor the status of each memory and designate which memory is refreshing the playback display. Part of the status that is monitored is whether a memory is full or empty. The circuit that designates which memory is refreshing is

part of the memory toggle circuit used to switch between memories. Switching between memories occurs when an EOD word is detected at both the input and the output sections. When this condition occurs, both memories will have completed a cycle. The memory assigned to the input section will have received a complete frame of data and will be ready for the refresh operation, and the memory assigned to the output section will have completed a refresh sycle and will be ready to receive data from tape. This board also includes a freeze circuit which inhibits the automatic switching between memories and allows for manual switching.

This board also contains circuits which generate the output enable signals which control the tri-state bus drivers on the MBD board.

Memory Bus Driver Board - This board contains two sets of 18 tri-state bus drivers. Each memory is assigned a set of drivers. The corresponding output lines of each section of 2048 memory bytes are tied together to form an input bus for each set of drivers. The corresponding outputs of both sets of drivers are tied together to form a common output bus between the memory section and the output section of the EPI. Figure 4-14 shows the general bus structure while figure 4-15 shows details of the bus operation.

4.2.3.1.4 - Output Section. - The output section consists of two circuit boards--the Output Control (OCO) board and the Output (OUT) board.

Output Control Board - The OCO board controls the flow of data from the memories through the OUT board to the DCVG. The OUT board contains a scratch pad memory which is used for temporary storage of data being read out of the memories. Whenever the scratch pad is empty, the OCO board will initiate a transfer of data to the scratch pad from the memory which contains the current refresh frame. The amount of data transferred at one time will depend on the W/B setting. When the scratch pad is full, the output control will wait for two signals to occur before initiating the transfer of data from the scratch pad to the DCVG. The first signal is a request from the DCVG for data; the second is the access enable signal generated by the access assignment table emulation circuit located on the MCL board. The DCVG data request signal must occur before the access signal. When the two signals occur in the proper order the OCO board will generate the VAD signal and send it along with the data to the DCVG.

This board contains circuits which control the read and write operations of the scratch pad and generate the various read and write clocks. This board also generates a clock which is used to increment the appropriate memory address counter in the memory section. The scratch pad address counter and the word and byte counters that are used to control the amount of data transferred through the output section are also located on this board.

Output Board - The OUT board, as previously mentioned, contains a scratch pad memory. This scratch pad has a capacity of four 64-bit words. It stores these words as sixteen 16-bit bytes. The board also contains a 16-bit output register which is used to reclock the data. This register allows the data lines to be synchronized with the other DCVG interface signals. The board also contains a parity check circuit which is used to generate the DCVG parity error signal. This error signal will be

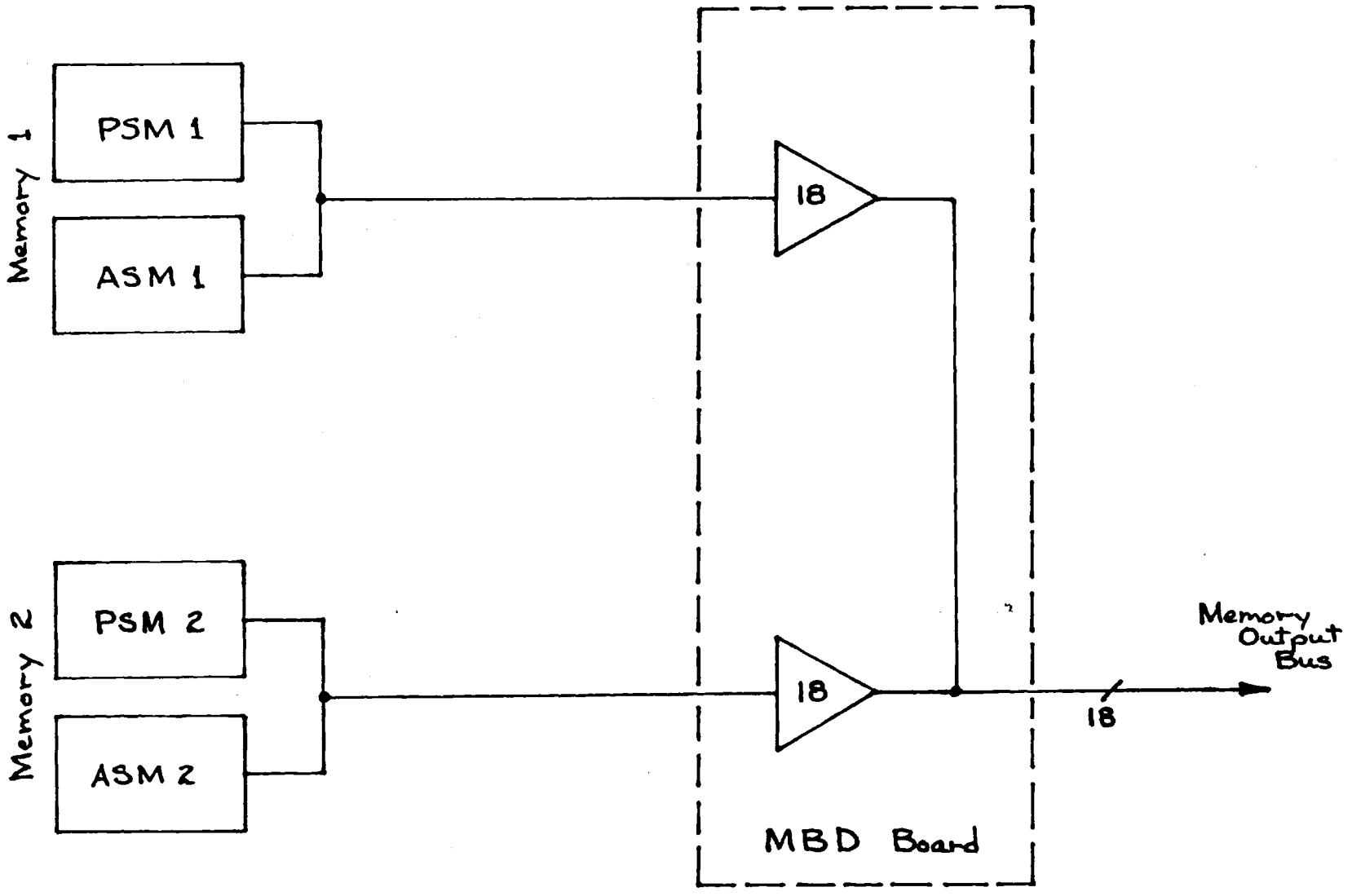


FIGURE 4-14. GENERAL BUS STRUCTURE — MEMORY BUS DRIVER (MBD) BOARD

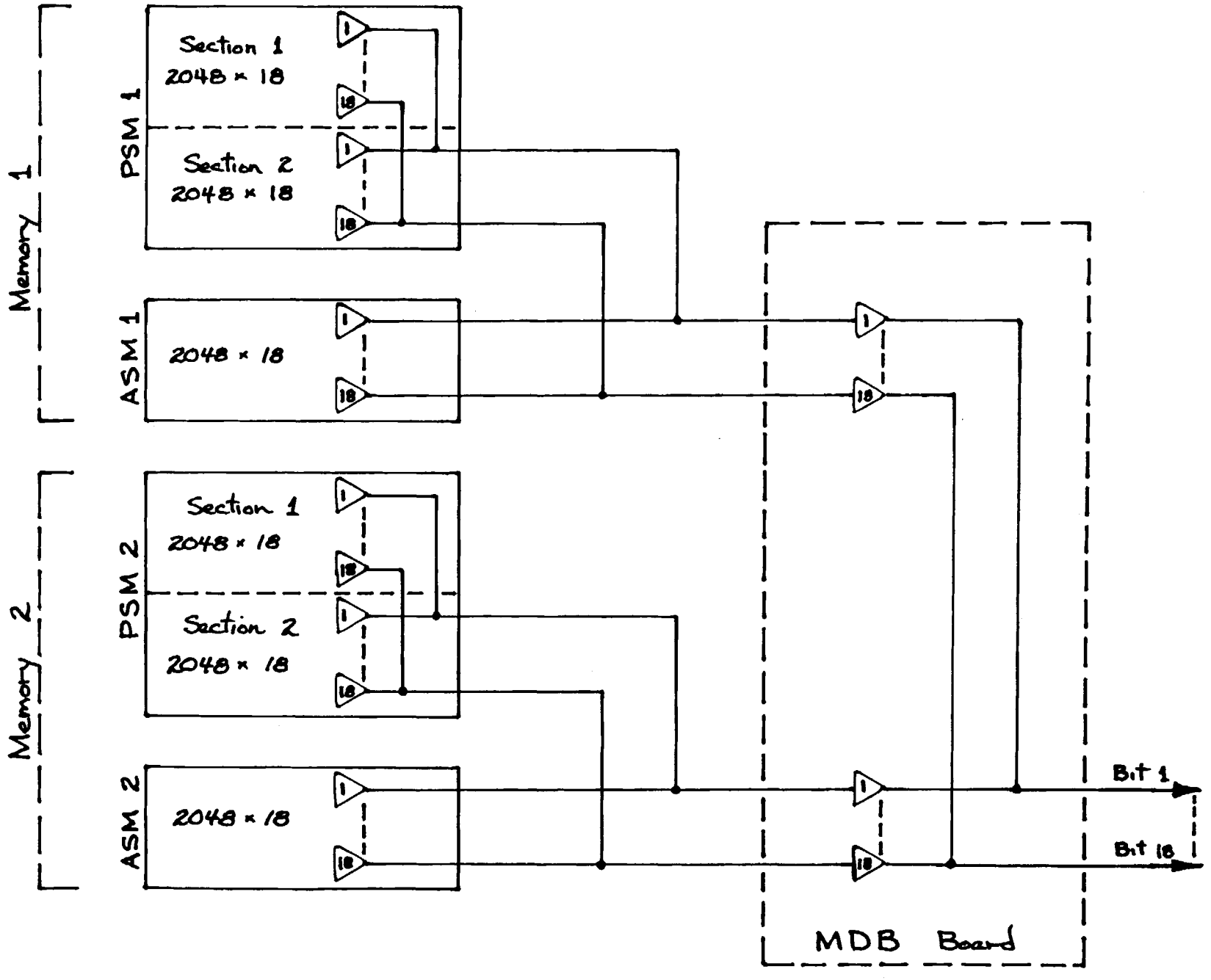


FIGURE 4-15. DETAILS OF BUS OPERATION — MEMORY BUS DRIVER (MBD) BOARD

transmitted to the DCVG during the first byte time of the word immediately following the word in which an error was detected. This parity is also checked against the parity generated at the input of the EPI. The input parity is stored in a second scratch pad along with the input error status. This data is stored at the same time the associated display data word is stored in the first scratch pad. A 4-bit register, similar to the error register used on the IED board, is used to store four instantaneous error conditions. These conditions are input error (word basis), input sync error, EPI parity error (difference in the parity generated for a word at the input and output), and DCVG error. The outputs of this register are sent to the Control Section to be stored in a second register which operates in a manner similar to the second register present on the IED board.

There is also a circuit which decodes the EOD word at the scratch pad input and signals the memory section that the EPI has completed the refreshing of a frame on the display.

Finally, there are buffer drivers which drive the interface lines to the DCVG. The interface signals which are sent include:

1. Valid Address (Z/VAD)
2. 4.444 MHz clock (Z/4.4 clk)
3. Parity Error (Z Par Err)
4. Data (Z/IBØØ through Z/IB15) 16 lines
5. Blink Clock (Z B Clock)
6. Master Reset (Z/MSTRSET)
7. W/B signals (Z/W/B MSB, Z/W/B LSB) (2 lines)

The VAD is generated by the OCO board. The 4.444 MHz clock is generated by the MCL board and reshaped on the OUT board. The parity error and data signals are generated by the OUT board. The blink clock, master reset and W/B signals are generated by the Control Section. The only interface signal generated by the DCVG is the data request signal received by the OCO board.

4.2.3.1.5 - Control Section. - The Control Section consists of two boards - the Status Indicator (STI) board and the Control (CON) board.

The STI board contains indicator drivers for all error and status signals sent to the Master Control Panel for display. It also contains the latch circuits used to temporarily store the instantaneous sync error and parity errors detected at the output of the EPI as described in paragraph 4.2.3.1.4 (Output Section - Output Board). Besides providing drivers and latches, the STI also performs some error and status checking. It contains two circuits which monitor the two memory address counters and detect an overflow condition. It also contains clock fail detection circuits--one for the input tape clock (CTC) and one for the basic 225 nsec clock (C225N) used in the EPI. A similar circuit is used to detect the presence of data at the input of the EPI. All indicator drivers are gated with

a lamp test signal generated by a switch on the Master Control Panel. This signal forces all indicators used to indicate errors and status to light.

The CON board provides all control signals used to control the data multiplexers in the EPI and the RISP, and also provides the display address code used by the EPI to compare with the address code contained in the sync word so as to accomplish data selection down to the display level. It also provides the adjustable blink clock, the various reset signals, and the freeze control signals. All controls and switches are located on the Master Control Panel with the CON board itself containing only decoding and timing circuits.

4.2.3.2 - Master Control Panel.- The Master Control Panel (MCP) contains all the controls, switches, and indicators used in the operation of both EPI's. It interfaces with the Control Section of each EPI. The control functions involved are as follows:

Display Selection - The MCP has controls to enable the operator to review data for any display recorded by the system. It uses interlocking push-button switches to select any port and display. It also uses controls to allow the operator to select the output of either recorder and, in the case of EPI-1, to bypass the recorders and receive data directly from the RIB.

Freeze Mode Control - The MCP contains the controls used to put each EPI into the freeze mode and to manually switch between stored frames in the two memories.

Master Resets - The MCP contains the manual reset controls needed to initialize each EPI and DCVG in the EPIC.

Words/Bank Selection - The MCP contains a thumbwheel switch which is used for selecting the words-per-bank (W/B) setting for the EPIC. Both EPI's in the EPIC use the same W/B setting.

Blink Clocks - The MCP contains controls for two blink clocks, one for each EPI. These clocks are independently variable from Ø.22 to 25 Hz. Using these controls, the blink clock used for one EPI can be selected for use with the other EPI, thus providing a common blink clock for both displays. Also the blink clock for each EPI can be disabled, and the blink data can either be deleted from the display (blanked) or forced to remain constantly visible on the display (unblanked) like non-blinking data.

Lamp Test - The MCP contains a switch which is used to test all error and status indicators to determine if any indicator has failed.

The MCP also contains indicators for the various error and status signals generated by each EPI. The indicators include:

Sync decode.

Idle time decode.

Sync error. This condition is stored in memory along with the data and is indicated via a second set of indicators when detected at the output of the EPI.

Input parity error(s). This condition is stored in memory along with the data and is indicated via a second set of indicators when detected at the output of the EPI.

Output parity error.

DCVG parity error.

Asynchronous refresh mode.

Memory overflows.

Freeze mode.

Master clock fail (C225N).

Tape clock fail.

Receiving data.

There is also a set of indicators used to show which memory in each EPI is being used to refresh the playback display, and an indicator for each EPI which blinks at the associated blink clock rate. When the blink clock is disabled, the blink clock indicator will be on when the blink data is unblanked and off when the blink data is blanked.

4.2.3.3 Display Control and Vector Generators. - For information on the DCVG, consult the FAA manual entitled: "Radar Display Subsystem (RDS) - Display Control and Vector Generators (DCVG) (Raytheon Corp.), Volume I-III". There are two DCVG's used in the EPIC, each driving one playback PVD. These DCVG's include an A1 card to drive the PVD's directly.

4.2.4 Plan View Display. - For information on the PVD, consult the FAA manual entitled: "Plan View Display Console and Plan View Display Monitor Console (Raytheon Corp.), Volume I-II". There are two PVD's used in the Playback Element.

4.2.5 Time Code Readers. - A total of four Time Code Readers are contained in the EM. One is used to display the CTS time which in an ARTCC is the system clock, two are used for searching for specific times on tape from the two recorders on playback, and one is a spare unit. These particular readers are Systron-Donner Model 8030 and they have the capability of reading a reproduced time code over varying tape speeds and in either direction.

4.3 Mechanical and Electrical Data. - The EPIC consists of an Optima vertical cabinet, Model number AR-702430. Figure 4-16 gives the dimensions of this cabinet while Figure 4-17 gives the outline dimensions of the units that are contained in the EPIC. Each EPI in the cabinet consists of a single card cage containing 16 printed circuit cards. All card cages are hinged on the left side and mounted at the front of the cabinet behind removable blank panels to facilitate easy maintenance. The controls and indicators are mounted on a separate 14 x 24 inch panel above the card cages. The two DCVG's used in the Playback Element are mounted behind the rear door of the EPIC.

Three DC power supplies are used in the EPIC--two 5-volt, 50-amp switching supplies (Powertec Model 9E5-50C-17), each used to supply power to an EPI/DCVG pair, and one 5-volt, 15-amp conventional supply (Power-One Model RD5-15/OVP), used to supply power to the MCP. These three power supplies are mounted on a roll-out shelf.

All units contained in the EPIC, with the exception of the DCVG's, are accessible from the front of the cabinet. Cables enter and leave the cabinet through connectors mounted on the top cover panel of the cabinet. Figure 4-18 shows the location of the various units within the EPIC.

Optima Vertical Cabinet

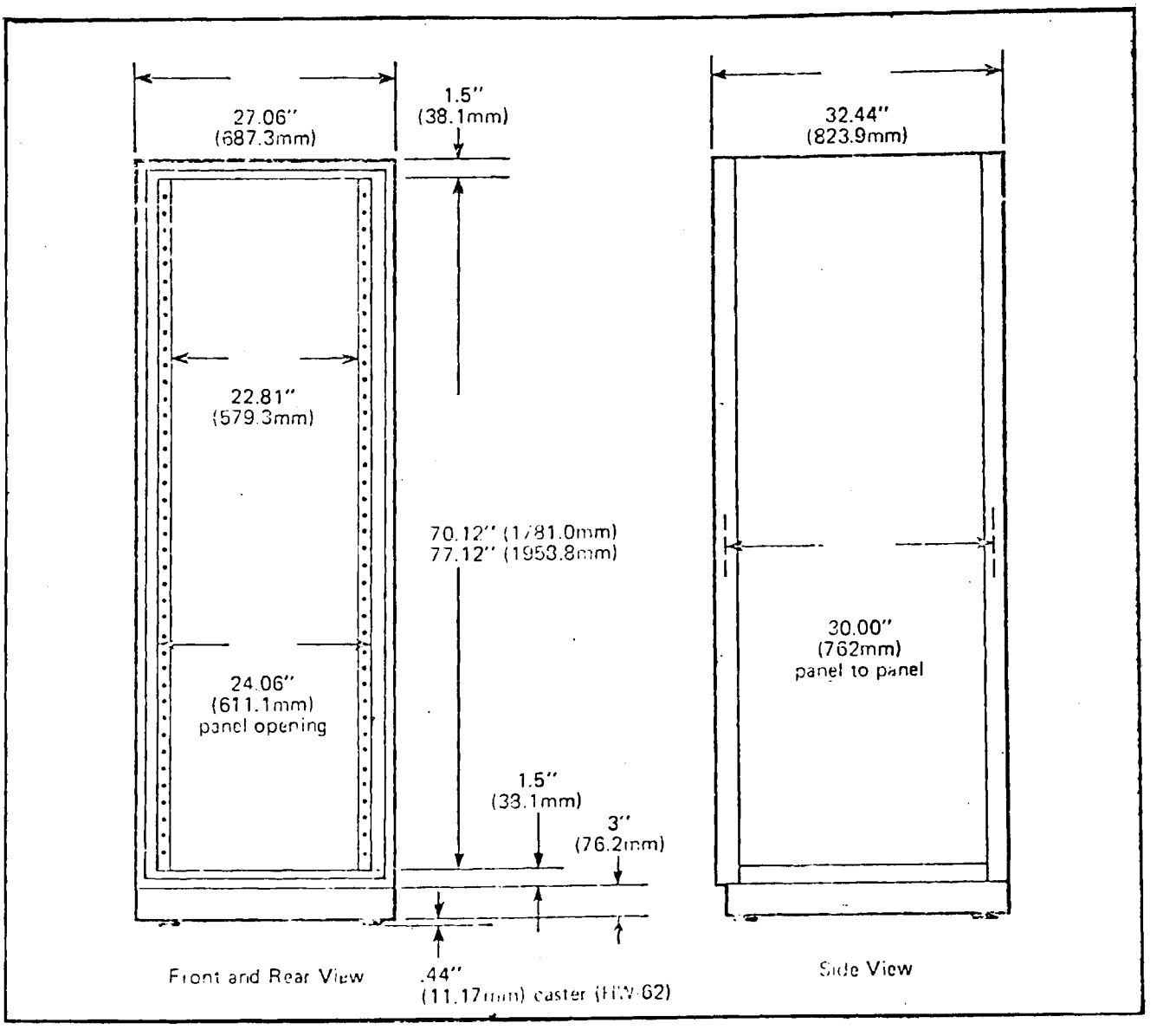
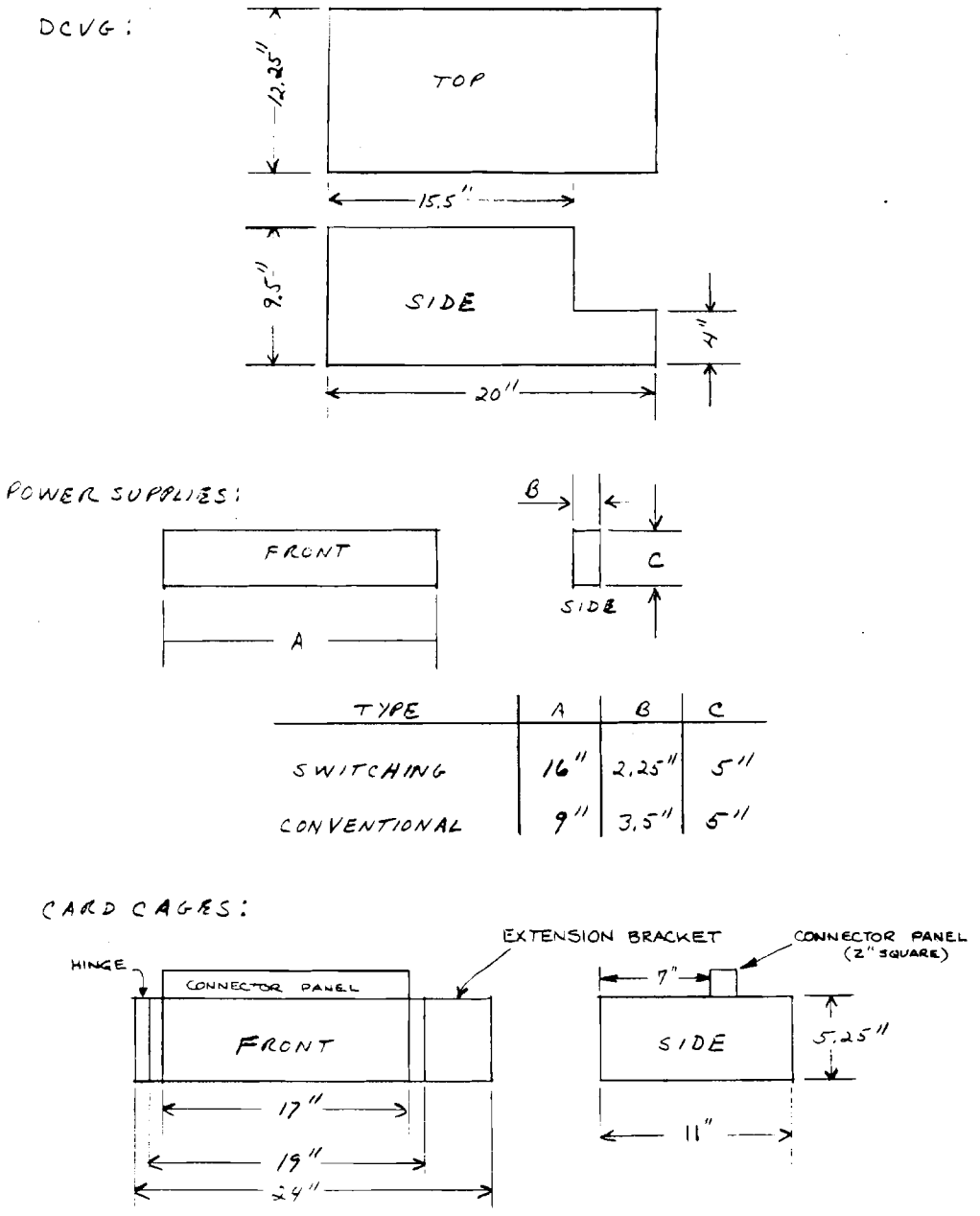
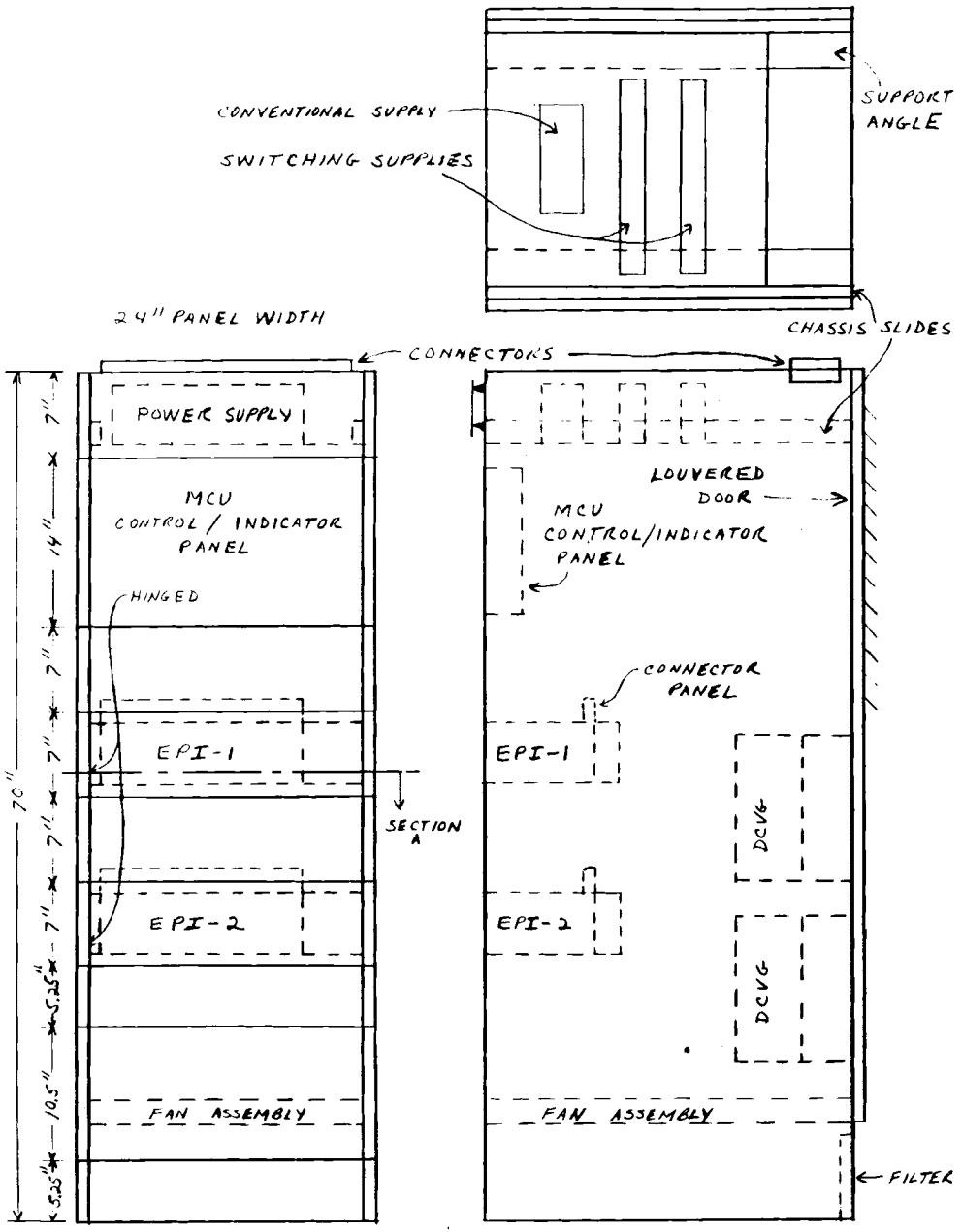


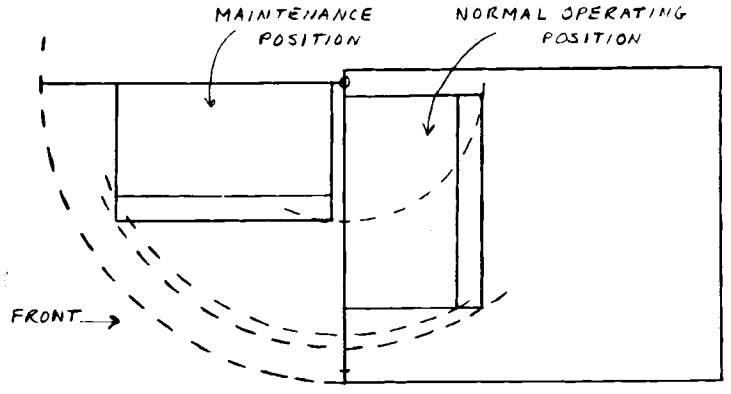
FIGURE 4-16. EPIC CABINET DIMENSION



TYPE	A	B	C
SWITCHING	16"	2.25"	5"
CONVENTIONAL	9"	3.5"	5"

FIGURE 4-17. OUTLINE DIMENSIONS OF UNITS IN THE EPIC





SECTION-A
TOP VIEW SHOWING TYPICAL CARD CAGE IN BOTH THE NORMAL OPERATING POSITION AND THE MAINTENANCE POSITION. CARD CAGES WILL BE 11" DEEP (APPROX.)

FIGURE 4-18. UNIT LOCATIONS WITHIN THE EPIC

APPENDIX A

BACKGROUND INFORMATION ON THE DGIO/DCVG INTERFACE

General. - The DGIO contains data reclocking logic, parity check logic, a DCVG address decoder, a blink clock generator, and the DCVG output multiplexers and drivers. Display data being transferred to all six DCVG's from either the Refresh Memory (RM) in the Computer Display Channel (CDC) system or the Display Element (DE) in the Display Channel Complex (DCC) system is intermixed on a common 16-line parallel bus within the DGIO. This bus terminates in six sets of gated drivers, one set for each DCVG. Address information is sent to the DGIO with each group of data designating which DCVG is to receive the data. The DGIO decodes this information and generates a Valid Address (VAD) signal for each DCVG which activates the proper driver and allows data to be gated to the DCVG that is being addressed.

The DCVG/PVD's are continually refreshed by the display computer refresh subsystem. The term "refresh subsystem" will be used when referring to details common to both display computer systems (CDC or DCC). Where details refer to a particular system it will be noted. Since the DARC system is not completely finalized, it will be assumed that the refresh function will closely follow that of the CDC and the DCC. Therefore, details peculiar to the DARC system will not be given at this time.

Refresh Rate. - The refresh subsystem refreshes the PVD at a maximum rate of 55 frames per second. This refresh rate allows the refresh subsystem approximately 18.2 msec (1 refresh cycle) to display a complete frame of data on the PVD. For the purposes of this document a refresh period will be defined as the time it takes to display a complete frame of data on a PVD. This period is of variable duration depending upon how the controller has configured his display and the amount of radar returns being processed by the system. If the refresh period for a particular frame of data is less than 18.2 msec, then the refresh subsystem is able to display the frame 55 times a second and the display is said to be in the synchronous mode. If the refresh period is longer than 18.2 msec, the refresh subsystem uses an extended refresh cycle to display the frame and the refresh rate drops below the nominal 55 frames per second. The exact refresh rate depends on the amount by which the refresh cycle is extended. In this situation the display is said to be in the asynchronous mode.

The actual frequency of the 55 Hz refresh rate clock is slightly greater than 55 Hz, and is different in both display computer systems. The CDC uses a 3.606380 MHz fixed crystal oscillator divided down to give a refresh rate of 55.029 Hz. The DCC uses a technique which enables the refresh rate to be varied from 11.3 Hz to 55.049 Hz by varying the period of the refresh clock in steps of 21.6 microseconds. This time period corresponds to the typical time between accesses of the memory by any particular DCVG in the DCC system. The refresh rate of 55.049 Hz is used in normal operation. The maximum number of data words that can be transferred to the DCVG before the display is put in the

asynchronous mode is given for each Words-per-Bank (W/B) setting (see Memory Access paragraph) as follows:

W/B	No. Words
1	1682
2	1682
3	1680
4	1680

Due to the fact that the DCVG processes the various types of words at different rates, the actual number of words received by a DCVG before its associated display becomes asynchronous may be less than these maximum figures. Figure A-1 illustrates the timing of both the synchronous and asynchronous modes.

Memory Access. - In the refresh subsystem the input/output interface to memory (either RM or DE) is time-shared between the processing computer and the displays in the display computer system. Each is given an opportunity to access memory according to a table called the access assignment table. This table allows a DCVG to obtain data from memory at a maximum rate of one word every 10.8 microseconds. During any single access, the DCVG is capable of receiving up to four 64-bit words. In the CDC system, the number of words transferred during any access (W/B setting) varies between one and four and is dependent upon quantity and configuration of RM modules in the system. In the DCC system the W/B setting is fixed at two so that two words are transferred each time an access is used. The table below shows the correspondence between the W/B setting and the time interval between assigned accesses:

W/B	Access Time (Microseconds)
1	10.8
2	21.6
3	32.4
4	43.2

If the DCVG is busy processing data from a previous access, it will skip all accesses assigned to it until the processing is complete, at which time it will use its next assigned access. When a DCVG is ready to access memory, it sets a flag called the "DCVG Request" which signals the refresh subsystem through the DGIO that it is ready to accept data. If this flag is not set when the refresh subsystem polls the DCVG it will give the access slot to the display processor to be used as an extra access for updating the refresh data base in the memory. If the flag is set, the refresh subsystem will give the access slot to the DCVG.

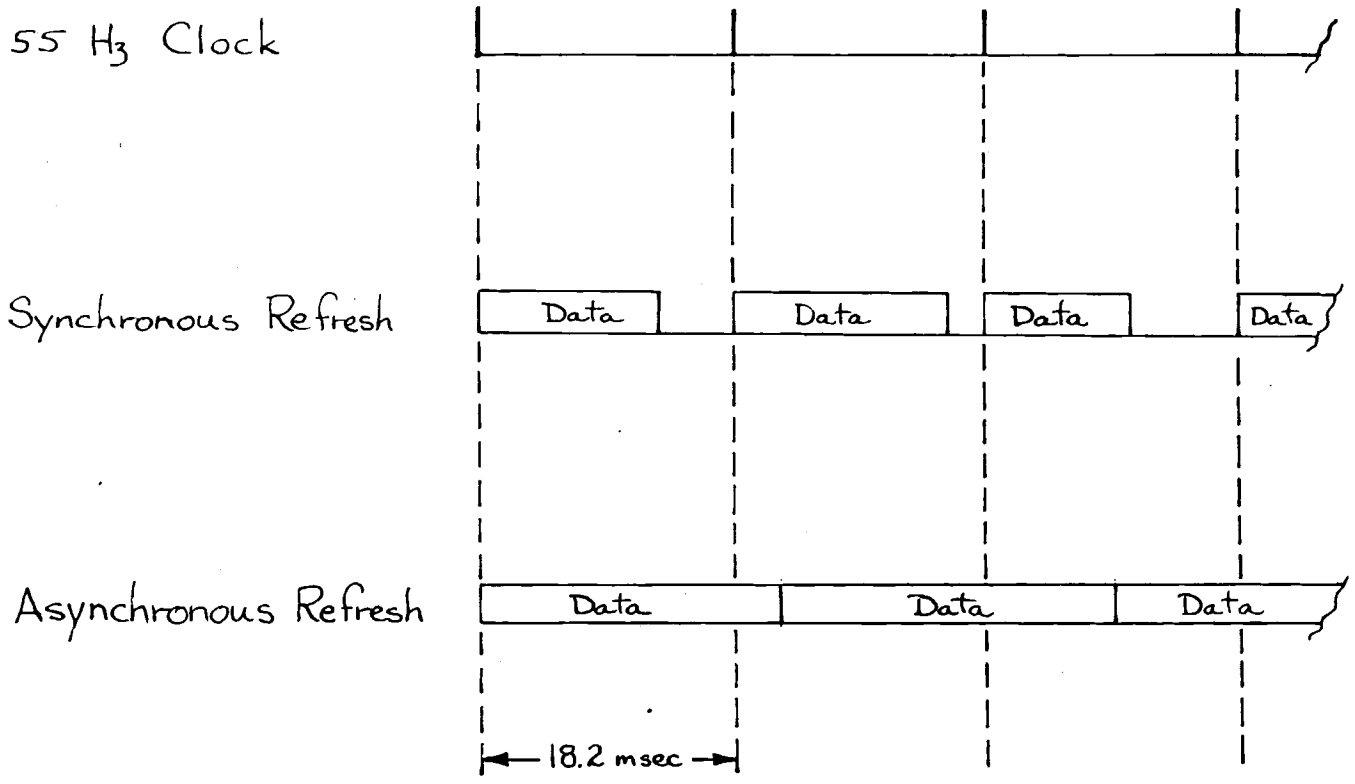


FIGURE A-1. REFRESH MODES

Display Data. - The refresh subsystem transfers 16 bits of parallel data (one byte) at a rate of 4.444 MHz. Since a complete DCVG word consists of 64 data bits, each word is made up of four 16-bit bytes. The DGIO received data for all 6 DCVG's intermixed on a single bus. The data are arranged sequentially in an order according to the access assignment table. In order to direct the data to the various displays, the refresh subsystem generates a display address code which is sent serially to the DGIO on a separate data line prior to the data. The DGIO decodes this address, enables a set of drivers which transmits the data to the appropriate DCVG, and signals the appropriate DCVG that data is available. The signal initiated by the DGIO is called the Valid Address (VAD) signal and is used by the DCVG to initiate the receiving of data. The VAD is generated during the first byte time of a transfer to the DCVG and there is a separate VAD for every DCVG within a DGU. Figure A-2 shows the timing relationship between the VAD, the data bytes, the 4.444 MHz clock, the display address, and the parity error signal (described in a later paragraph) used in the refresh subsystem.

The DCVG examines certain bits present in the 64-bit data words to determine whether or not a specific piece of data is to be blinked on the display. If the bits are set to a logic "one" the DCVG uses the blink clock which is generated in each DGU to blink the data it sends to the PVD. Therefore, information regarding the blinking of data is inherently sampled and recorded along with the data. The blink clock in each DGU is variable from 0.25 Hz to 12.5 Hz and is independent of other DGU's.

As data is transferred from memory to the DCVG, the refresh subsystem examines each 64-bit word to determine if odd parity exists. If the parity of a word is even, an error flag is set during the first byte time following the word as shown in Figure A-2. This error flag is detected by the DCVG which enables the PVD to display the error symbol (X).

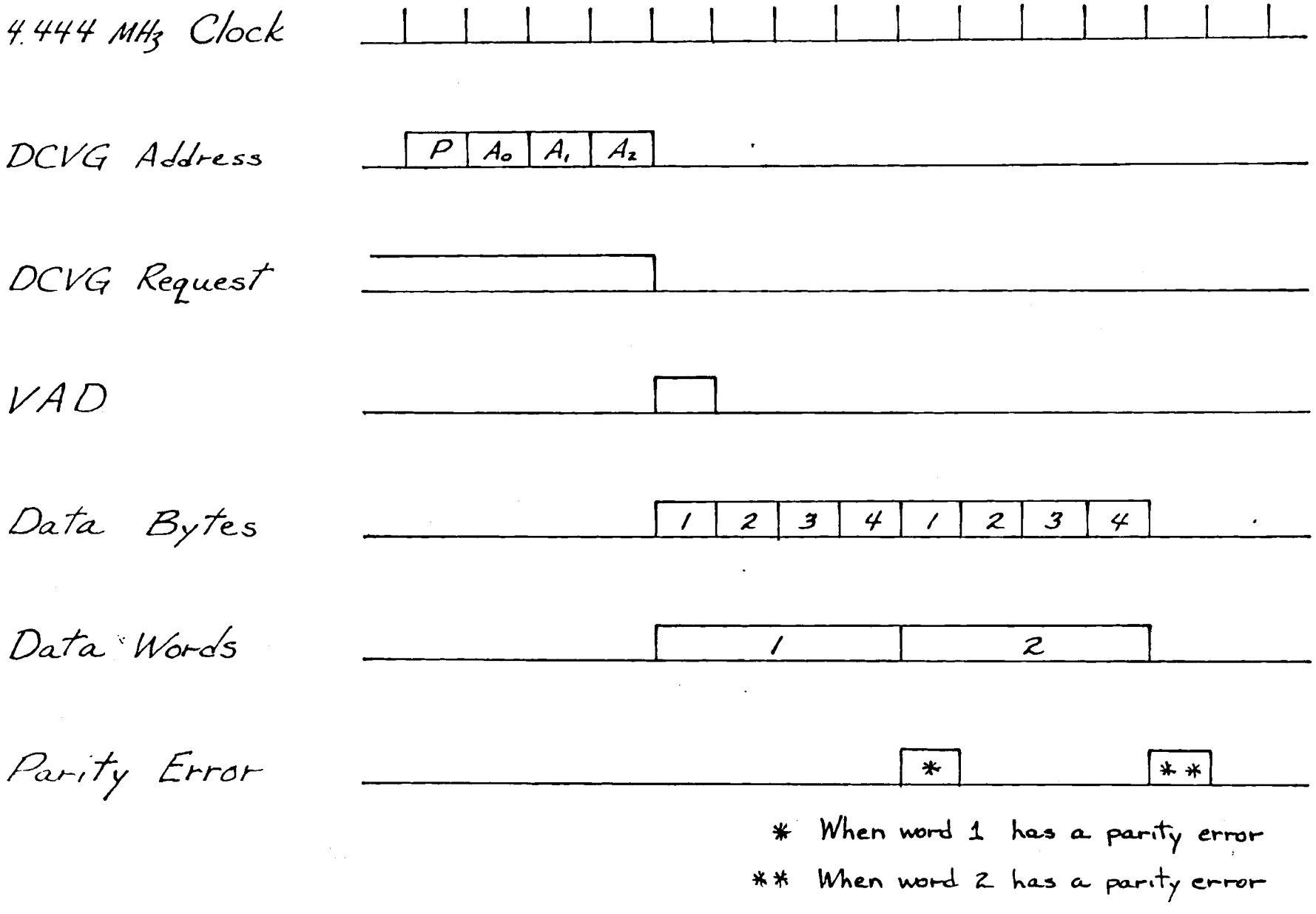


FIGURE A-2. INTERFACE TIMING — TWO WORDS PER BANK

APPENDIX B

DISPLAY GENERATOR UNIT MODIFICATION

This modification, which was requested under NAS Change Proposal 5351A, case file # ANA-170-CDC-001-A, dated March 28, 1979, was installed at the Technical Center in six DGU's in order to provide an interface between the DGU and the RIB. The purpose was to obtain data for recording from the bus feeding the six DCVG's within the DGU. The modification consists of the addition of a new board in the XA06 slot (which was previously unused) of the DGI/O assembly and backplane wiring changes consisting of the following:

1. The select line (DVG 6 DSELN) which enables the set of gated drivers used to send data (16 bits) to DCVG 6 was disconnected. This select line originates on the XAØ5 board and is used by the drivers on the XAØ1, XAØ2, and XAØ3 boards. The connection was broken at the source, leaving the inputs to the three boards XAØ1, XAØ2, and XAØ3 interconnected.

2. The select line inputs to the XAØ1, XAØ2, and XAØ3 boards were connected to a pin on the XAØ6 slot. With the XAØ6 board inserted, this pin is jumpered to ground, and the drivers on the XAØ1, XAØ2, and XAØ3 boards are continuously gated on.

3. The select line signal originating on the XAØ5 board was connected to a pin on the XAØ6 slot. With the XAØ6 board inserted, this signal controls a set of gated drivers located on the XAØ6 board. With the XAØ6-J jumper board inserted, this signal is jumpered to the pin which is connected to the select line inputs on the XAØ1, XAØ2, and the XAØ3 boards, thus restoring the connection between these boards and the XAØ5 board.

4. The outputs of the gated drivers on the XAØ1, XAØ2, and XAØ3 boards were disconnected from the connectors which are used to interface the DGI/O assembly with DCVG 6.

5. The outputs of these drivers were then connected to pins on the XAØ6 slot. These pins are connected to two sets of drivers on the XAØ6 board. One set consists of gated drivers used to interface with DCVG 6; the other set consists of differential drivers used to interface with the RIB.

6. The outputs of the DCVG interface drivers on the XAØ6 board were then connected to the connectors which are used to interface the DGI/O assembly with DCVG 6.

7. The non-gated signals sent to DCVG 6, which originate on XAØ3 (signal "DVG 6 4.4MN"), XAØ4 (signals "DVG 6 LSBN", "DVG 6 MSBN", and "DVG 6 RESN") and XAØ5 (signals "DVG 6 VADN" and "DVG 6 DPAR"), were disconnected from the connectors which are used to interface the DGI/O assembly with DCVG 6.

8. The outputs of these drivers were then connected to pins on the XAØ6 slot. These pins are connected to two sets of drivers on the XAØ6 board. One set consists of non-gated drivers used to interface with DCVG 6; the other consists of differential drivers used to interface with the RIB.

9. The outputs of the DCVG interface drivers on the XAØ6 board were then connected to the connectors which are used to interface the DGI/O assembly with DCVG 6.

10. The "VAD" signals used for DCVG's 1 through 5, which originate on the XAØ5 board, were connected to the inputs of the RIB interface drivers on the XAØ6 board.

11. The "Off-line" signals associated with DCVG's 1 through 6, which originate on the XA1Ø, XA12, XA14, XA16, XA18, and XA2Ø boards, were connected to the inputs of the RIB interface drivers on the XAØ6 board.

This modification accomplishes the following;

1. All signals necessary for recording data for the six DCVG's contained in the DGU are made available to differential drivers on the XAØ6 board. The outputs of these drivers are connected to two connectors located along the edge of the XAØ6 board opposite the edge which is inserted into thebackplane connector.

2. The original data path for DCVG 6 is broken and all signals sent to DCVG 6 are routed through the XAØ6 board. Thus this board becomes an integral part of the DGI/O-DCVG 6 interface. A jumper board is provided which will restore the original data path by jumpering all the pins used for the inputs to the DCVG interface drivers on the XAØ6 board with the pins used for the outputs of these drivers.

The XAØ6 board draws a maximum of 1.6 Amps from the power supply used for the DGI/O basket. This power supply is rated at 70 Amps. The DGI/O basket, without the XAØ6 board inserted, draws 53 Amps.

The following three sections contain the DGI/O backplane changes, revised DGI/O documentation, and the XAØ6 board documentation, which includes schematics, parts lists, parts location drawings, and printed circuit layout drawings and modifications. Also included are the printed circuit layout drawings for the XAØ6-J jumper board.

Section 1 - DGI/O Backplane Changes

ITEM	ACTION	SIGNAL NAME	WIRE NO.	FROM	TO	Z
1	del.	DVG 6 BTØØN	1	J21 1	XAØ1 22	2
2	del.	DVG 6 BTØ1N	1	J21 15	XAØ1 23	2
3	del.	DVG 6 BTØ2N	1	J21 3	XAØ1 63	2
4	del.	DVG 6 BTØ3N	1	J21 17	XAØ1 66	2
5	del.	DVG 6 BTØ4N	1	J21 5	XAØ1 97	2
6	del.	DVG 6 BTØ5N	1	J21 19	XAØ1 99	2
7	del.	DVG 6 BTØ6N	1	J21 7	XAØ2 22	2
8	del.	DVG 6 BTØ7N	1	J21 21	XAØ2 23	2
9	del.	DVG 6 BTØ8N	1	J21 9	XAØ2 63	2
10	del.	DVG 6 BTØ9N	1	J21 23	XAØ2 66	2
11	del.	DVG 6 BT1ØN	1	J21 11	XAØ2 97	2
12	del.	DVG 6 BT11N	1	J21 25	XAØ2 99	2
13	del.	DVG 6 BT12N	1	J2Ø 1	XAØ3 22	2
14	del.	DVG 6 BT13N	1	J2Ø 15	XAØ3 23	2
15	del.	DVG 6 BT14N	1	J2Ø 3	XAØ3 64	2
16	del.	DVG 6 BT15N	1	J2Ø 17	XAØ3 66	2
17	del.	DVG 6 DSELN	3	XAØ3 72	XAØ5 69	2
18	del.	DVG 6 LSBN	1	J2Ø 13	XAØ4 53	2
19	del.	DVG 6 MSBN	1	J2Ø 25	XAØ4 45	2
20	del.	DVG 6 RESN	1	J2Ø 23	XAØ4 61	2
21	del.	DVG 6 VADN	1	J2Ø 5	XAØ5 93	2
22	del.	DVG 6 DPAR	1	J2Ø 9	XAØ5 23	2
23	del.	DVG 6 4.4MN	1	J2Ø 21	XAØ3 99	2
24	add	DVG BTØØN	1	XAØ1 22	XAØ6 21	1
25	add	DVG BTØ1N	1	XAØ1 23	XAØ6 19	1

ITEM	ACTION	SIGNAL NAME	WIRE NO.	FROM	TO	Z
26	add	DVG BTO2N	1	XAØ1 63	XAØ6 17	1
27	add	DVG BTO3N	1	XAØ1 66	XAØ6 23	1
28	add	DVG BTO4N	1	XAØ1 97	XAØ6 29	1
29	add	DVG BTO5N	1	XAØ1 99	XAØ6 39	1
30	add	DVG BTO6N	1	XAØ2 22	XAØ6 45	1
31	add	DVG BTO7N	1	XAØ2 23	XAØ6 43	1
32	add	DVG BTO8N	1	XAØ2 63	XAØ6 41	1
33	add	DVG BTO9N	1	XAØ2 66	XAØ6 47	1
34	add	DVG BT10N	1	XAØ2 97	XAØ6 49	1
35	add	DVG BT11N	1	XAØ2 99	XAØ6 51	1
36	add	DVG BT12N	1	XAØ3 22	XAØ6 63	1
37	add	DVG BT13N	1	XAØ3 23	XAØ6 55	1
38	add	DVG BT14N	1	XAØ3 64	XAØ6 53	1
39	add	DVG BT15N	1	XAØ3 66	XAØ6 65	1
40	add	DVG 6 DSELN	1	XAØ5 69	XAØ6 75	1
41	add	DVG LSBN	1	XAØ4 53	XAØ6 73	1
42	add	DVG MSBN	1	XAØ4 45	XAØ6 71	1
43	add	DVG 6 OFFL	3	XA2Ø 39	XAØ6 66	2
44	add	DVG RESN	1	XAØ4 61	XAØ6 69	1
45	add	DVG 6 RVADN	1	XAØ5 93	XAØ6 15	1
46	add	DVG 4.4MN	1	XAØ3 99	XAØ6 67	1
47	add	DVG 1 OFFL	3	XA1Ø 39	XAØ6 56	2
48	add	DVG 2 OFFL	3	XA12 39	XAØ6 54	2
49	add	DVG 3 OFFL	3	XA14 39	XAØ6 58	2
50	add	DVG 4 OFFL	3	XA16 39	XAØ6 62	2
51	add	DVG 5 OFFL	3	XA18 39	XAØ6 64	2
52	add	DVG 1 VADN	2	XAØ5 96	XAØ6 3	3

ITEM	ACTION	SIGNAL TIME	WIRE NO.	FROM	TO	Z
53	add	DVG 2 VADN	2	XAØ5 98	XAØ6 7	3
54	add	DVG 3 VADN	2	XAØ5 95	XAØ6 9	3
55	add	DVG 4 VADN	2	XAØ5 97	XAØ6 11	3
56	add	DVG 5 VADN	2	XAØ5 91	XAØ6 13	3
57	add	DVG 6 BTØØN	1	XAØ6 10	J21 1	1
58	add	DVG 6 BTØ1N	1	XAØ6 2	J21 15	1
59	add	DVG 6 BTØ2N	1	XAØ6 8	J21 3	1
60	add	DVG 6 BTØ3N	1	XAØ6 12	J21 17	1
61	add	DVG 6 BTØ4N	1	XAØ6 16	J21 5	1
62	add	DVG 6 BTØ5N	1	XAØ6 14	J21 19	1
63	add	DVG 6 BTØ6N	1	XAØ6 24	J21 7	1
64	add	DVG 6 BTØ7N	1	XAØ6 18	J21 21	1
65	add	DVG 6 BTØ8N	1	XAØ6 20	J21 9	1
66	add	DVG 6 BTØ9N	1	XAØ6 22	J21 23	1
67	add	DVG 6 BT1ØN	1	XAØ6 26	J21 11	1
68	add	DVG 6 BT11N	1	XAØ6 30	J21 25	1
69	add	DVG 6 BT12N	1	XAØ6 88	J2Ø 1	1
70	add	DVG 6 BT13N	1	XAØ6 80	J2Ø 15	1
71	add	DVG 6 BT14N	1	XAØ6 82	J2Ø 3	1
72	add	DVG 6 BT15N	1	XAØ6 84	J2Ø 17	1
73	add	DVG 6 LSBN	1	XAØ6 50	J2Ø 13	1
74	add	DVG 6 MSBN	1	XAØ6 46	J2Ø 25	1
75	add	DVG 6 RESN	1	XAØ6 48	J2Ø 23	1
76	add	DVG 6 VADN	1	XAØ6 98	J2Ø 5	1
77	add	DVG 6 4.4MN	1	XAØ6 40	J2Ø 21	1
78	add	DVG CSELN	3	XAØ6 77	XAØ3 72	2
79	add	DVG DPAR	1	XAØ5 23	XAØ6 96	1
80	add	DVG 6 DPAR	1	XAØ6 94	J2Ø 9	1

Section 2 - Revised DGI/O Documentation

This section consists of updated wiring data lists and schematics which constitute that part of the NAS documentation on the DGI/O assembly which is changed by the incorporation of the modification. Copies of original wiring data lists with changes written in by hand are included along with an additional handwritten list. The schematic diagrams show changes in signal names only. This documentation will be formally updated when the modification is approved for permanent installation in the field.

WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE TYPE	CLASS
DVG1 BT11N	1	J06	25	XA02	82	2	M	PRI
DVG1 BT12N	1	XA03	2	J05	1	2	M	PRI
DVG1 BT13N	1	XA03	7	J05	15	2	M	PRI
DVG1 BT14N	1	XA03	32	J05	3	2	M	PRI
DVG1 BT15N	1	XA03	36	J05	17	2	M	PRI
DVG1 DPAR	1	XA05	19	J05	9	2	M	PRI
DVG1 DSELN	1	XA01	25	XA02	25	2	M	PRI
DVG1 DSELN	2	XA02	25	XA03	25	1	M	PRI
DVG1 DSELN	3	XA03	25	XA05	77	2	M	PRI
DVG1 ERRDR	1	XA06	47	J05	11	2	M	PRI
DVG1 LSBN	1	XA04	47	J05	13	2	M	PRI
DVG1 MSBN	1	XA04	39	J05	25	2	M	PRI
DVG1 OFFL	1	XA10	39	XA09	39	1	M	PRI
DVG1 OFFL	2	XA09	39	XA04	95	2	M	PRI
DVG1 OFFL	3	XA10	39	XA06	56	2		
DVG1 ONL	1	J27	25	XA06	43	1	M	PRI
DVG1 ONL	2	XA08	43	XA04	96	2	M	PRI
DVG1 RER	1	XA05	55	J05	19	2	M	PRI
DVG1 RESN	1	XA04	54	J05	23	2	M	PRI
DVG1 VADN	1	XA05	96	J05	5	2	M	PRI
DVG1 VADN	2	XA05	96	XA06	3	3		
DVG1 4.4MN	1	XA03	89	J05	21	2	M	PRI
DVG2 BLCLK	1	XA04	8	J08	7	2	M	PRI
DVG2 BT00N	1	J09	1	XA01	3	2	M	PRI
DVG2 BT01N	1	J09	15	XA01	8	2	M	PRI
DVG2 BT02N	1	J09	5	XA01	34	2	M	PRI
DVG2 BT03N	1	J09	17	XA01	38	2	M	PRI

	SIZE	CODE IDENT NO.	MD 851572
	A	49956	REV A SHEET 31
	SCALE NONE		

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WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE TYPE	CLASS
DVG2 BT04N	1	J09	5	XA01	79	2	M	PRI
DVG2 BT05N	1	J09	19	XA01	81	2	M	PRI
DVG2 BT06N	1	J09	7	XA02	3	2	M	PRI
DVG2 BT07N	1	J09	21	XA02	8	2	M	PRI
DVG2 BT08N	1	J09	9	XA02	34	2	M	PRI
DVG2 BT09N	1	J09	23	XA02	38	2	M	PRI
DVG2 BT10N	1	J09	11	XA02	79	2	M	PRI
DVG2 BT11N	1	J09	25	XA02	81	2	M	PRI
DVG2 BT12N	1	J08	1	XA03	3	2	M	PRI
DVG2 BT13N	1	J08	15	XA03	8	2	M	PRI
DVG2 BT14N	1	J08	3	XA03	34	2	M	PRI
DVG2 BT15N	1	J08	17	XA03	38	2	M	PRI
DVG2 DPAR	1	XA05	21	J08	9	2	M	PRI
DVG2 DSELM	1	XA03	26	XA05	79	2	M	PRI
DVG2 DSELN	2	XA02	26	XA03	26	1	M	PRI
DVG2 DSELM	3	XA01	26	XA02	26	2	M	PRI
DVG2 ERROR	1	XA08	45	J08	11	2	M	PRI
DVG2 LSBN	1	XA04	48	J08	13	2	M	PRI
DVG2 MSBN	1	XA04	40	J08	25	2	M	PRI
DVG2 OFFL	1	XA12	39	XA11	39	1	M	PRI
DVG2 OFFL	2	XA11	39	XA04	94	2	M	PRI
DVG2 OFFL	3	XA12	39	XA06	54	2		
DVG2 ONL	1	XA08	73	J27	24	2	M	PRI
DVG2 ONL	2	XA04	93	XA08	73	1	M	PRI
DVG2 REQ	1	XA05	57	J08	19	2	M	PRI
DVG2 RESN	1	XA04	56	J08	23	2	M	PRI

	SIZE	CODE IDENT NO.	WD 851572
	A	49956	REV A SHEET 32
	SCALE NONE		

WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE CLASS TYPE	
DVG2 VADN	1	XA05	98	J08	5	2	M	PRI
DVG2 VADN	2	XA05	98	XA06	7	23		
DVG2 4.4MN	1	J08	21	XA03	92	2	M	PRI
DVG3 BLCLK	1	J11	7	XA04	7	2	M	PRI
DVG3 BT00N	1	J12	1	XA01	9	2	M	PRI
DVG3 BT01N	1	J12	15	XA01	19	2	M	PRI
DVG3 BT02N	1	J12	3	XA01	40	2	M	PRI
DVG3 BT03N	1	J12	17	XA01	61	2	M	PRI
DVG3 BT04N	1	J12	5	XA01	84	2	M	PRI
DVG3 BT05N	1	J12	19	XA01	95	2	M	PRI
DVG3 BT06N	1	J12	7	XA02	9	2	M	PRI
DVG3 BT07N	1	J12	21	XA02	19	2	M	PRI
DVG3 BT08N	1	J12	9	XA02	40	2	M	PRI
DVG3 BT09N	1	J12	23	XA02	61	2	M	PRI
DVG3 BT10N	1	J12	11	XA02	84	2	M	PRI
DVG3 BT11N	1	J12	25	XA02	95	2	M	PRI
DVG3 BT12N	1	J11	1	XA03	9	2	M	PRI
DVG3 BT13N	1	J11	15	XA03	19	2	M	PRI
DVG3 BT14N	1	J11	3	XA03	39	2	M	PRI
DVG3 BT15N	1	J11	17	XA03	62	2	M	PRI
DVG3 DPAR	1	XA05	45	J11	9	2	M	PRI
DVG3 DSELN	1	XA01	29	XA02	29	2	M	PRI
DVG3 DSELN	2	XA02	29	XA03	29	1	M	PRI
DVG3 DSELN	3	XA03	29	XA05	73	2	M	PRI
DVG3 ERROR	1	XA08	55	J11	11	2	M	PRI

SIZE	CODE IDENT NO.	WD 851572
A	49956	REV A SHEET 33
SCALE NONE		

FORM NO. 48-0453

WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE TYPE	CLASS
DVG3 LSDN	1	J11	13	XA04	52	2	M	PRI
DVG3 MSDN	1	J11	25	XA04	43	2	M	PRI
DVG3 OFFL	1	XA14	39	XA13	39	1	M	PRI
DVG3 OFFL	2	XA13	39	XA04	72	2	M	PRI
DVG3 OFFL	3	XA14	39	XAØ6	58	2		
DVG3 ONL	1	J27	13	XA08	41	1	M	PRI
DVG3 ONL	2	XA08	41	XA04	73	2	M	PRI
DVG3 REQ	1	XA05	92	J11	19	2	M	PRI
DVG3 RESN	1	J11	23	XA04	63	2	M	PRI
DVG3 VADN	1	XA05	95	J11	5	2	M	PRI
DVG3 VADN	2	XAØ5	95	XAØ6	9	3		
DVG3 4.6MN	1	J11	21	XA03	93	2	M	PRI
DVG4 BLCLK	1	J14	7	XA04	9	2	M	PRI
DVG4 BT00N	1	J15	1	XA01	10	2	M	PRI
DVG4 BT01N	1	J15	15	XA01	20	2	M	PRI
DVG4 BT02N	1	J15	3	XA01	42	2	M	PRI
DVG4 BT03N	1	J15	17	XA01	62	2	M	PRI
DVG4 BT04N	1	J15	5	XA01	83	2	M	PRI
DVG4 BT05N	1	J15	19	XA01	96	2	M	PRI
DVG4 BT06N	1	J15	7	XA02	10	2	M	PRI
DVG4 BT07N	1	J15	21	XA02	20	2	M	PRI
DVG4 BT08N	1	J15	9	XA02	42	2	M	PRI
DVG4 BT09N	1	J15	23	XA02	62	2	M	PRI
DVG4 BT10N	1	J15	11	XA02	83	2	M	PRI
DVG4 BT11N	1	J15	25	XA02	96	2	M	PRI
DVG4 BT12N	1	J14	1	XA03	10	2	M	PRI

SIZE	CODE IDENT NO.	WD 851572
A	49956	REV A SHEET 34
SCALE NONE		

FORM NO. 45-0453

WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE TYPE	CLASS
DVG4 BT13N	1	J14	15	XA03	20	2	M	PRI
DVG4 BT14N	1	J14	3	XA03	40	2	M	PRI
DVG4 BT15N	1	J14	17	XA03	58	2	M	PRI
DVG4 DPAR	1	J14	9	XA05	17	2	M	PRI
DVG4 DSELN	1	XA01	72	XA02	72	2	M	PRI
DVG4 DSELN	2	XA02	72	XA03	70	1	M	PRI
DVG4 DSELN	3	XA03	70	XA05	75	2	M	PRI
DVG4 ERROR	1	XA08	37	J14	11	2	M	PRI
DVG4 LSBN	1	J14	13	XA04	49	2	M	PRI
DVG4 MSBN	1	J14	25	XA04	44	2	M	PRI
DVG4 OFFL	1	XA16	39	XA15	39	1	M	PRI
DVG4 OFFL	2	XA15	39	XA04	77	2	M	PRI
DVG4 OFFL	3	XA16	39	XAØ6	62	2		
DVG4 ONL	1	J27	26	XA08	16	1	M	PRI
DVG4 ONL	2	XA08	16	XA04	75	2	M	PRI
DVG4 REQ	1	J14	19	XA05	67	2	M	PRI
DVG4 RESN	1	J14	23	XA04	64	2	M	PRI
DVG4 VADN	1	J14	5	XA05	97	2	M	PRI
DVG4 VADN	2	XAØ5	97	XAØ6	11	3		
DVG4 4.4MN	1	J14	21	XA03	94	2	M	PRI
DVG5 BLCLK	1	J17	7	XA04	13	2	M	PRI
DVG5 BT00N	1	J18	1	XA01	21	2	M	PRI
DVG5 BT01N	1	J18	15	XA01	24	2	M	PRI
DVG5 BT02N	1	J18	3	XA01	64	2	M	PRI
DVG5 BT03N	1	J18	17	XA01	65	2	M	PRI
DVG5 BT04N	1	J18	5	XA01	98	2	M	PRI
DVG5 BT05N	1	J18	19	XA01	100	2	M	PRI

SIZE	CODE IDENT NO.	MD 851572
A	49956	REV A SHEET 35
SCALE NONE		

WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE TYPE	CLASS
DVG5 BT06N	1	J18	7	XA02	21	2	M	PRI
DVG5 BT07N	1	J18	21	XA02	24	2	M	PRI
DVG5 BT08N	1	J18	9	XA02	64	2	M	PRI
DVG5 BT09N	1	J18	23	XA02	65	2	M	PRI
DVG5 BT10N	1	J18	11	XA02	98	2	M	PRI
DVG5 BT11N	1	J18	25	XA02	100	2	M	PRI
DVG5 BT12N	1	J17	1	XA03	21	2	M	PRI
DVG5 BT13N	1	J17	15	XA03	24	2	M	PRI
DVG5 BT14N	1	J17	3	XA03	61	2	M	PRI
DVG5 BT15N	1	J17	17	XA03	63	2	M	PRI
DVG5 DPAR	1	J17	9	XA05	25	2	M	PRI
DVG5 DSELN	1	XA02	70	XA01	70	2	M	PRI
DVG5 DSELN	2	XA03	71	XA02	70	1	M	PRI
DVG5 DSELN	3	XA05	71	XA03	71	2	M	PRI
DVG5 ERROR	1	XA08	51	J17	11	2	M	PRI
DVG5 LEBN	1	J17	13	XA04	51	2	M	PRI
DVG5 MEBN	1	J17	25	XA04	46	2	M	PRI
DVG5 OFFL	1	XA18	39	XA17	39	1	M	PRI
DVG5 OFFL	2	XA17	39	XA04	84	2	M	PRI
DVG5 OFFL	3	XA18	39	XA06	64	2		
DVG5 ONL	1	J27	1	XA08	27	1	M	PRI
DVG5 ONL	2	XA08	27	XA04	83	2	M	PRI
DVG5 REQ	1	J17	19	XA05	65	2	M	PRI
DVG5 RESN	1	J17	23	XA04	62	2	M	PRI
DVG5 VADN	1	J17	5	XA05	91	2	M	PRI
DVG5 VADN	2	XA05	91	XA06	13	3		
DVG5 4.4MN	1	J17	21	XA03	98	2	M	PRI

SIZE	CODE IDENT NO.	MD 851572
A	49956	REV A SHEET 36
SCALE NONE		

WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE TYPE	CLASS
DVG6 BLCLK	1	J20	7	XA04	11	2	M	PRI
DVG6 BT00N	1	J21	1	~~XA01~~ XA06	~~22~~ 10	~~2~~ 1	M	PRI
DVG6 BT01N	1	J21	15	~~XA01~~ XA06	~~23~~ 2	~~2~~ 1	M	PRI
DVG6 BT02N	1	J21	3	~~XA01~~ XA06	~~65~~ 8	~~2~~ 1	M	PRI
DVG6 BT03N	1	J21	17	~~XA01~~ XA06	~~66~~ 12	~~2~~ 1	M	PRI
DVG6 BT04N	1	J21	5	~~XA01~~ XA06	~~67~~ 16	~~2~~ 1	M	PRI
DVG6 BT05N	1	J21	19	~~XA01~~ XA06	~~68~~ 14	~~2~~ 1	M	PRI
DVG6 BT06N	1	J21	7	~~XA02~~ XA06	~~22~~ 24	~~2~~ 1	M	PRI
DVG6 BT07N	1	J21	21	~~XA02~~ XA06	~~23~~ 18	~~2~~ 1	M	PRI
DVG6 BT08N	1	J21	9	~~XA02~~ XA06	~~65~~ 20	~~2~~ 1	M	PRI
DVG6 BT09N	1	J21	23	~~XA02~~ XA06	~~66~~ 22	~~2~~ 1	M	PRI
DVG6 BT10N	1	J21	11	~~XA02~~ XA06	~~67~~ 26	~~2~~ 1	M	PRI
DVG6 BT11N	1	J21	25	~~XA02~~ XA06	~~68~~ 30	~~2~~ 1	M	PRI
DVG6 BT12N	1	J20	1	~~XA03~~ XA06	~~22~~ 88	~~2~~ 1	M	PRI
DVG6 BT13N	1	J20	15	~~XA03~~ XA06	~~23~~ 80	~~2~~ 1	M	PRI
DVG6 BT14N	1	J20	3	~~XA03~~ XA06	~~66~~ 82	~~2~~ 1	M	PRI
DVG6 BT15N	1	J20	17	~~XA03~~ XA06	~~66~~ 84	~~2~~ 1	M	PRI
DVG6 DPAR	1	J20	9	~~XA05~~ XA06	~~23~~ 94	~~2~~ 1	M	PRI
DVG6 ~~DSELN~~ CSELN	1	XA01	68	XA02	68	2	M	PRI
DVG6 ~~DSELN~~ CSELN	2	XA02	68	XA03	72	1	M	PRI
DVG6 ~~DSELN~~ CSELN	3	XA03	72	~~XA05~~ XA06	~~69~~ 77	~~2~~ 2	M	PRI
DVG6 ERROR	1	XA08	33	J20	11	2	M	PRI
DVG6 LSBN	1	J20	13	~~XA04~~ XA06	~~53~~ 50	~~2~~ 1	M	PRI
DVG6 MSBN	1	J20	25	~~XA04~~ XA06	~~45~~ 46	~~2~~ 1	M	PRI

SIZE	CODE IDENT NO.	WD 85:572
A	69956	REV A SHEET 37
SCALE NONE		

WIRING DATA

SIGNAL NAME	WIRE NO.	FROM PIN DESIGNATION		TO PIN DESIGNATION		Z	WIRE TYPE	CLASS
DVG6 OFFL	1	XA20	39	XA19	39	1	M	PRI
DVG6 OFFL	2	XA19	39	XA04	90	2	M	PRI
DVG6 OFFL	3	XA20	39	XA06	66	2		
DVG6 ONL	1	J27	3	XA08	25	1	M	PRI
DVG6 ONL	2	XA08	25	XA04	67	2	M	PRI
DVG6 REQ	1	J20	19	XA05	67	2	M	PRI
DVG6 REQN	1	J20	23	XA06 ~~XA04~~	98 ~~61~~	1 ~~2~~	M	PRI
DVG6 VADN	1	J20	5	XA06 ~~XA05~~	98 ~~93~~	1 ~~2~~	M	PRI
DVG6 4.4MN	1	J20	21	XA06 ~~XA03~~	90 ~~99~~	1 ~~2~~	M	PRI
DW Y 2 0+	1	J55	19	XA20	74	1	M	PRI
DW Y 2 0-	1	J55	18	XA20	73	2	M	PRI
DW Y 2 1+	1	J55	17	XA20	81	2	M	PRI
DW Y 2 1-	1	J55	16	XA20	75	2	M	PRI
DW Y 2 2+	1	J55	15	XA20	43	2	M	PRI
DW Y 2 2-	1	J55	14	XA20	45	1	M	PRI
DW Y 2 3+	1	J55	13	XA20	6	2	M	PRI
DW Y 2 3-	1	J55	26	XA20	12	1	M	PRI
DW Y 2 4+	1	J55	11	XA20	17	2	M	PRI
DW Y 2 4-	1	J55	12	XA20	18	1	M	PRI
DW Y 2 5+	1	J55	9	XA20	10	2	M	PRI
DW Y 2 5-	1	J55	10	XA20	15	1	M	PRI
DW Y 2 6+	1	J55	7	XA20	79	2	M	PRI
DW Y 2 6-	1	J55	8	XA20	84	1	M	PRI
DW Y 2 7+	1	J55	5	XA20	41	2	M	PRI
DW Y 2 7-	1	J55	6	XA20	47	1	M	PRI

SIZE	CODE IDENT NO.	MD 851572
A	49956	REV A SHEET 38
SCALE NONE		

FORM NO. 48-0433

SIGNAL NAME	WIRE NO.	FROM		TO		≡
DVG ETØ0N	1	XAØ1	21	XAØ6	21	1
DVG ETØ1N	1	XAØ1	23	XAØ6	19	1
DVG ETØ2N	1	XAØ1	63	XAØ6	17	1
DVG ETØ3N	1	XAØ1	66	XAØ6	23	1
DVG ETØ4N	1	XAØ1	97	XAØ6	29	1
DVG ETØ5N	1	XAØ1	99	XAØ6	39	1
DVG ETØ6N	1	XAØ2	22	XAØ6	45	1
DVG ETØ7N	1	XAØ2	23	XAØ6	43	1
DVG ETØ8N	1	XAØ2	63	XAØ6	41	1
DVG ETØ9N	1	XAØ2	66	XAØ6	47	1
DVG ET1ØN	1	XAØ2	97	XAØ6	49	1
DVG ET11N	1	XAØ2	99	XAØ6	51	1
DVG ET12N	1	XAØ3	22	XAØ6	63	1
DVG ET13N	1	XAØ3	23	XAØ6	55	1
DVG ET14N	1	XAØ3	64	XAØ6	53	1
DVG ET15N	1	XAØ3	66	XAØ6	65	1
DVG 6 DSELN	1	XAØ5	69	XAØ6	75	1
DVG LSBN	1	XAØ4	53	XAØ6	73	1
DVG MSBN	1	XAØ4	45	XAØ6	71	1
DVG RESN	1	XAØ4	61	XAØ6	69	1
DVG 6 RVADN	1	XAØ5	93	XAØ6	15	1
DVG 4.4MN	1	XAØ3	99	XAØ6	67	1
DVG DPAR	1	XAØ5	23	XAØ6	96	1

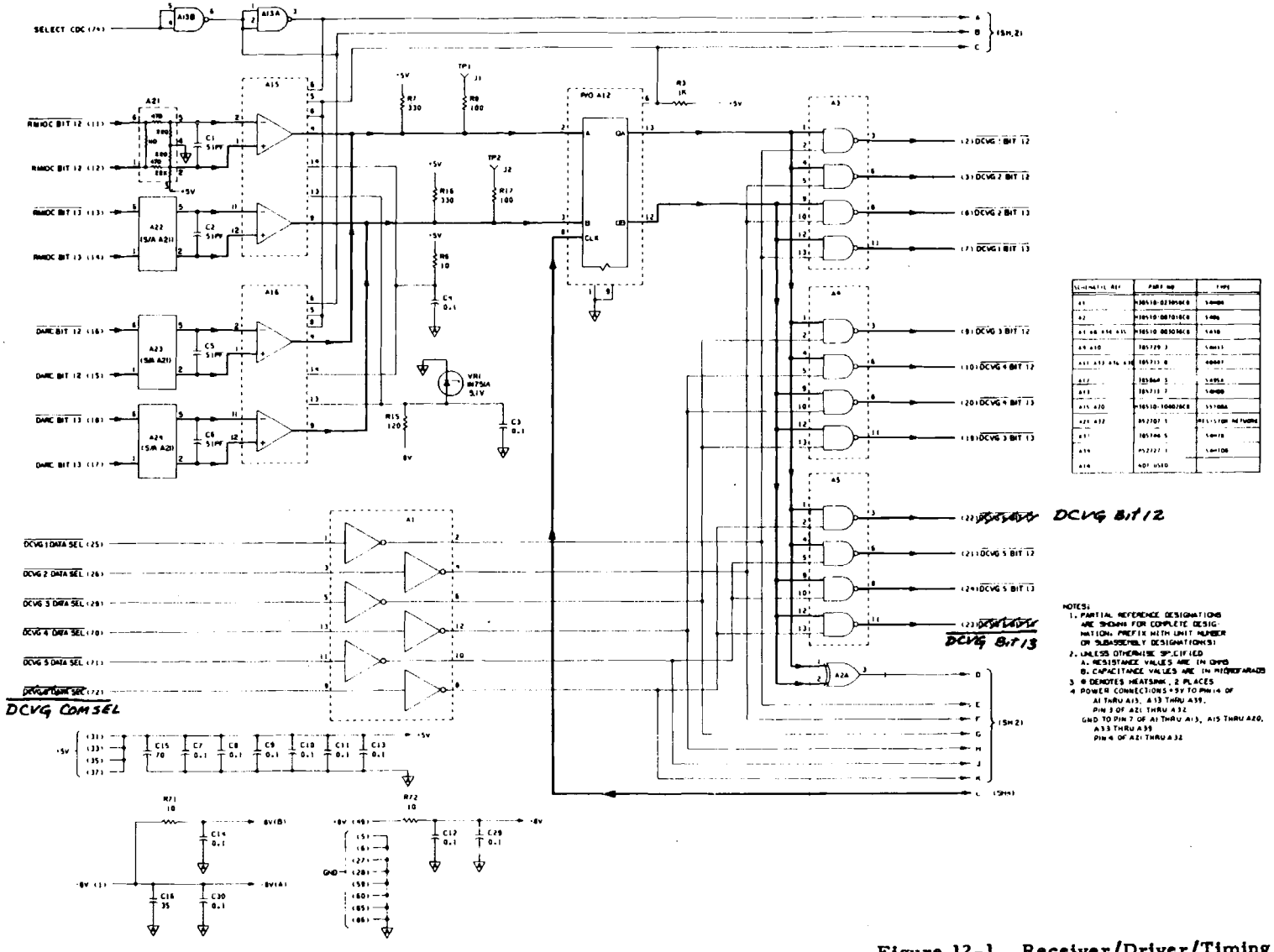


Figure 12-1. Receiver/Driver/Timing PCB N1A8A3, N2A8A3 (EL578900-1B) Schematic Diagram (Sheet 1 of 4)

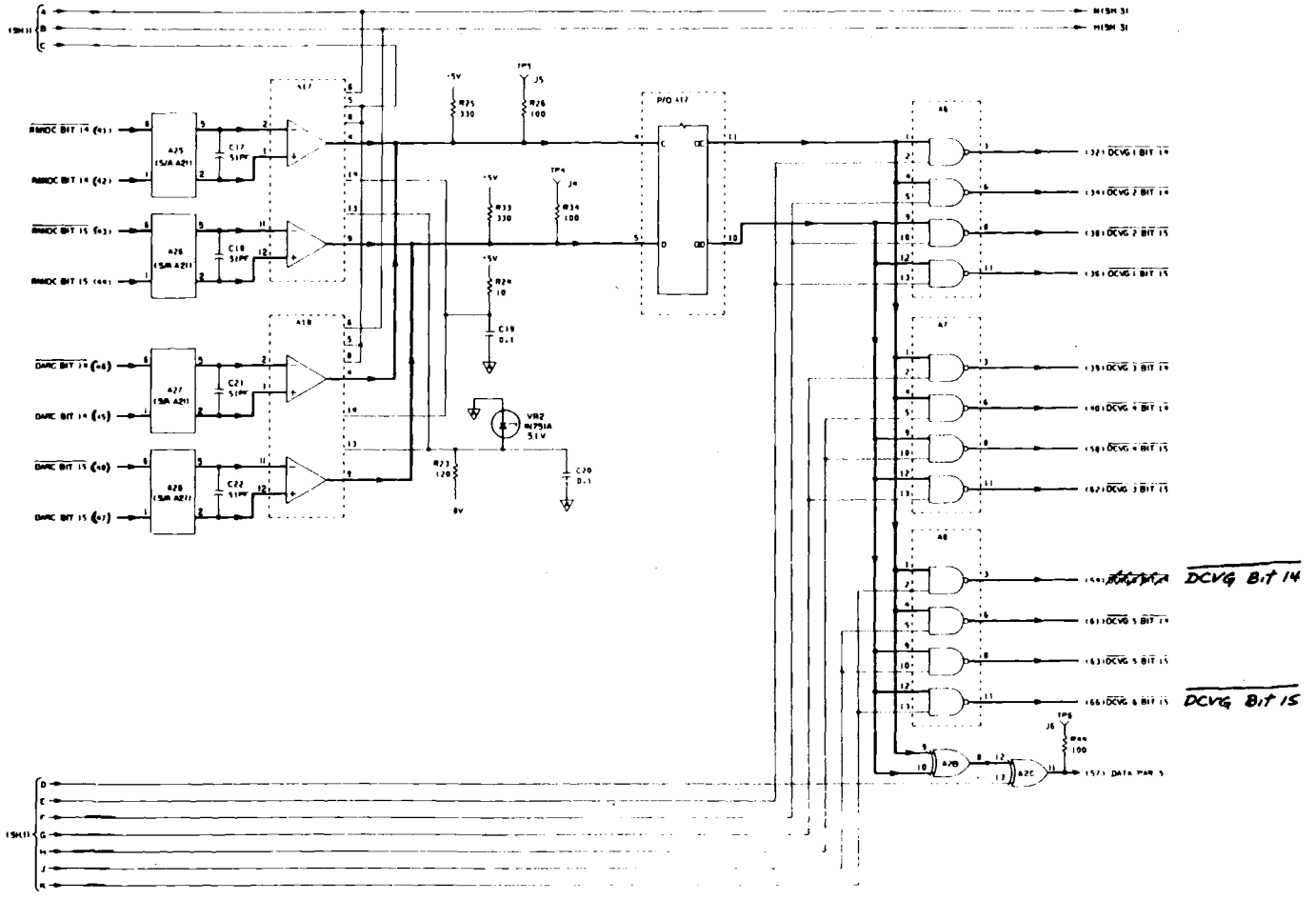


Figure 12-1. Receiver/Driver/Timing PCB N1A8A3, N2A8A3 (EL578900-1B) Schematic Diagram (Sheet 2 of 4)

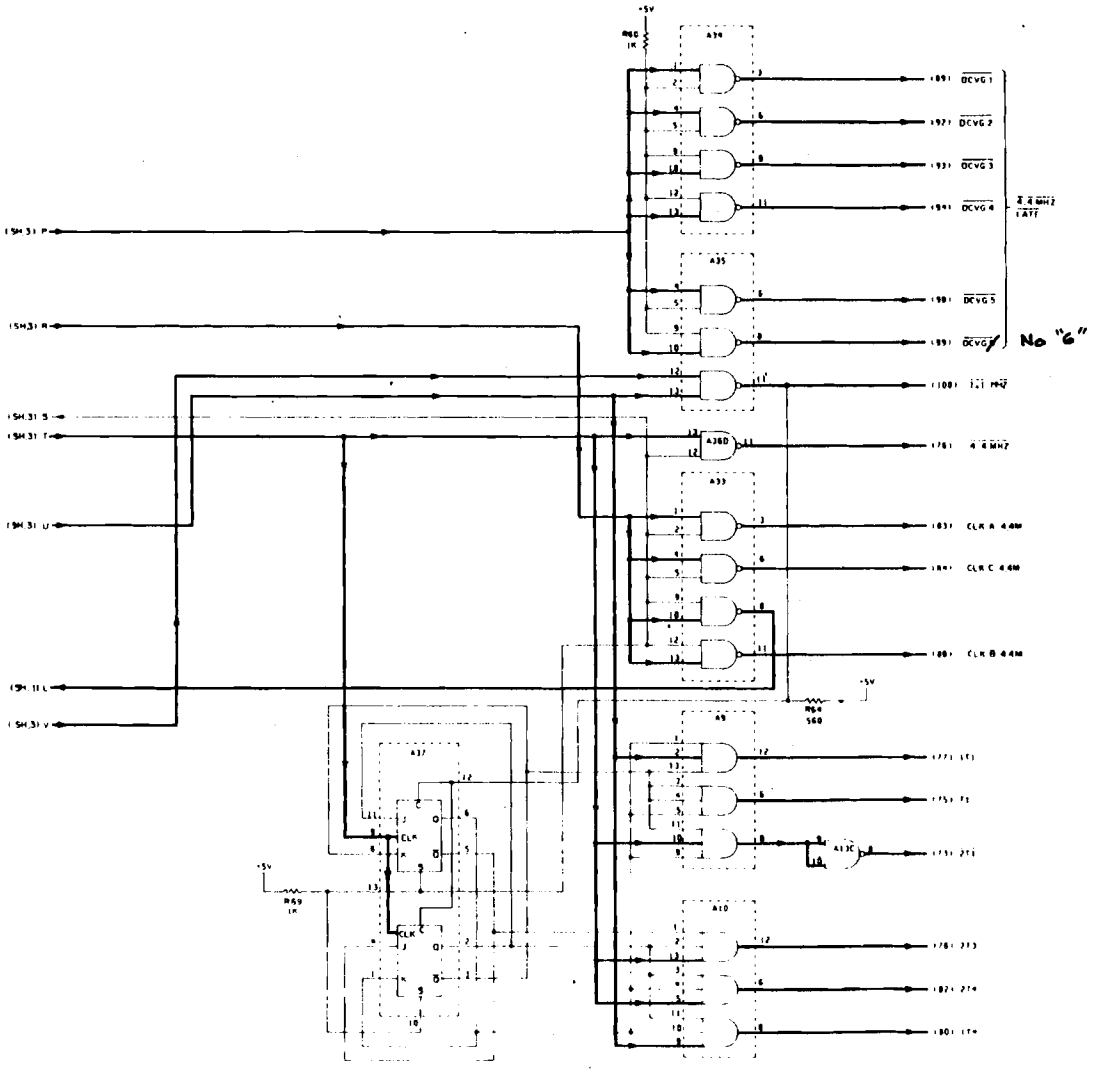


Figure 12-1. Receiver/Driver/Timing PCB N1A8A3, N2A8A3 (EL578900-1B) Schematic Diagram (Sheet 4 of 4)

12-6/12-6A

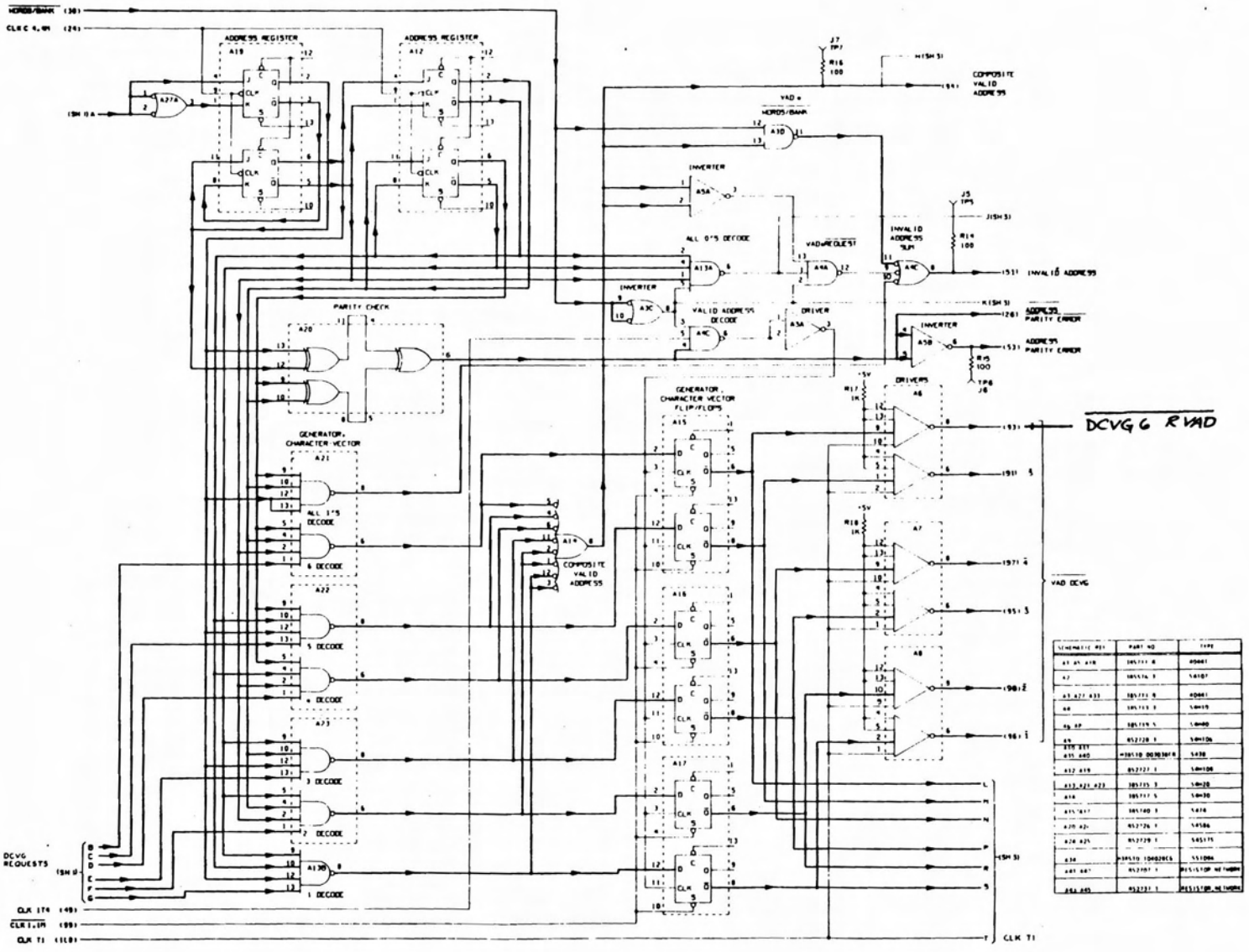


Figure 12-3. Address Request Generator PCB N1A8A5 N2A8A5 (EL578902-1B) Schematic Diagram (Sheet 2 of 3)

12-11/12-12

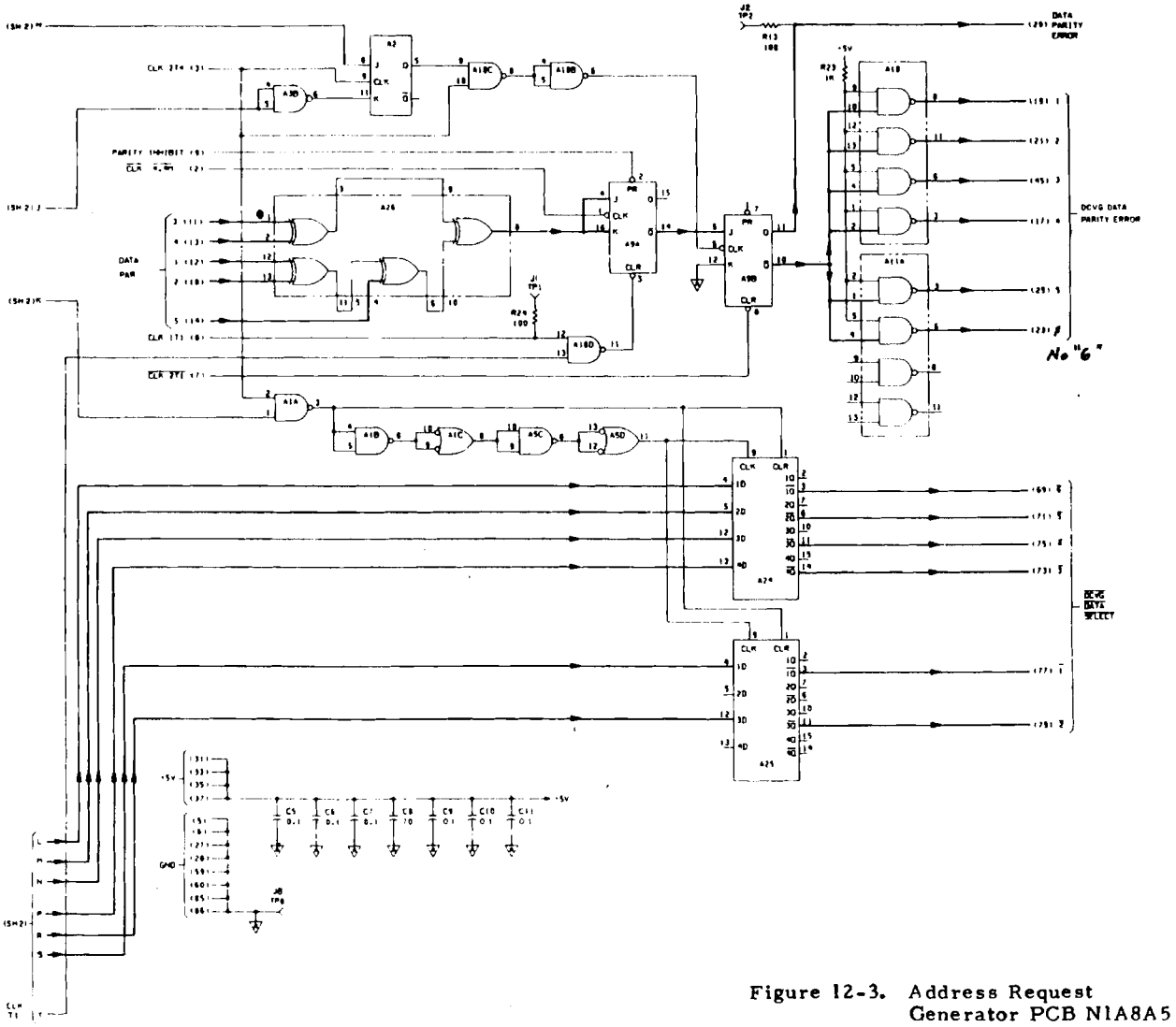


Figure 12-3. Address Request Generator PCB N1A8A5 N2A8A5 (EL578902-1B) Schematic Diagram (Sheet 3 of 3)

12-13/12-14

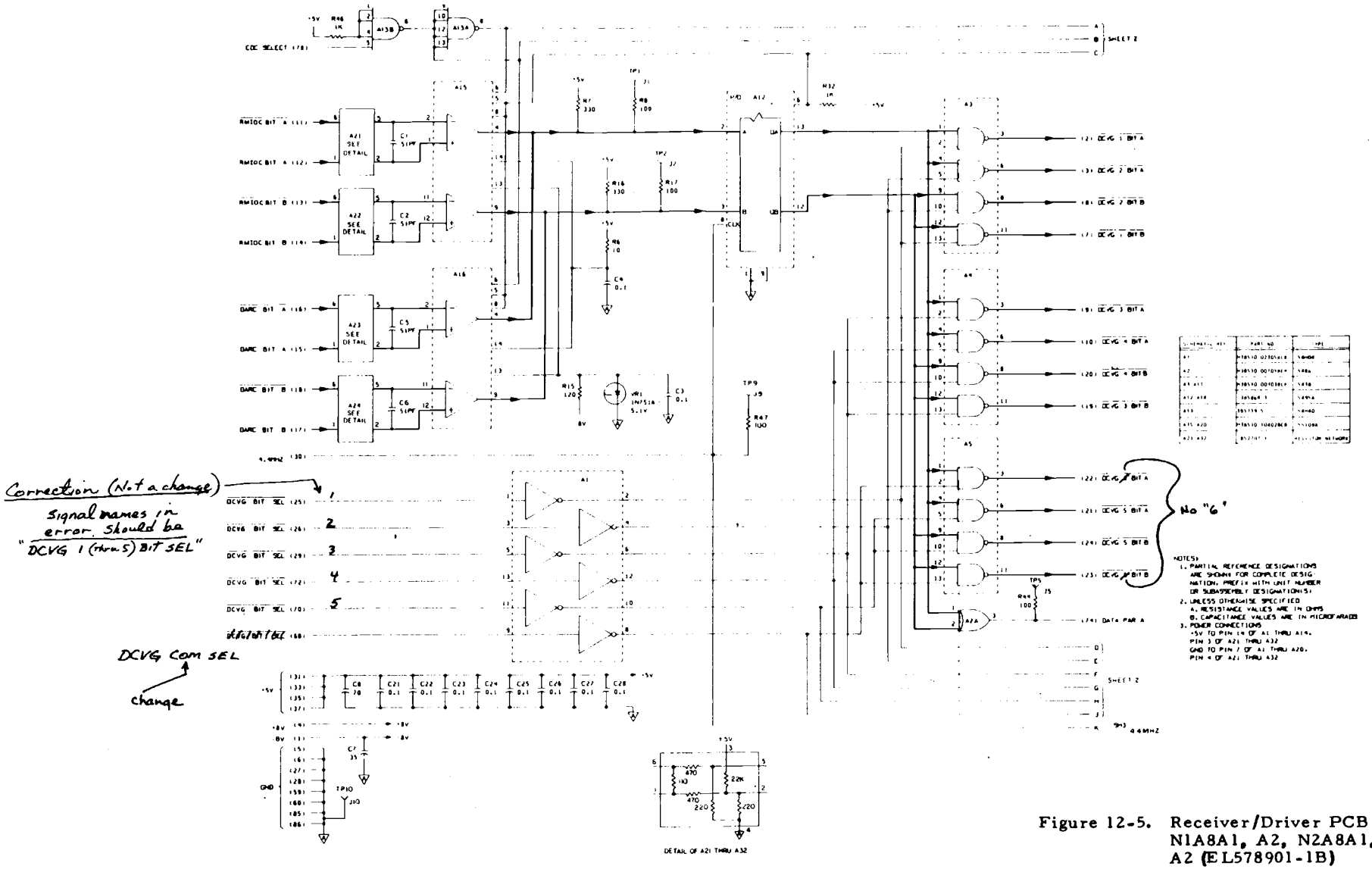


Figure 12-5. Receiver/Driver PCB N1A8A1, A2, N2A8A1, A2 (EL578901-1B) Schematic Diagram (Sheet 1 of 3)

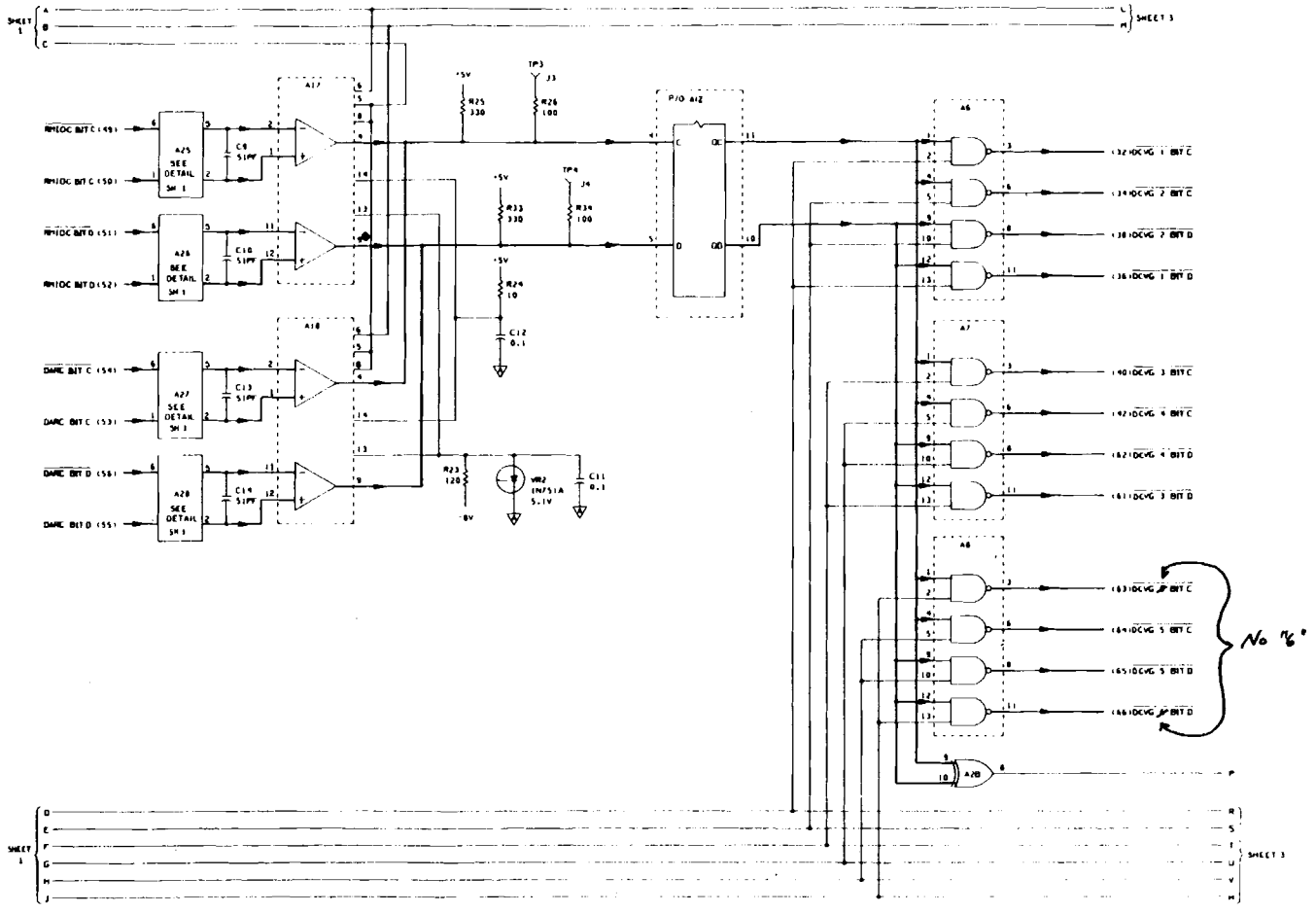


Figure 12-5. Receiver/Driver PCB N1A8A1, A2, N2A8A1, A2 (EL578901-1B) Schematic Diagram (Sheet 2 of 3)

12-19/12-19A

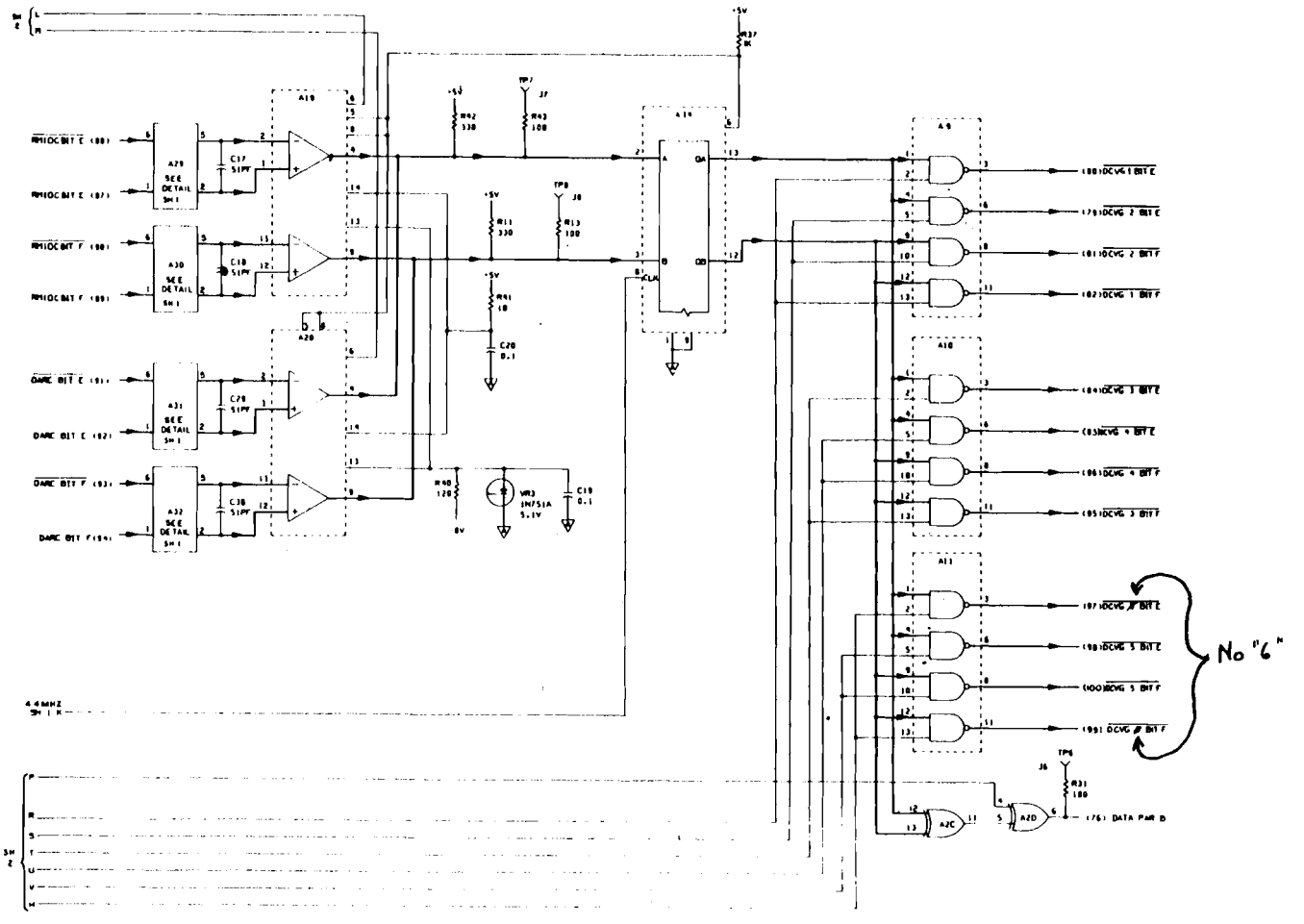


Figure 12-5. Receiver/Driver PCB N1A8A1, A2, N2A8A1, A2 (EL578901-1B) Schematic Diagram (Sheet 3 of 3)

12-20/12-20A

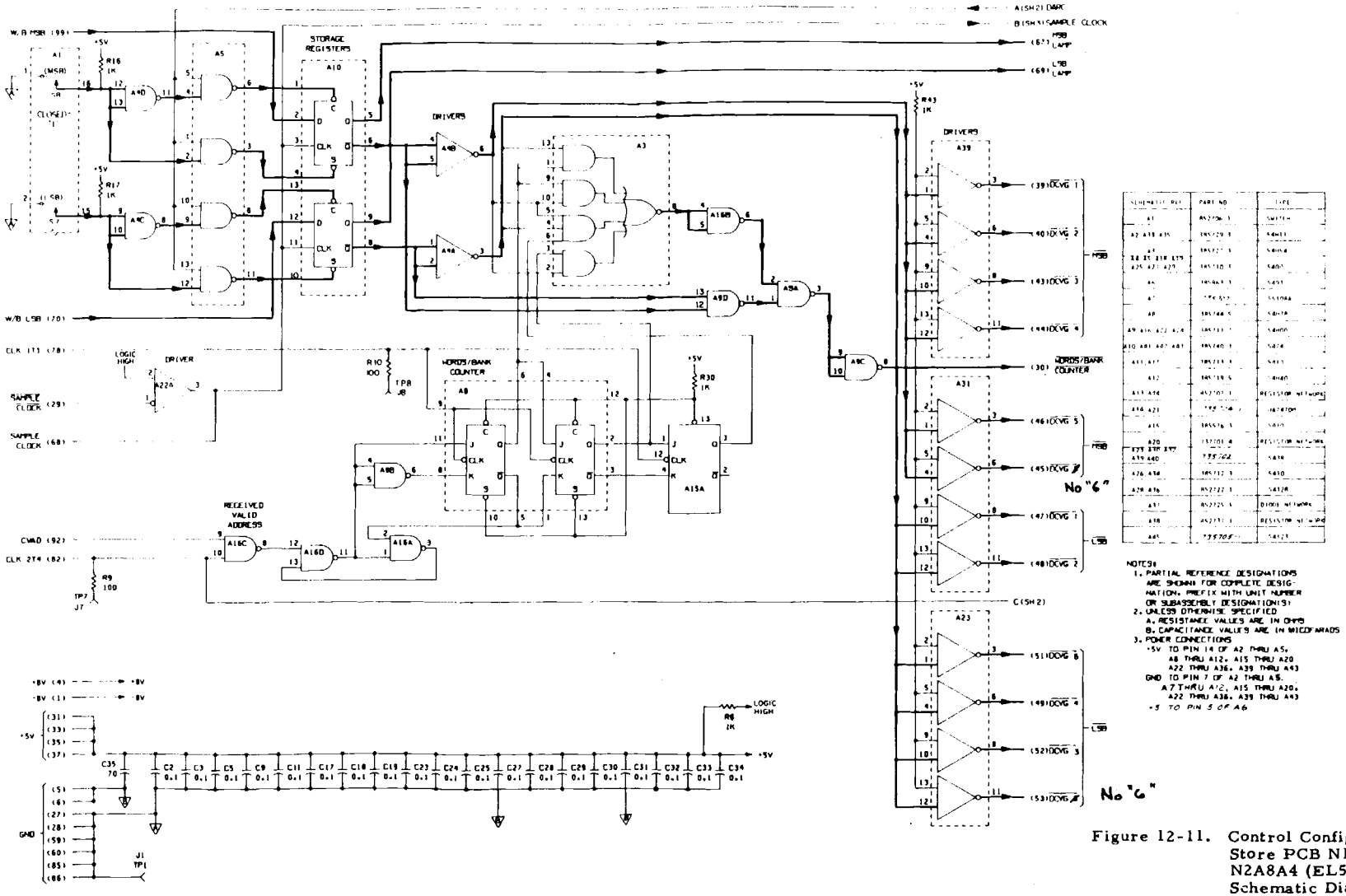
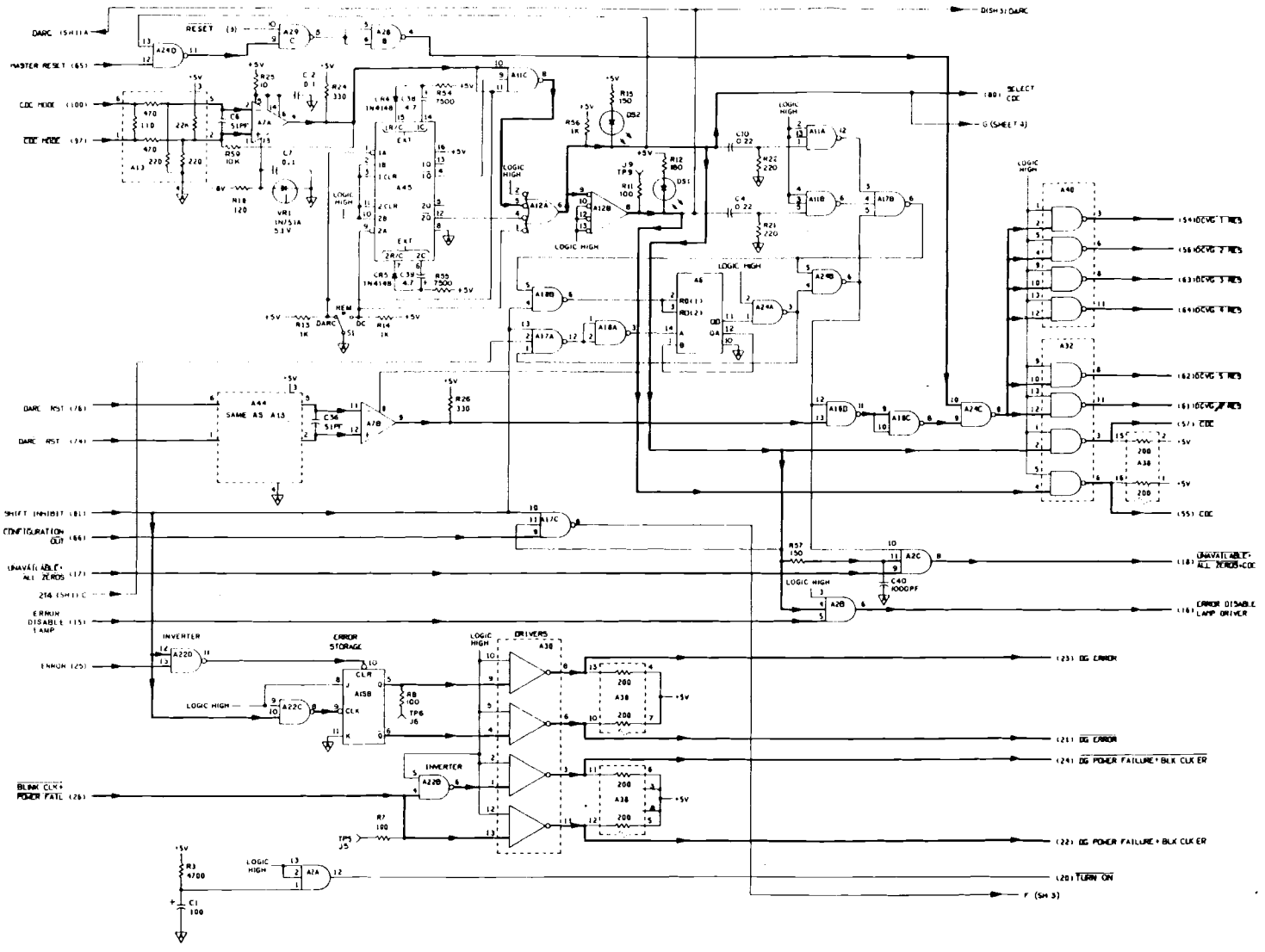


Figure 12-11. Control Configuration Store PCB N1A8A4, N2A8A4 (EL578899-1H) Schematic Diagram (Sheet 1 of 4)



No "6"

Figure 12-11. Control Configuration Store PCB N1A8A4, N2A8A4 (EL578899-1H) Schematic Diagram (Sheet 2 of 4)

Section 3 - XAØ6 Board Documentation

This section contains all the documentation pertinent to the design and fabrication of the XAØ6 driver board and the XAØ6-J jumper board. For the XAØ6 board, this documentation includes schematics (5 sheets), a parts list, a parts location diagram, printed circuit layout diagrams, and a dimensional drawing. For the XAØ6-J board, only the printed circuit layout diagrams and the dimensional drawing are given.

Modifications to the XAØ6 printed circuit boards were made in order to include additional circuitry found to be required after the boards were fabricated and to correct an error not discovered in the original layout artwork. These modifications are indicated by an asterisk (*) next to the added line on the schematic. The modifications are not shown on the printed circuit layout diagrams. The changes made were as follows:

1. The foil pattern connecting pin 2 of U2 with pin 4 of U6 was broken near pin 4 of U6 and a jumper wire was installed between pin 5 of U6 and the foil pattern connected to pin 2 of U2. This was to correct an artwork error.

2. A jumper wire was installed between the ground bus and backplane connector pad 77.

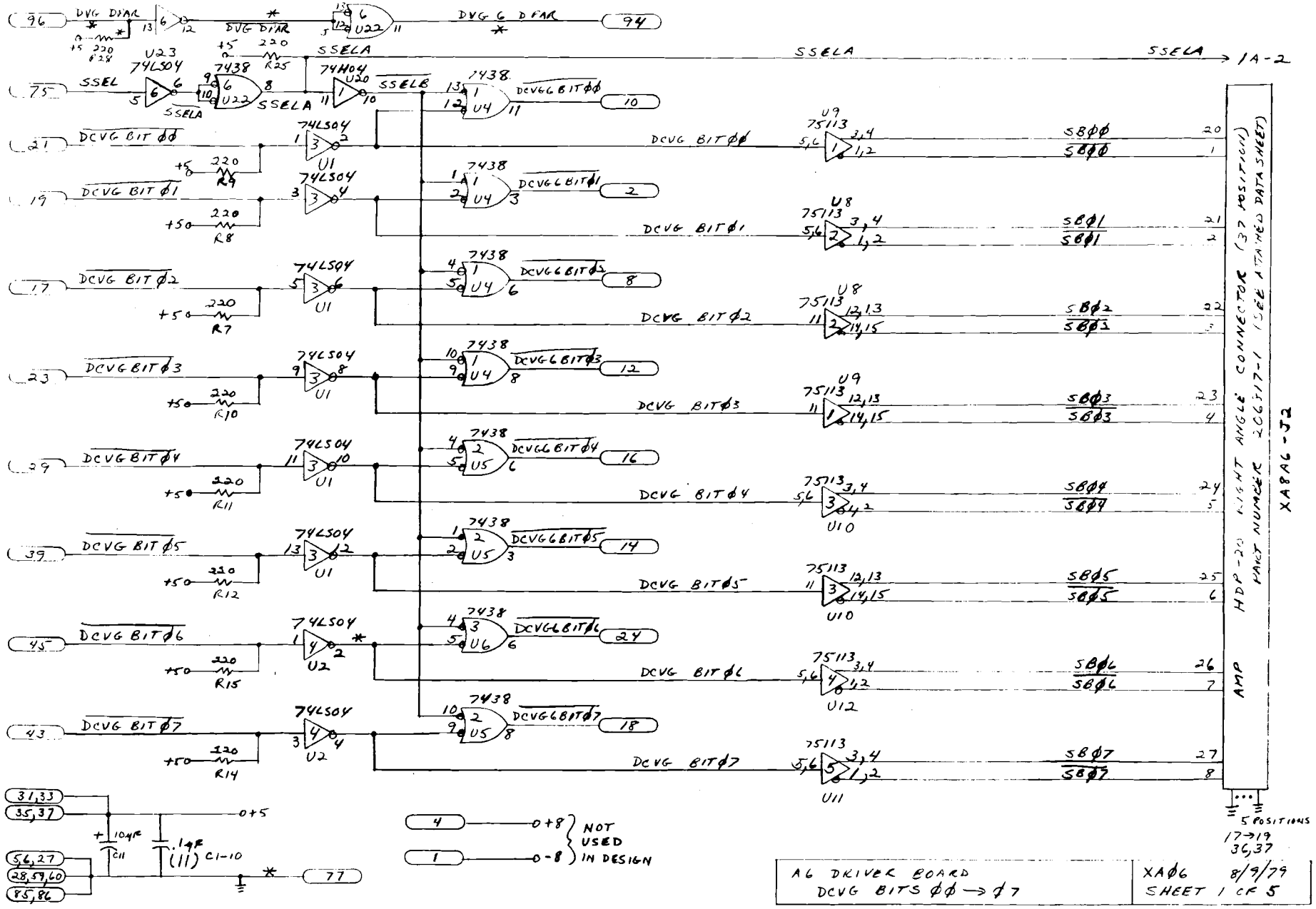
3. A jumper wire was installed between backplane connector pad 96 and pin 13 of U23.

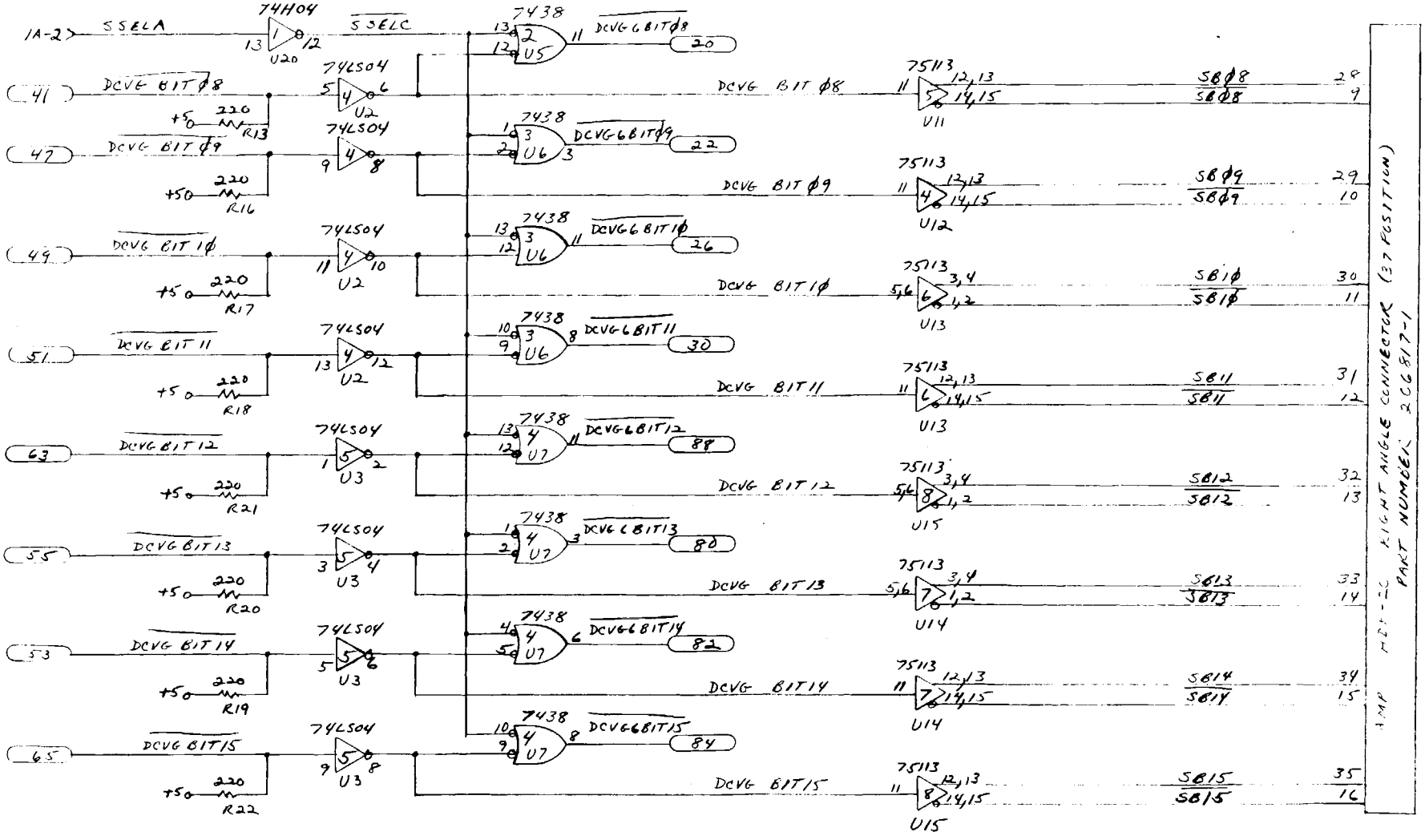
4. A 220 OHM (1/4 W) resistor was installed between backplane connector pad 96 and the +5V power bus.

5. A jumper wire was installed between pin 12 of U23 and pins 12 and 13 of U22.

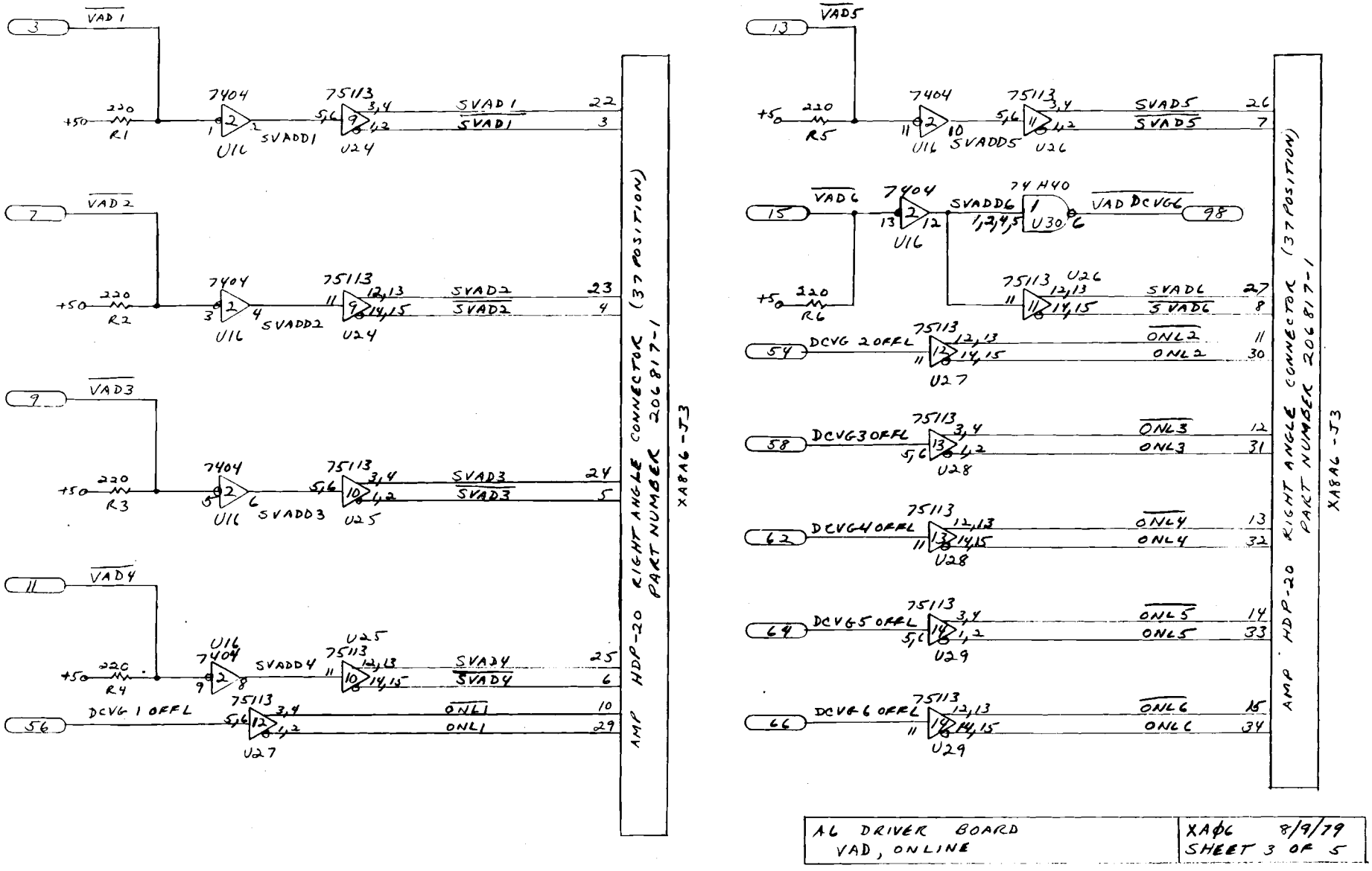
6. A jumper wire was installed between pin 11 of U22 and backplane connector pad 94.

Sockets were installed for all integrated circuit components used on the board so as to provide ease of replacement in the event of a component failure. All discrete components, including capacitors, resistors, and connectors, were soldered directly to the board. On sheet 5 of the schematics, a user option is shown which allows for the selection of the value of the termination resistor used at the input to the differential line receiver U21. By connecting a jumper wire between pins 6 and 7, use can be made of the internal termination resistor which has a nominal value of 130 ohms. Resistors of other values may be installed between pins 5 and 7 with no jumper between pins 6 and 7. This line receive is used to receive a signal which is used to control the state of the differential output drivers which supply signals to the RIB. Using this control signal and SN75113 dual differential line drivers with tri-state outputs, the output lines from several XAØ6 boards can be tied together to perform a tri-state multiplexing function. This could be used in the future to expand the capacity of each port in multiples of 6 DCVG's.

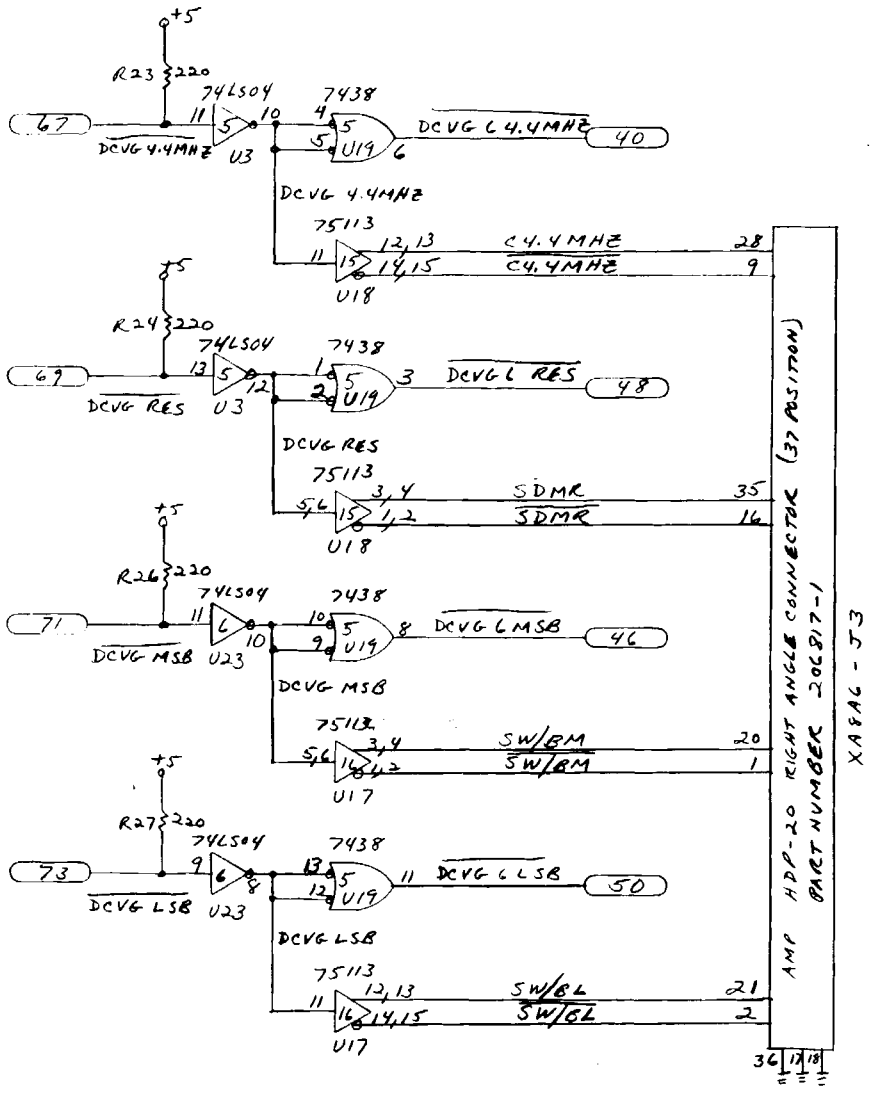

DVG DIAG
DVG G DIAG
SSELA
SSELB
DCVG BIT ØØ
DCVG BIT Ø1
DCVG BIT Ø2
DCVG BIT Ø3
DCVG BIT Ø4
DCVG BIT Ø5
DCVG BIT Ø6
DCVG BIT Ø7
74LS04
7438
74H04
75113
220
+5
U1
U2
U4
U5
U6
U8
U9
U10
U11
U12
R4
R8
R7
R10
R11
R12
R15
R14
SBØØ
SBØ1
SBØ2
SBØ3
SBØ4
SBØ5
SBØ6
SBØ7
HDP-20 RIGHT ANGLE CONNECTOR (37 POSITION)
PART NUMBER 2061J7-1 (SEE ATTACHED DATA SHEET)
AMP
XA8A6-J2
5 POSITIONS
17→19
36,37
31,33
35,37
5,6,27
28,59,60
85,86
.1µF (11) C1-10
10µF C11
NOT USED IN DESIGN
AG DRIVER BOARD
DCVG BITS ØØ → Ø7
XAØ6 8/9/79
SHEET 1 OF 5



A6 DRIVER BOARD DCVG BITS Ø8 → 15	XAØ6 8/9/79 SHEET 2 OF 5

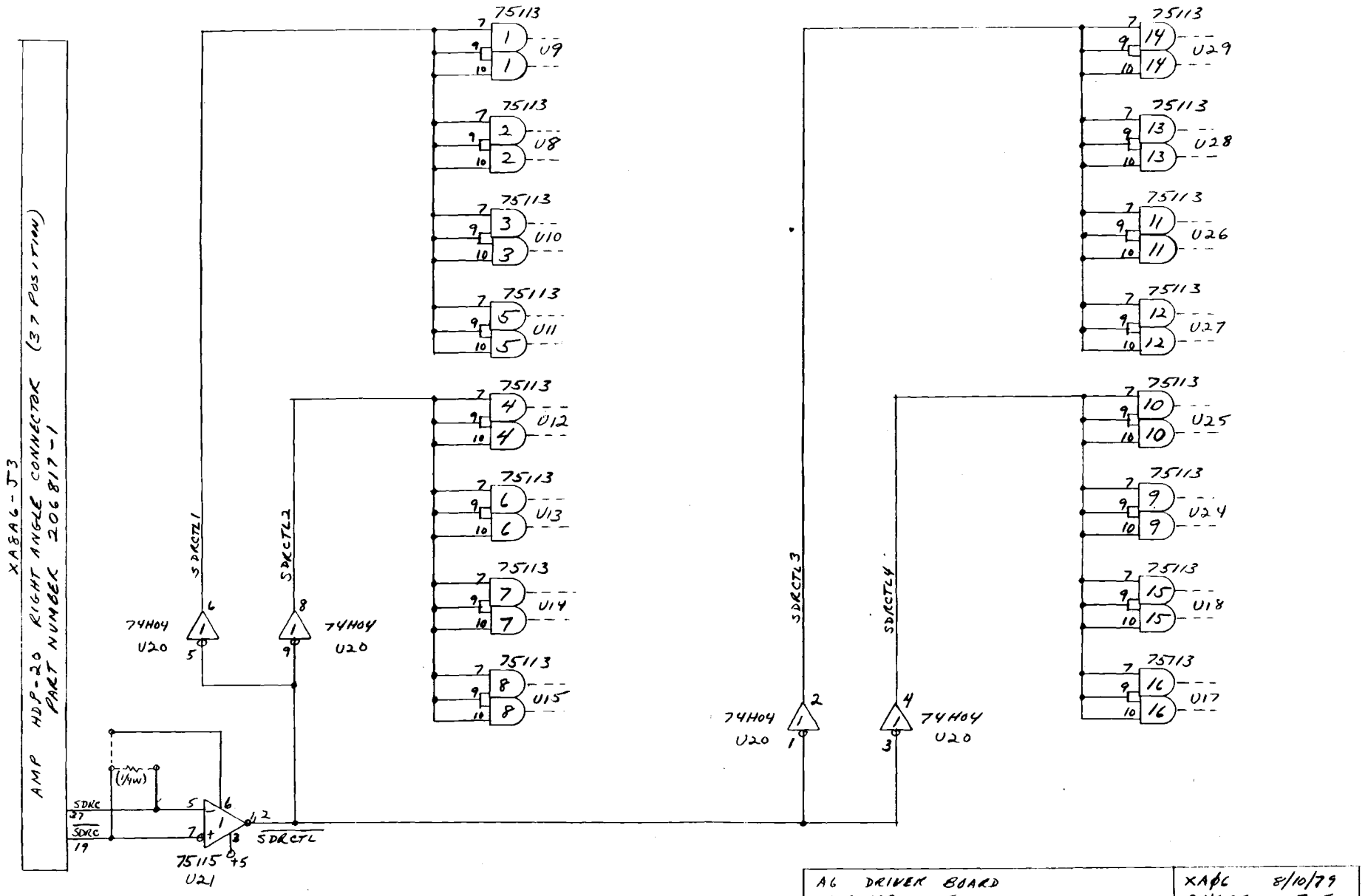


A6 DRIVER BOARD VAD, ONLINE	XAØ6 8/9/79 SHEET 3 OF 5



(B-30)

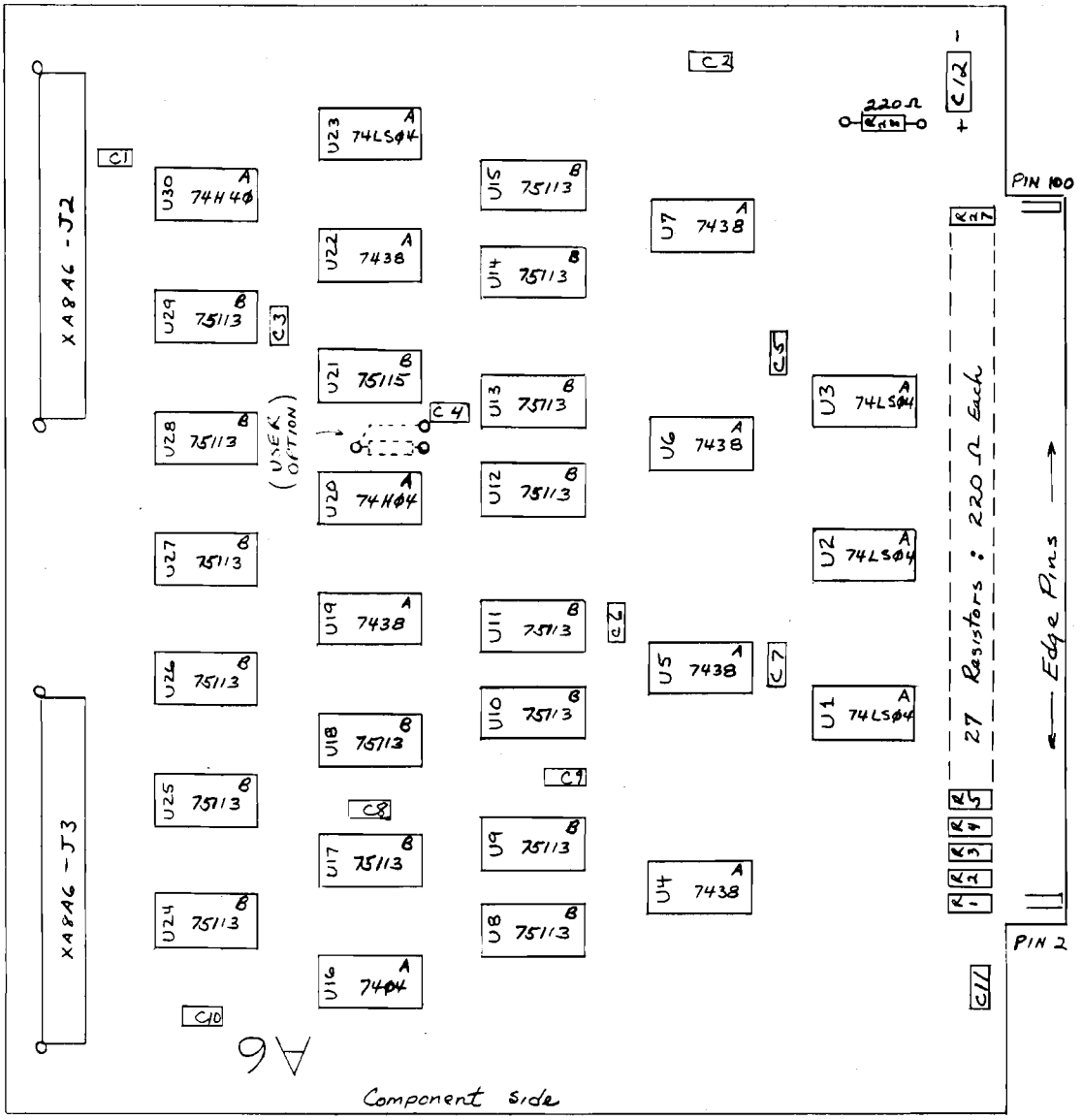
A6 DRIVER BOARD 4.4 MHz, MR, W/B	XA06 8/10/79 SHEET 4 OF 5



A6 DRIVER BOARD DRIVER CONTROL	XA8C 8/10/79 SHEET 5 OF 5

PARTS LIST

TYPE	QUANT.	DESCRIPTION	LOCATIONS
7404	1	Hex nverter	U16
74H04	1	" , High Speed	U20
74LS04	4	" , Low power Schottky	U1-3, U23
7438	6	Quad 2-input positive-NAND Buffers, with open-collector outputs	U4-7, U19, U22
74H40	1	Dual 4-input positive-NAND Buffers, High Speed	U30
75113	16	Dual Differential Line Drivers with Tri-state outputs	U8-15, U17, U18, U24-29
75115	1	Dual Differential Line Receivers	U21
583527-1	13	14-pin IC socket, AMP INC.	U1-7, U16, U19, U20, U22, U23, U30
583529-1	17	16-pin IC socket, AMP INC.	U8-15, U17, U18, U21, U24-29
206817-1	2	Receptacle assembly, 37 position AMP INC.	XA8A6 J2, XA8A6 J3
Resistor	28	220 Ohms, 1/4 W	R1-28
Capacitor	10	0.1 uF, ceramic	C1-10
Capacitor	1	10 uF, tantalum electrolytic	C11

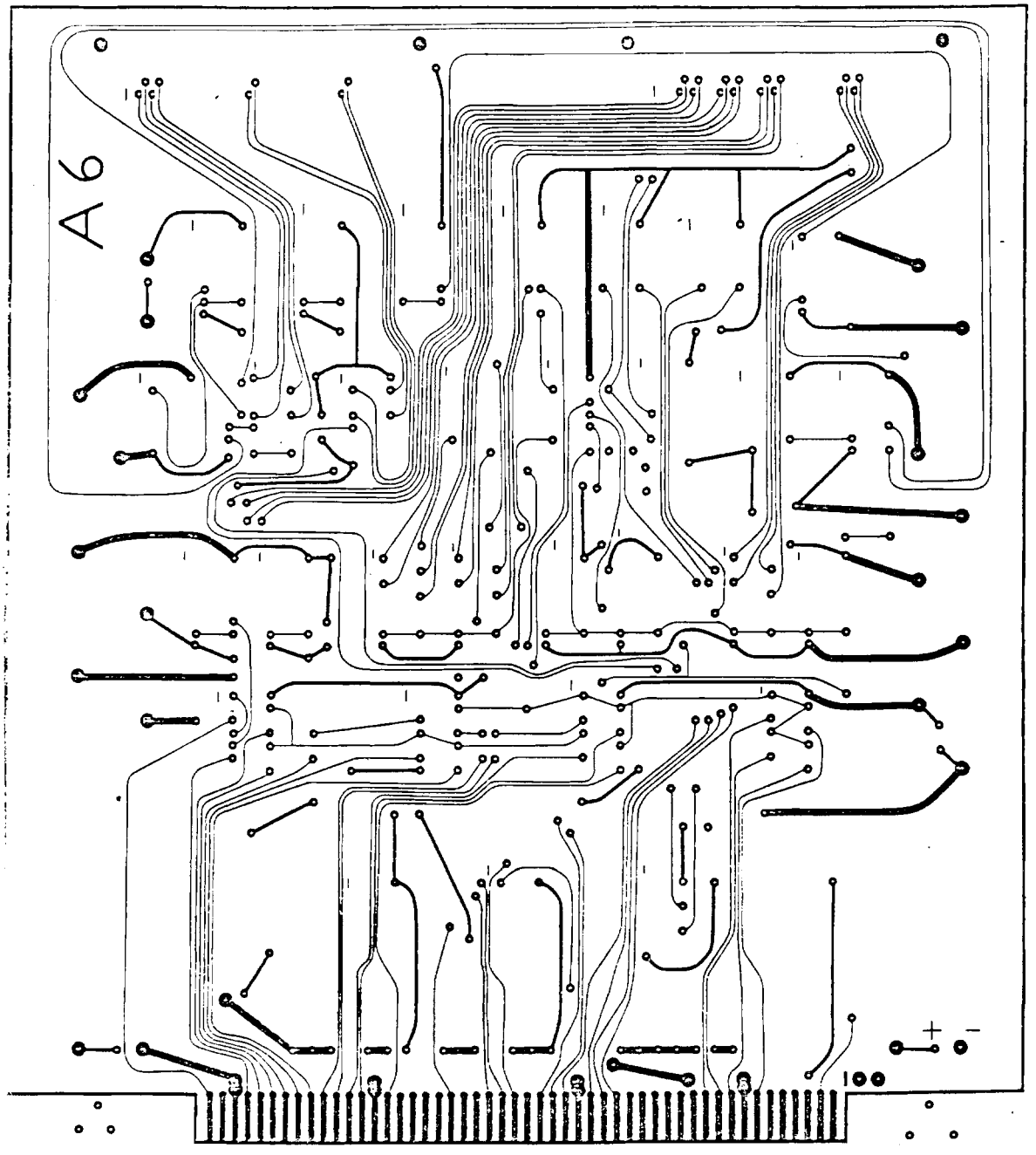


A6 Card Component Layout Sketch

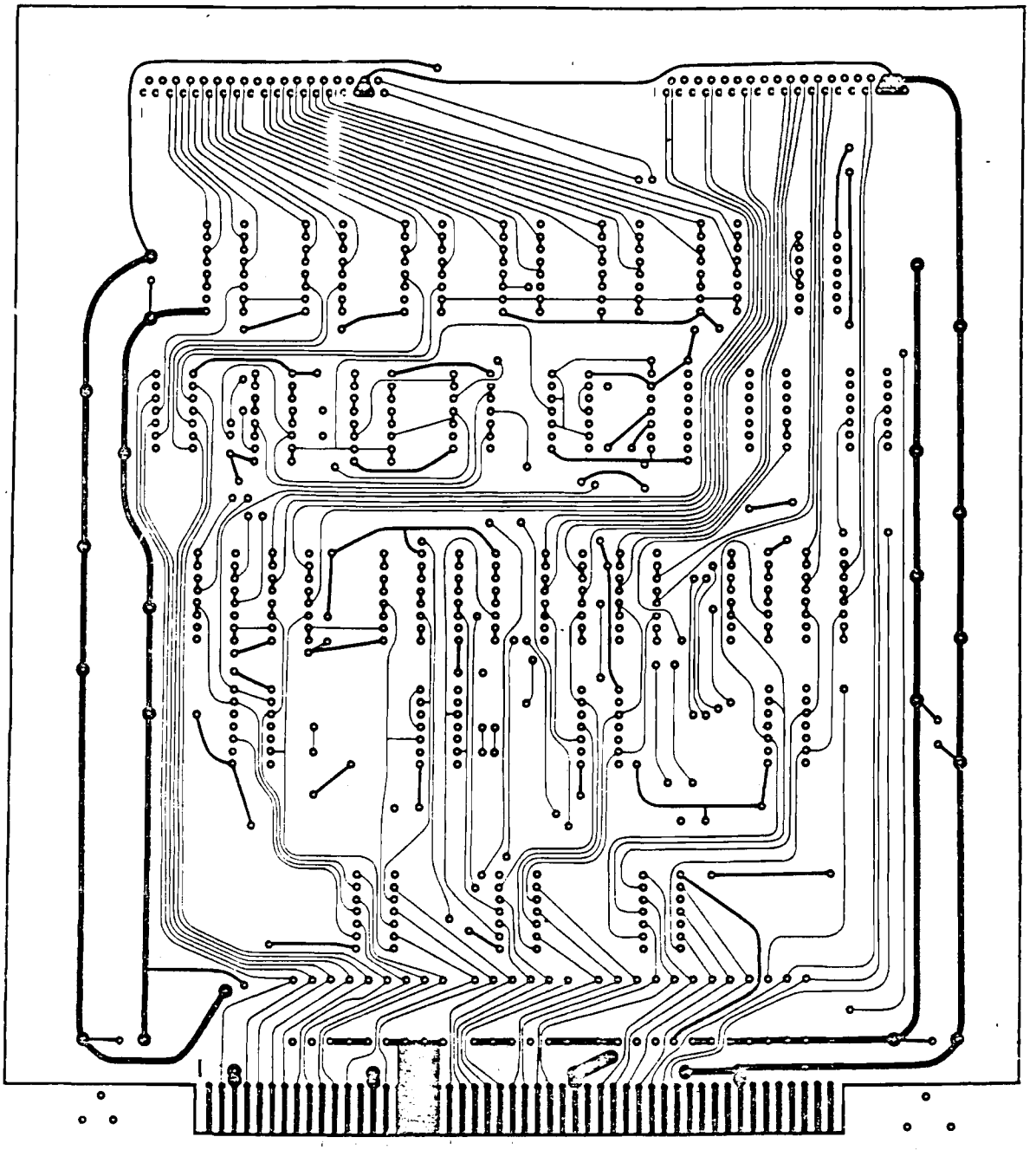
Not to Scale

C1-11 = 0.1 uf Capacitors
C12 = 10 uf Electrolytic Capacitor

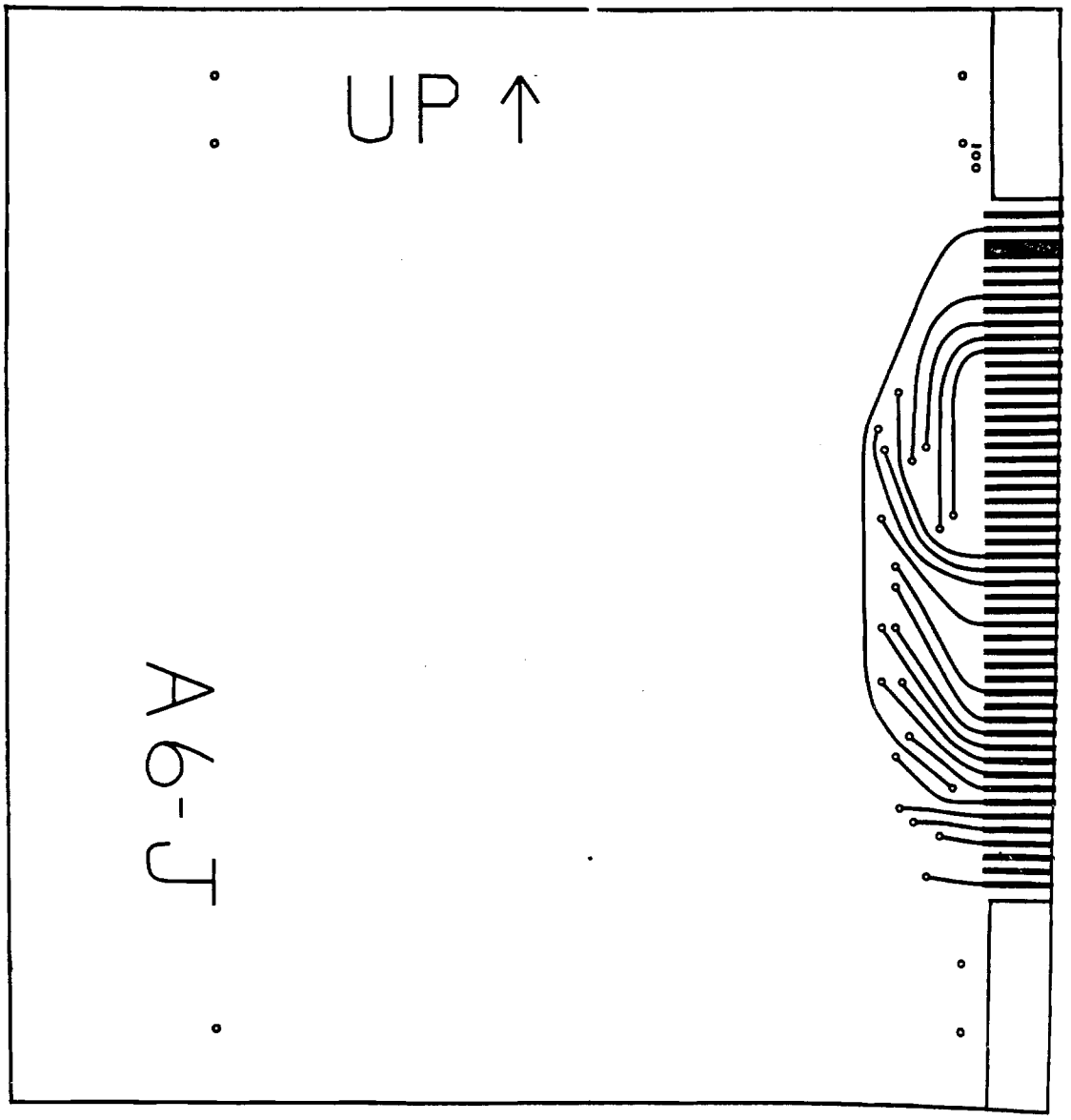
A - 14-PIN SOCKET
B - 16-PIN SOCKET



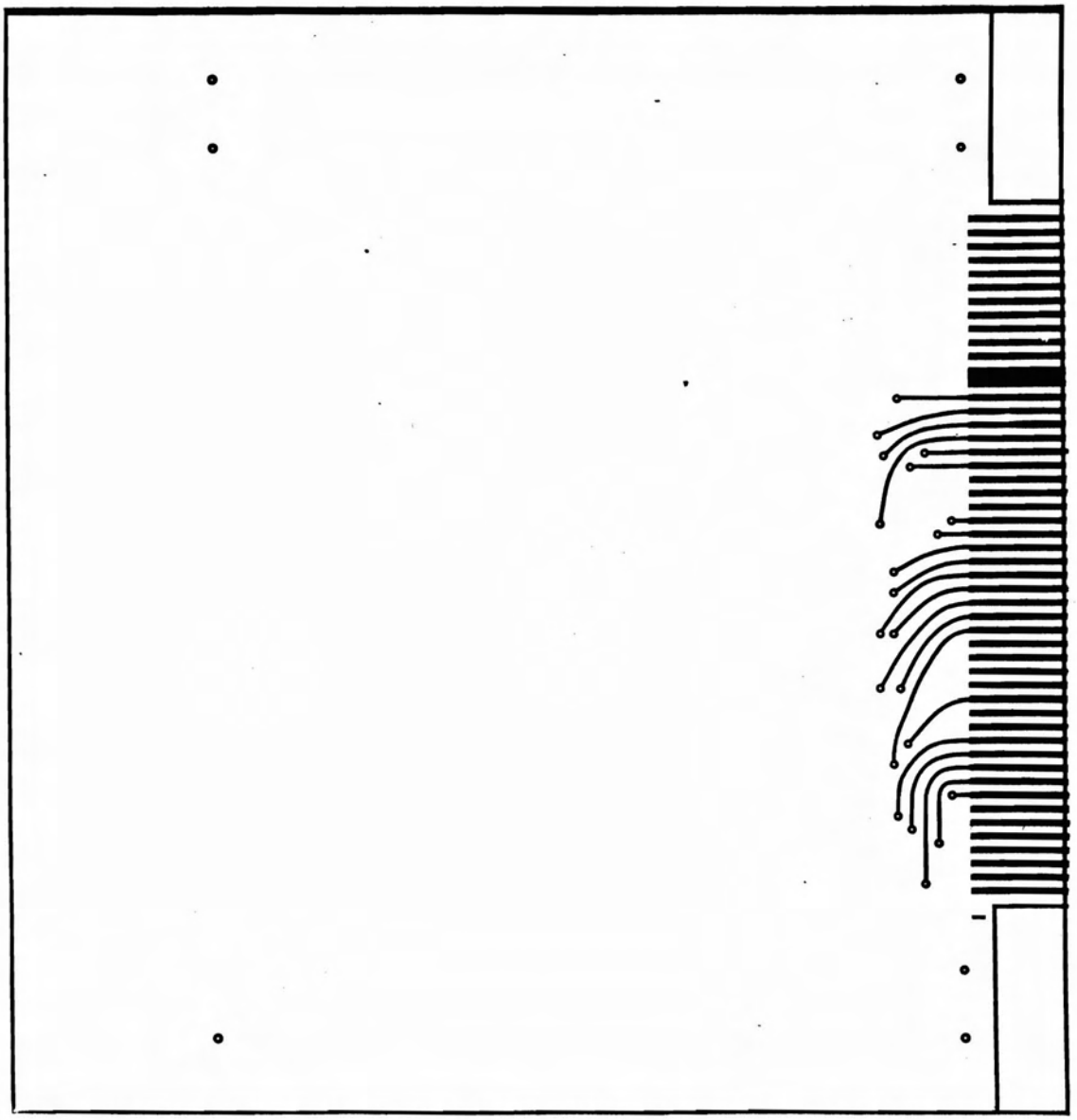
PRINTED CIRCUIT LAYOUT DIAGRAM - XAØC
COMPONENT SIDE



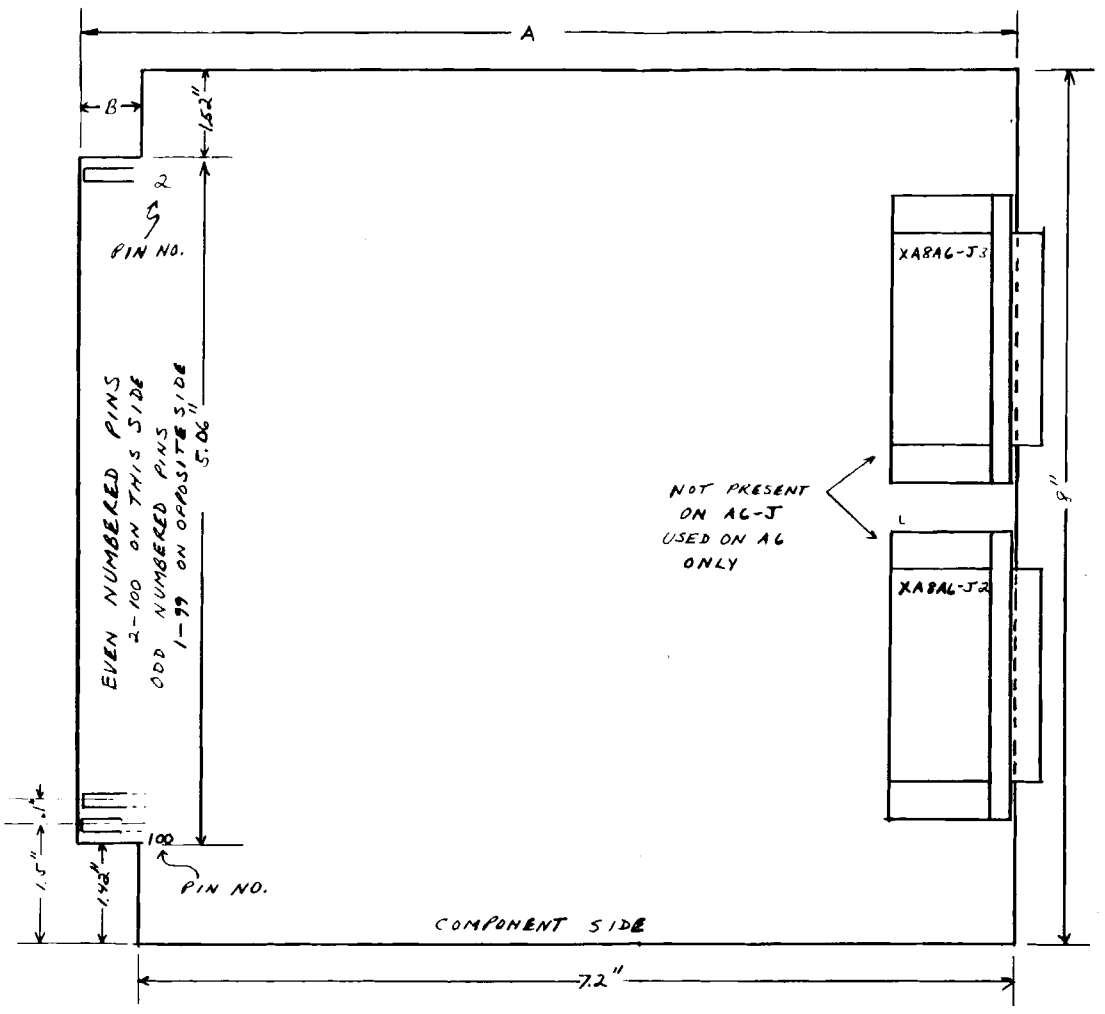
PRINTED CIRCUIT LAYOUT DIAGRAM - XAØ6
SOLDER SIDE



PRINTED CIRCUIT LAYOUT DIAGRAM - XAØ6-J
EVEN-PIN SIDE



PRINTED CIRCUIT LAYOUT DIAGRAM - XAØ6-J
ODD-PIN SIDE



DIMENSION	A6	A6-J
A	7.6"	7.7"
B	0.4"	0.5"

NOTE: THE FOLLOWING EDGE CONNECTIONS ARE ALREADY COMMITTED ON THE BACKPLANE

+5	31, 33, 35, 37
GND	5, 6, 27, 28, 59, 60, 85, 86
+8	4
-8	1

MATERIALS: 1/16 INCH THICK EPOXY GLASS BOARD; TWO-OUNCE COPPER CLAD PER SIDE.
SEE CONTRACT FOR PLATING SPECIFICATIONS.
PLATED-THROUGH HOLES USED ON A6 ONLY.

A6 DRIVER BOARD AND A6-J JUMPER BOARD OUTLINE DRAWING	XAØ6/J 8/9/79 SHEET 1 OF 1

APPENDIX C

PHOTOGRAPHS OF ERDIRS ENGINEERING MODEL EQUIPMENTS

LIST OF ILLUSTRATIONS

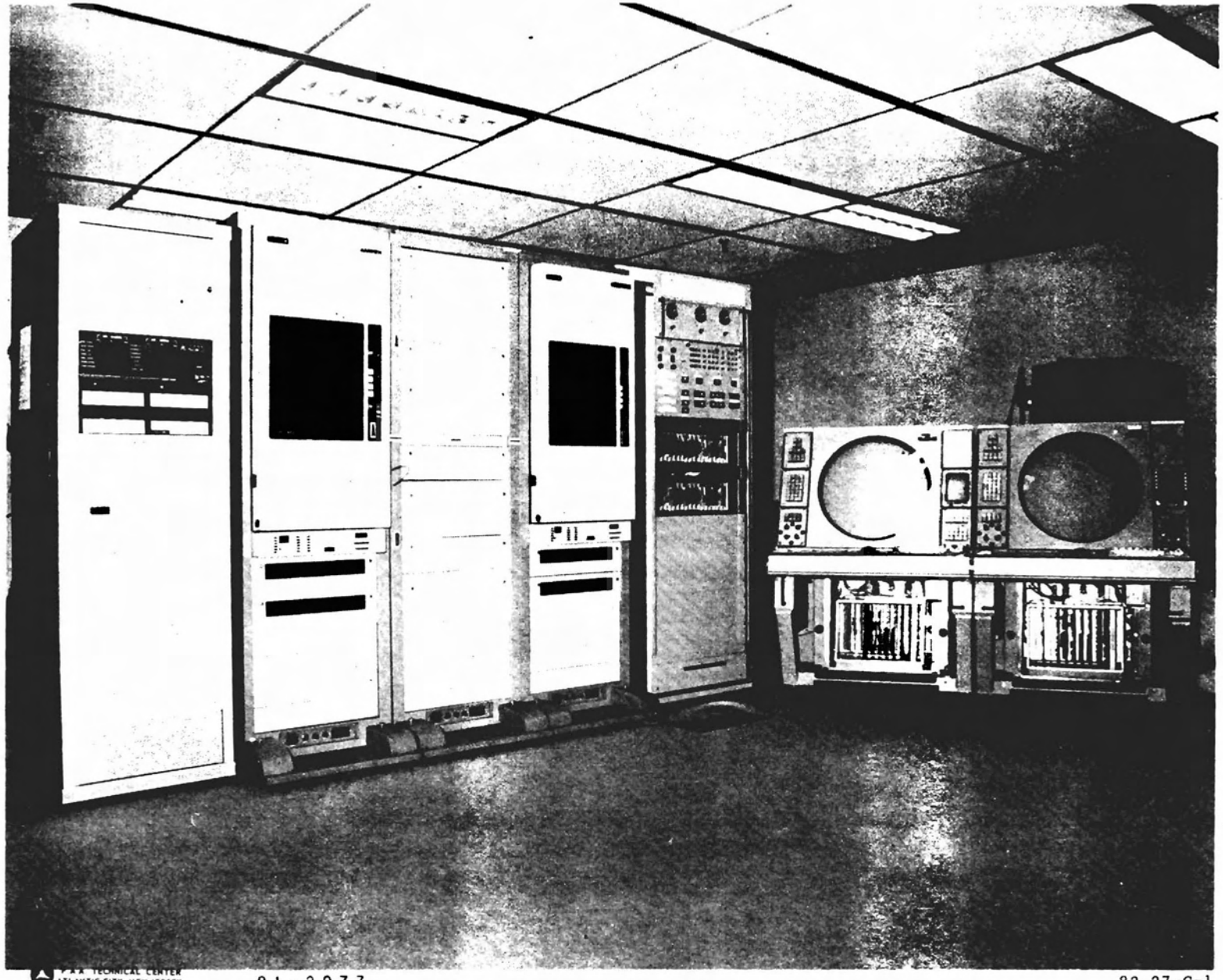


FIGURE C-1. ERDIRS ENGINEERING MODEL

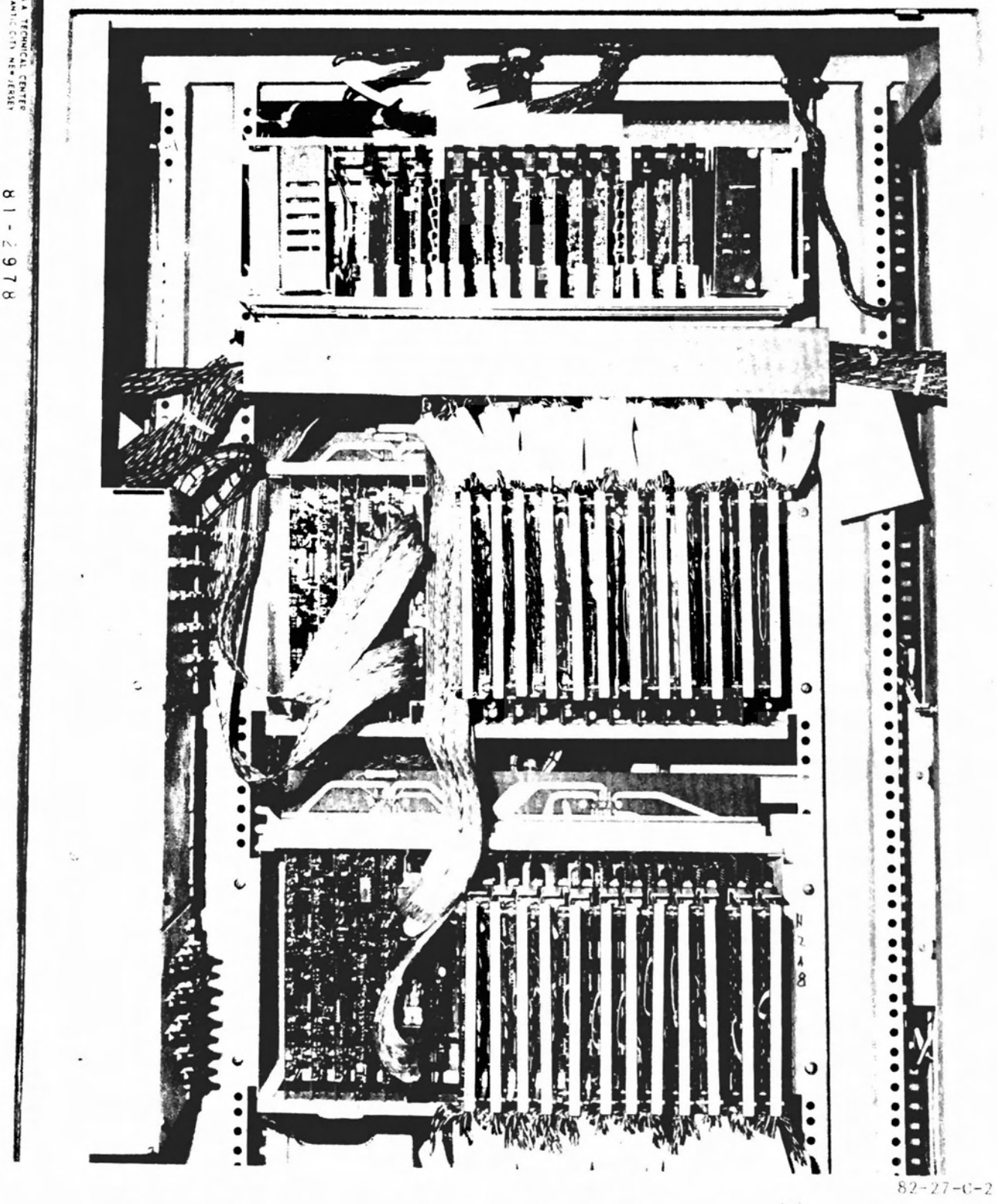


FIGURE C-2. DUAL RIB LOCATED IN DG CABINET ABOVE DGI/O BASKETS

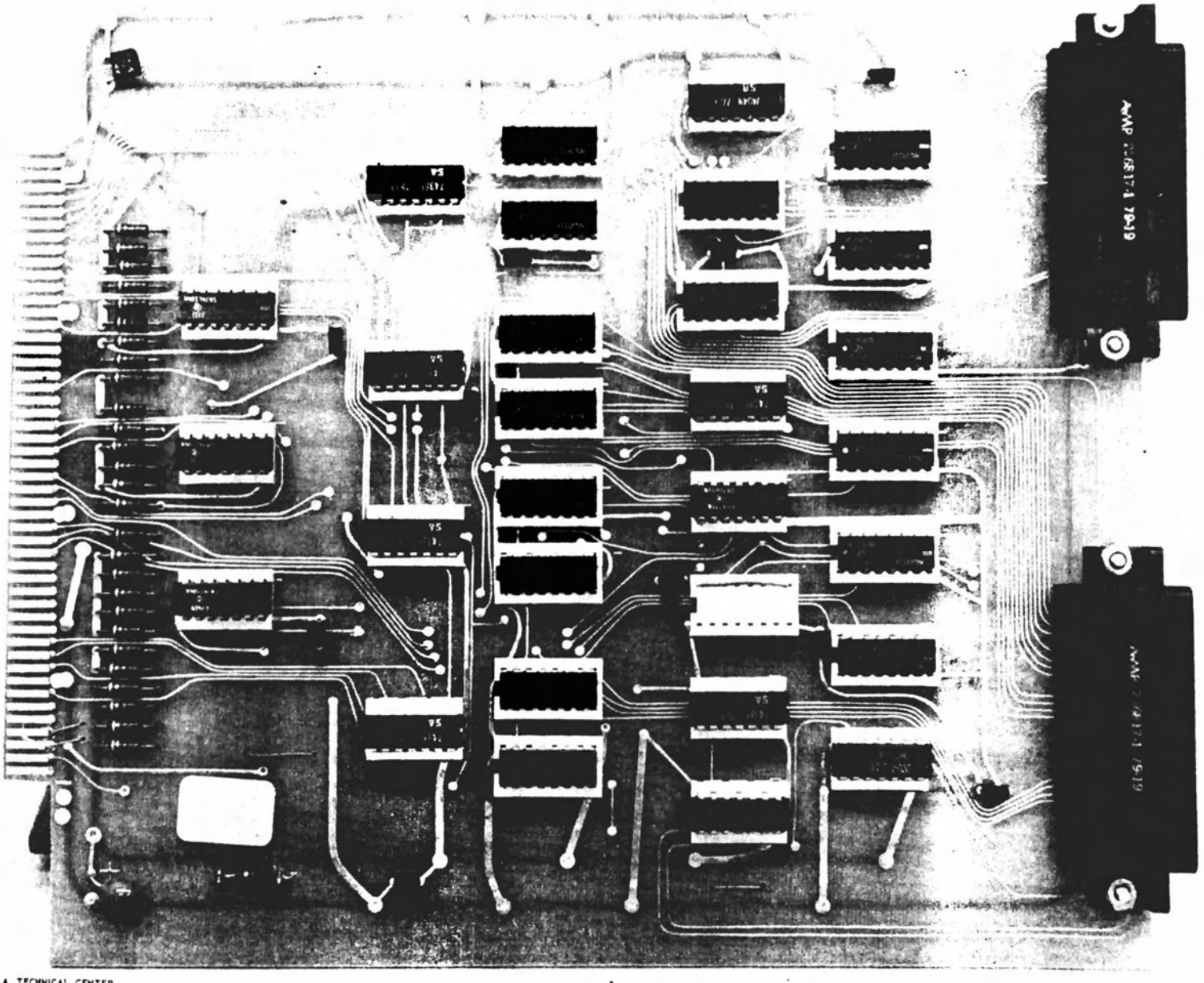


FIGURE C-3. A6 DRIVER BOARD

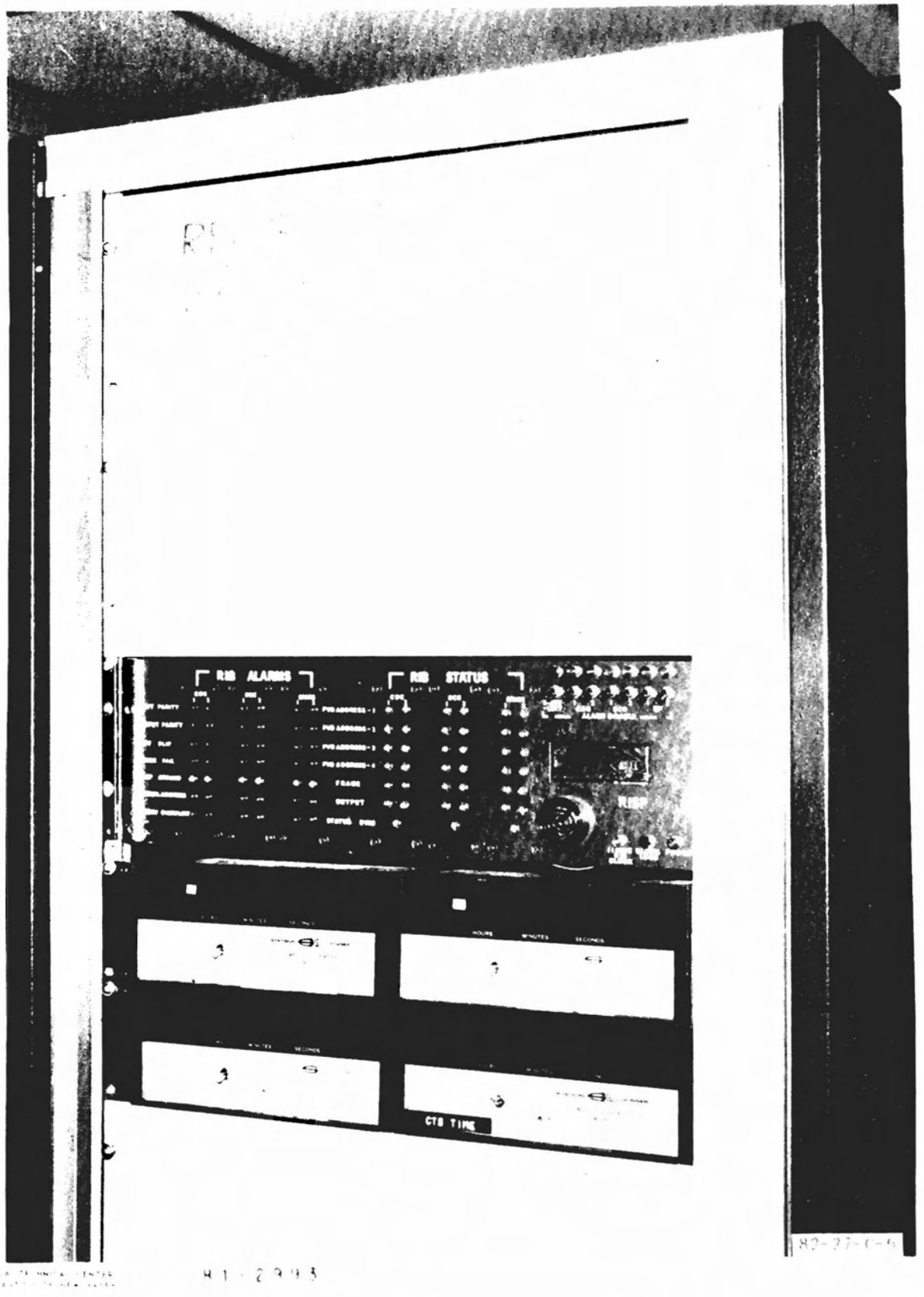


FIGURE C-4. RISP FRONT PANEL

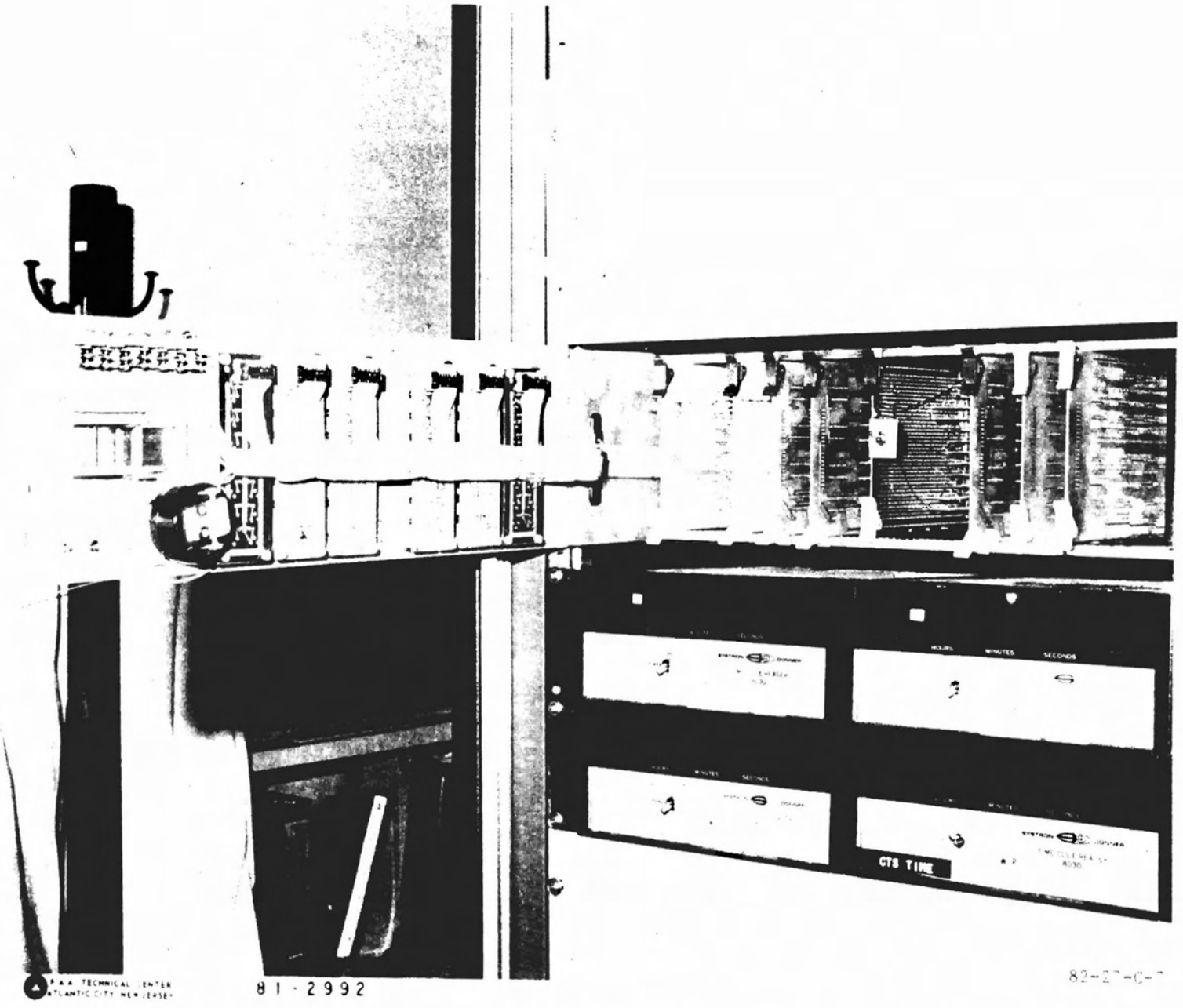


FIGURE C-5. RISP CARD CAGE — PANEL OPEN

FIGURE C-6. HDD RECORDERS

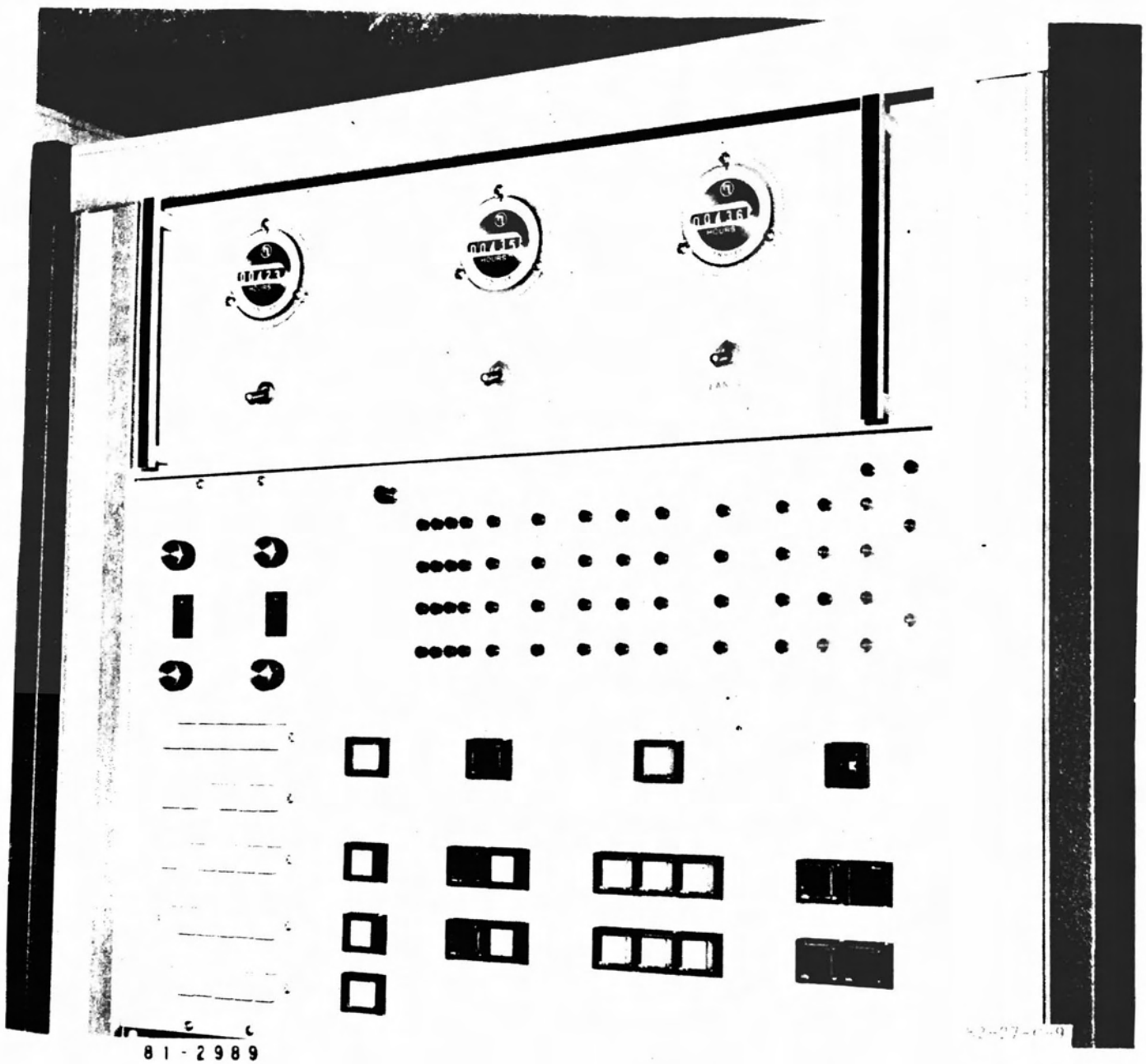


FIGURE C-7. EPIC FRONT PANEL

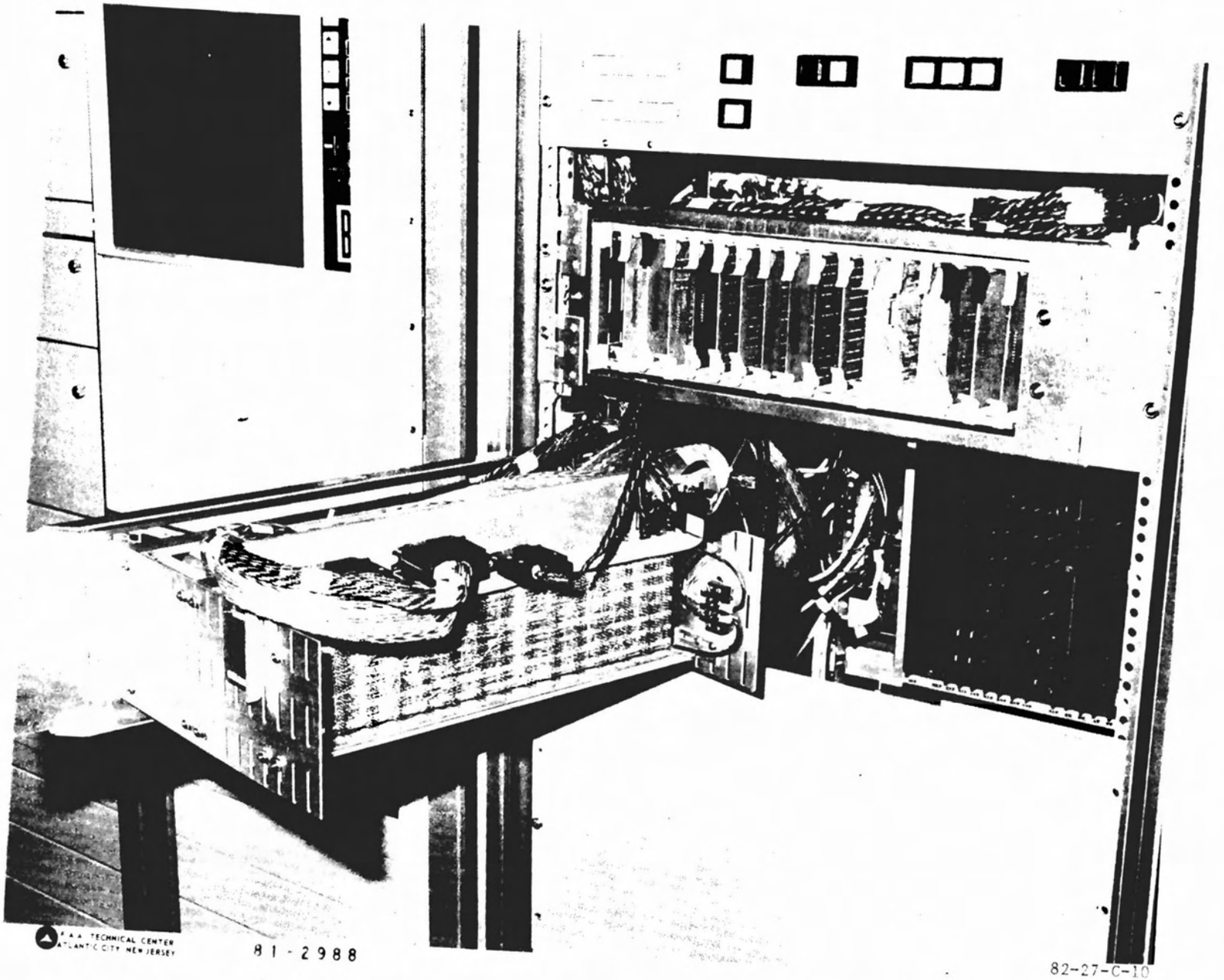


FIGURE C-8. EPI CARD CAGES — ONE CAGE PULLED OPEN

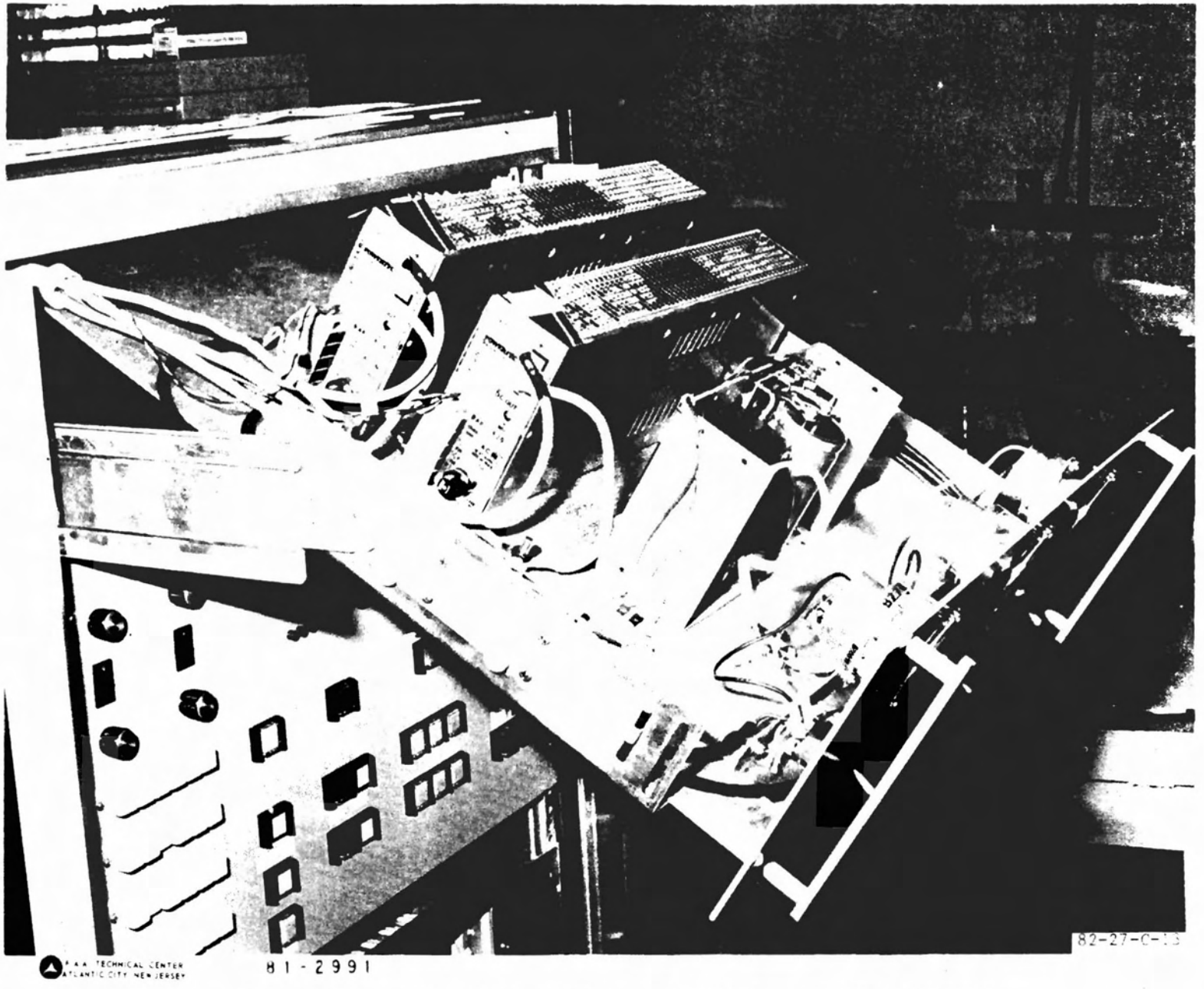


FIGURE C-9. EPIC POWER SUPPLY — DRAWER OPEN AND TILTED DOWN

APPENDIX B

DRAFT SPECIFICATION FOR EN ROUTE RADAR DISPLAY RECORDING SYSTEM (ERDIRS)

TABLE OF CONTENTS

1. SCOPE.

1.1 SCOPE.

This specification establishes requirements for the design, development, fabrication, testing, delivery, installation, and checkout of an En Route Radar Display Recording System (ERDIRS) in production quantities as specified in the contract. ERDIRS's are to be installed at each of 20 Air Route Traffic Control Centers (ARTCC), at the Federal Aviation Administration (FAA) Technical Center, and at the FAA Academy. These systems will be used to record all air traffic control data presented to the en route Plan View Displays (PVD's) and, when required, to play back this data for purposes of situation analysis, training, and other related uses.

At the present time, data is recorded at several points in the en route air traffic control system but there is a need to record data at the display end of the system at a point as close to the PVD as is possible and practical. This point close to the PVD would also minimize the amount of operational type equipment required for playback purposes. The ERDIRS will provide this recording capability and will be designed to interface with both the Computer Display Channel (CDC) and the Display Channel Complex (DCC) equipments.

To the extent practical, the ERDIRS shall be designed using off-the-shelf equipment and modules and presently demonstrable techniques.

2. APPLICABLE DOCUMENTS.

2.1 GENERAL.

The following specifications standards, publications, and amendments or supplements thereto, form a part of this document and are to be used to the extent specified herein.

2.2 FAA DOCUMENTS.

2.2.1 FAA Specifications.

FAA-G-1375a	Spare Parts Peculiar for Electronics, Electrical, and Mechanical Equipment.
FAA-G-2100	Supplement 4 — Electronic Equipment, General Requirements, FAA List of Applicable Documents.
FAA-G-2100/1	Electronic Equipment, General Requirements Part I. Basic Requirements for All Equipments.
FAA-G-2100/3	Electronic Equipment, General Requirements, Part 3, Requirements for Equipments Employing Semiconductor Devices.
FAA-G-2100/4	Electronic Equipment, General Requirements, Part 4, Requirements for Equipments Employing Printed Wiring Techniques.

FAA-G-2100/5	Electronic Equipment, General Requirements, Part 5, Requirements for Equipments Employing Microelectronic Devices.
FAA-D-2494/1	Technical Instruction Book Manuscripts; Part 1, Preparation of Manuscript.
FAA-D-2494/2	Technical Instruction Book Manuscripts; Part 2, Preparation of Reproducible Copy and Original Artwork.

2.2.2 FAA Standards.

FAA-STD-007	PERT Procedures for Contractor or Grantee Use.
FAA-STD-010C	Graphic Symbols for Digital Logic Diagrams.
FAA-STD-016	Quality Control System Requirements.
FAA-STD-020	Transient Protection, Grounding, Bonding and Shielding Requirements for Equipment.

2.2.3 FAA Manuals.

Radar Display Subsystem (RDS) Display Generator (DG) (Raytheon Corporation)	Volume I-II
Radar Display Subsystem (RDS) Display Control and Vector Generators (DCVG's) (Raytheon Corporation)	Volume I-III
Plan View Display Console and Plan View Display Monitor Console (Raytheon Corporation)	Volume I-II
Coded Time Source System Type FA-7952 (Electronic Laboratories, Inc.)	Volume I-II
System Maintenance Monitor Console Type FA-8770 (Electronic Laboratories, Inc.)	Volume I-IV

2.2.4 FAA Design Data.

En Route Radar Display Recording System (Engineering Model)
System Design Data, Engineering Model, (FAA)

2.3 MILITARY DOCUMENTS.

2.3.1 Military Standards.

MIL-STD-461a	Electromagnetic Interference Characteristics.
MIL-STD-470	Military Standard, Maintainability Program Requirements for Systems and Equipment.
MIL-STD-471	Maintainability Verification/Demonstration/Evaluation.
MIL-STD-883	Test Methods and Procedures for Microelectronics.
MIL-STD-481a	Configuration Control — Engineering Changes, Deviations and Waivers.
MIL-STD-721	Definition of Terms for System Effectiveness.
MIL-STD-756	Reliability Prediction.
MIL-STD-781C	Reliability Tests, Exponential Distribution.
MIL-STD-785	Reliability Programs for Systems and Equipment Development and Production.
MIL-E-17555	Electronic and Electrical Equipment, Accessories and Repair Parts; Packaging and Packing of.

2.3.2 Military Handbooks.

MIL-HDBK-217C	Reliability Stress and Failure Rate Data for Electronic Equipment.
MIL-HDBK-472	Maintainability Prediction.

2.4 OTHER PUBLICATIONS.

2.4.1 Inter-Range Instrumentation Group Standards.

IRIG 106-80	Telemetry Standards
IRIG 118-75	Test Methods for Telemetry Systems

2.4.2 Miscellaneous Documents.

National Electric Code

2.5 COPIES OF DOCUMENTS.

Copies of the applicable FAA specifications and standards may be obtained from the Federal Aviation Administration, Washington, D.C. 20591, Attention: Contracting Officer. Requests should fully identify material desired; i.e., specification numbers, dates, amendment numbers, etc.; also, requests should identify the invitation for bids, request for proposals, or the contract involved, or other

use to be made of the requested material. The referenced FAA manuals (paragraph 2.2.3) will be available for inspection at the times and locations specified in the RFP.

Single copies of Military Documents may be obtained from the Naval Supply Depot, 5801 Tabor Avenue, Philadelphia, Pa. 19120. Mail requests should cite the invitation for bids, request for proposals, or contract for which the documents are needed.

Information on obtaining copies of Federal Standards may be obtained from General Services Administration Offices in Washington, D.C.; Auburn, Washington; San Francisco, California; Denver, Colorado; Kansas City, Missouri; Atlanta, Georgia; Chicago, Illinois; New York, New York; Boston, Massachusetts; New Orleans, Louisiana; Fort Worth, Texas; and Los Angeles, California.

Information on obtaining copies of the National Electrical Code may be obtained from the National Fire Protection Association, 60 Batterymarch Street, Boston, Massachusetts 02110.

Information on obtaining copies of Electronic Industries Association (EIA) Standards may be obtained from the Electronic Industries Association, 2001 I Street N.W., Washington, D.C. 20006.

Copies of other publications referenced may be obtained from the Federal Aviation Administration, Washington, D.C. 20591, Attention: Contracting Officer. Requests should fully identify material desired; i.e., publication numbers, dates, etc., and use to be made of the requested material.

2.6 PRECEDENCE OF DOCUMENTS.

This specification shall have precedence over all subsidiary documents referenced herein with precedence of these referenced documents being FAA documents, military documents, and other publications, respectively.

3. REQUIREMENTS.

3.1 GENERAL.

The contractor shall provide all necessary services and materials to design, fabricate, test, deliver, install, and checkout the equipments described in this specification, in the quantities and at the times indicated in the contract. Any feature or item necessary for proper operation of the system in accordance with these requirements shall be incorporated even though that item or feature may not be specifically described herein.

3.1.1 System Description.

The En Route Radar Display Recording System (ERDIRS) shall record all display data presented to the air traffic controller's Plan View Display (PVD) and shall be capable of playing back this data in order to provide a reconstruction of the air traffic conditions existing at any particular time.

The ERDIRS equipment configuration required for each operational Air Route Traffic Control Center (ARTCC), shall consist of two subsystems: the Recording Subsystem and the Playback Subsystem. The Recording Subsystem shall perform the functions of sampling and recording display data being sent to all PVD's. It shall also provide the capability of monitoring the sampled display data using both the System Maintenance Monitor Console (SMMC) See-All PVD and the Maintenance PVD. These two PVD's will serve a dual function; they shall be capable of being independently switched between displaying data directly from the display computer and monitoring data being processed by the ERDIRS. In addition, status and alarm information shall be provided at the recording equipment and at the SMMC.

The display data to be recorded shall be picked off at the Display Generator Unit (DGU) which is a common equipment to any of the display computers currently in operational use at the 20 conterminous ARTCC's; i.e., the Computer Display Channel (CDC), the Display Channel Complex (DCC), and the Direct Access Radar Channel (DARC). The government will furnish information to be used in modifying these equipments so that display data can be made available for recording. A Coded Time Source (CTS) available at the ARTCC shall also be recorded.

Recording of data shall be on magnetic tape utilizing paired high-density digital recorders operating in a sequential mode to prevent the loss of data when end of tape is reached. Failure of the active recorder shall result in automatic switchover to the alternate recorder.

There shall be a separate recorder for use in the off-line recording of training data. The recorder used to perform this training recording function shall be identical to, and interchangeable with, those used in recording operational data.

The Playback Subsystem shall perform several functions related to playing back display data. The playback of training data will normally be accomplished using the Training Recorder and two training PVD's designated as playback PVD's. These two playback PVD's will serve a dual function and shall have the capability of being independently switched between the display computer and the ERDIRS.

Within the operational playback function, the capability shall exist to playback operational display data from any two displays simultaneously. Playback shall be performed using the same two playback PVD's utilized in the training area. The Playback Reproducer used to perform the operational playback function shall be identical to the units used elsewhere in the ERDIRS except that it shall be a reproducer only.

The capability shall exist during playback to time synchronize the playback of display data tapes with an associated voice data tape which will be played back on a government-owned voice reproducer.

Based upon the number of displays at each individual ARTCC, it may be necessary to use more than one operational recorder pair to record all display data. Thus display data from two different displays may be recorded on separate tapes. In order to play back display data from these two tapes simultaneously, both the Training Recorder and the Playback Reproducer shall be utilized with the capability of time synchronizing them together. The Playback Reproducer shall act as the master. When they are time synchronized with a Voice Reproducer, the Voice Reproducer shall act as the master.

The Training Recorder shall be used in conjunction with the operational Playback Reproducer to perform tape duplication.

During the recording of training data, the Training Recorder shall be considered a part of the Recording Subsystem. When this same Recorder is used to playback training or operational data, it shall be considered a part of the Playback Subsystem.

A system block diagram of a typical ERDIRS field configuration is shown in figure 1.

3.1.1.1 System Capacity and Growth.

The number of operational and training PVD's varies among ARTCC's; therefore, each system delivered under the contract schedule shall be designed to have a recording capacity tailored to a specific site. The system shall be a modular design capable of being expanded by adding additional modules sufficient for recording data from a maximum of 120 active displays. The number of PVD's to be recorded by each module shall be optimized to keep unused capacity to a minimum. However, the contractor shall provide additional recording capacity in accordance with paragraph 3.2.1.1.4.

3.1.2 Deliverable Items.

The following items shall be furnished in the quantities and at the times and locations specified in the contract schedule:

En route Radar Display Recording System, complete with:

Record Interface Equipment	3.2.1.1.1
Digital Recording Equipment	3.2.1.1.2
Display Data Monitoring Equipment	3.2.1.2.1.1
Status Monitoring Equipment	3.2.1.2.2 3.2.2.2.1
Playback Interface Equipment	3.2.2.1.1
Digital Reproducer	3.2.2.1.2
Maintenance Equipment	3.1.2.1
Documentation	3.5
Spare Parts	3.6.2

3.1.2.1 Maintenance Equipment.

Any special maintenance equipment necessary for proper installation, test, repair, and adjustment of the ERDIRS equipment shall be provided by the contractor. Special maintenance equipment is defined as tools and test equipment required for maintenance of the system and not carried as a standard item by the contractor or

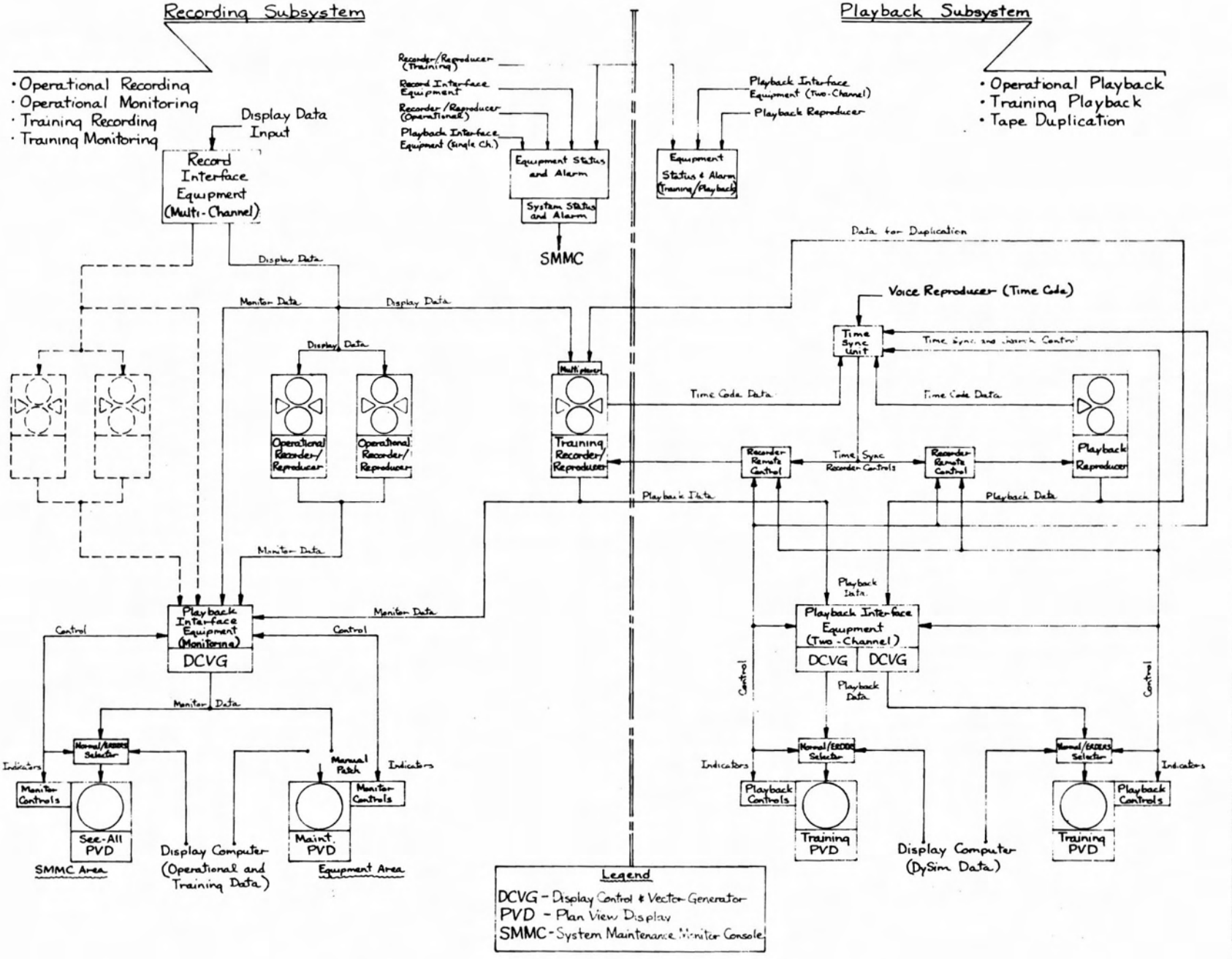


FIGURE 1. ERDIRS BLOCK DIAGRAM

another manufacturer. A list of all special maintenance equipment shall be submitted to the Government for approval. A list of all standard maintenance equipment necessary for proper installation, test, repair, and adjustment of the ERDIRS equipments shall also be provided. This list shall include the manufacturer's name, model, and part numbers.

3.1.3 Government Responsibilities.

These requirements are covered under General Provisions in the RFP.

3.2 SYSTEM FUNCTIONAL REQUIREMENTS.

The functions of the ERDIRS are distributed between two subsystems: the Recording Subsystem and the Playback Subsystem.

3.2.1 Recording Subsystem.

There are two functions associated with the Recording Subsystem: the recording of display data and the monitoring of this recording operation. These two functions are discussed in detail in the following paragraphs.

3.2.1.1 Data Recording.

Data recording shall be performed using digital recorders with interface buffer(s) between the recorders and DGU's. These Recorders shall be called the Operational Recorders. Display data sampled (reference 3.2.1.1.1.3) at a point in the DGU between the DGIO and the DCVG's shall be recorded on magnetic tape. Data to all on-line DCVG's will be sampled and recorded on the Operational Recorders. This data shall include data for all training as well as operational displays. The SMMC See-All PVD is classified as an operational PVD, and even when it is switched to monitoring ERDIRS data, the Recording Subsystem shall continue to record normal operational data being provided to the SMMC See-All PVD. The Maintenance PVD is not an operational PVD. It is located in the display computer equipment room and is used to connect manually into any PVD position. Therefore, any display data being monitored by the Maintenance PVD is already being recorded.

Sampling and recording of display data shall be continuous. Recorder pairs operating in a sequential mode shall be used. Each recorder shall have the capacity of recording all the data for a minimum of 72 PVD's, plus time code data for a minimum of 4 hours before the alternate recorder is automatically activated to continue the recording task.

All training data shall also be recorded on an additional independent digital recorder using the same interface equipment used with the Operational Recorders. This Recorder shall be called the Training Recorder. In an emergency, this unit shall be avaliable for use as a spare for the Operational Recorder.

The training displays are driven by DCVG's in the same manner as the operational displays.

Since training is not a continuous activity, there is no requirement for an alternate recorder.

In addition to the recording of display data, a time code (reference paragraph 3.2.1.1.3) available in each ARTCC shall be recorded on a separate track on all recorders including the Training Recorder.

3.2.1.1.1 Record Interface Equipment.

The interface between the Recorders and the DGU shall be provided by the Record Interface Equipment. Hardwired logic is preferred but a processor with firmware logic will be considered. In addition, it shall be designed to be completely transparent to the operation of the DGU, with the exception of a printed circuit board to provide the actual interface to the DGU, as specified in paragraph 3.2.1.1.1.1, all other parts of the Record Interface Equipment shall be external to the DG cabinet.

A delimiting sync word shall be generated by the Record Interface Equipment so that the Playback Interface Equipment (paragraph 3.2.2.1.1) will be capable of determining the beginning or end of data groups. The recorder deskew words may be used for this purpose. Also, address label data (on an air traffic control sector basis) shall be injected in the recorded data stream at appropriate positions in order to identify the data for each specific PVD for access on playback. This equipment shall have two parallel output ports. One port will supply data to the Operational Recorders while the other port will supply the same data to the Training Recorder.

3.2.1.1.1.1 Display Generator Unit/ERDIRS Record Interface.

The ERDIRS shall obtain the necessary data and control signals from the interface between the DGIO and the input to the DCVG.

3.2.1.1.1.1.1 Display Generator Unit Modification.

To provide the display data and necessary control signals to the ERDIRS, the DGIO assembly within each DGU shall be modified. A common bus within the DGIO supplies the display data to each of six DCVG's through individually gated line drivers (16 per DCVG). This means that each DCVG receives only the data specifically addressed to it. This modification will continuously enable the 16 data line drivers for one DCVG (DCVG No. 6) so that all data for all six DCVG's are available at the output of this one set of drivers. The existing path between the output of these drivers and DCVG No. 6 shall be broken and a new path wired between the drivers and the spare A6 card slot in the DGIO assembly. Utilizing a new printed circuit board, the data available at the input to the new board shall be routed to another set of gated line drivers with the output being connected to the input of DCVG No. 6. The display data path to DCVG No. 6 is now through another level of gates in series with the original gates. The data available at the input to the new gated line drivers shall be routed to a second set of ungated line drivers, the output of which will contain the data for all six DCVG's. This output shall be wired to connectors mounted on the front of the card and will be used to interface with the ERDIRS. Control signals which are sent to the DCVG without being gated will also go through an additional level of logic on the A6 board in order to maintain the same propagation delay as the display data. Additional control signals for the other five DCVG's, and any other control signals necessary; i.e., on-line signals, VAD signals, etc., shall also be routed to the new interface board and made available to the Record Interface Equipment. A detailed description of the DGIO modification is contained in the ERDIRS Engineering Model System Design Data (paragraph 2.2.4).

The new A6 printed circuit board and associated cabling shall be the only contractor-furnished equipment to be contained in the DG cabinet during normal operation. In addition to the new A6 printed circuit board, a jumper board shall also be provided that will restore the normal configuration when installed in place of the A6 board.

3.2.1.1.1.1.2 Display Generator Unit Modification Responsibilities.

The contractor shall utilize the basic design concept specified in paragraph 3.2.1.1.1.1.1 but shall modify or expand it if necessary to insure compatibility with the ERDIRS design. The final design shall be submitted to the FAA for approval. After the design of the interface is approved, the contractor shall deliver two modification kits, including the new printed circuit cards, documentation and installation procedures, to the FAA for installation and testing at the FAA Technical Center. Joint FAA/contractor tests will be conducted at the FAA Technical Center to verify that the modification is compatible with the display computer system. Upon acceptance by the FAA, the contractor shall proceed to fabricate required quantities of these modification kits. These kits, including all documentation, shall then be delivered to the FAA at least 90 days prior to delivery of the ERDIRS equipment for installation. It shall be the responsibility of the contractor to ensure proper interfacing of the ERDIRS with the interface modification installed in the DG cabinets.

3.2.1.1.1.2 Display Data.

The display computer refresh subsystem refreshes each PVD via its associated DCVG at a nominal 55 Hz rate. Each of these refresh cycles or frames contains the entire display pattern.

Each DCVG data word in a display pattern consists of four 16-bit parallel bytes. Each byte is sent to the DCVG at a data rate of 4.444 Megabytes/second.

Data are transferred to each DCVG at this rate in groups or banks of one to four 64-bit words during each access time with the VAD being active during the first byte of the first word of each bank.

3.2.1.1.1.3 Sampling.

In order to reduce the amount of data to be recorded, a sampling technique shall be used. A complete refresh frame from each DCVG shall be sampled in real time, stored temporarily in a buffer memory, and transmitted to the recorder at the appropriate data rate. The size of the buffer memory shall be at least 2048 words. The system shall sample multiple DCVG's in a cyclical sequence with the cycle period being variable and dependent upon the amount of data sampled. The Recording Subsystem shall be capable of sampling the data from each PVD within a time interval of 2 seconds or less. During the sample interval, should the maximum capacity of the Record Interface Equipment memory be reached, the sampled frame shall be truncated by generating and recording an artificial EOD word. This word is used only by the refresh elements which send data to the DCVG to determine the end of a refresh cycle. Since the DCVG does not interpret the EOD word as the last word of a frame, this word must be sent as the last word of a multiword transfer. The design of the Record and Playback Interface Equipment shall be such that, if an EOD word is forced in order to truncate a frame, multiple EOD words shall be used

to fill all unused word positions in the last data transfer to the DCVG during playback. When a frame has been truncated, information shall also be recorded to advise during playback that data has been truncated.

3.2.1.1.1.4 Reconfiguration.

The ERDIRS shall not sample the input of any DCVG that is not in an on-line status. Therefore, reconfiguration signals available within each DGU shall be monitored. When a spare DGU or DCVG is activated, the data sent to the activated spare DCVG shall be recorded in place of the data being sent to the previously active DCVG. When this occurs, the data to the activated spare DCVG shall retain the same sector address label used for the previously active DCVG.

This will insure that the playback presentation will use the same data which was sent to a particular PVD whether it was originally processed by an active or spare DCVG. The sampling of display data shall resume automatically so that any interruption of the playback presentation shall not exceed the total of the time required for the on-line PVD to recover following reconfiguration plus one record sample period.

Information that a reconfiguration has occurred shall be recorded so that it may be used on playback to indicate which sector or sectors were reconfigured.

3.2.1.1.2 Recording Equipment.

The Recording Subsystem shall use high-density digital recorders with a read-after-write capability. The requirements common to all the recorders in the ERDIRS are specified in paragraph 3.2.3. The Training Recorder shall be used to replace a failed Operational Recorder in any emergency situation when the failed recorder requires extensive maintenance. Recorder requirements pertinent to the Recording Subsystem are specified in the following subparagraphs.

3.2.1.1.2.1 Switchover.

The Operational Recorders shall be paired and capable of operating in a sequential mode such that when the active recorder approaches end-of-tape, the standby recorder will start recording in sufficient time to preclude any loss of data. When the recorder reaches end-of-tape it shall rewind and remain in standby. This shall be accomplished automatically; however, the capability shall be provided to switchover by means of a manual intervention when required.

Should the on-line recorder fail or become inoperative while in the active state, automatic switchover shall occur and the alternate recorder shall continue recording. Should one of the paired recorders be unavailable or fail to go on-line, the active recorder, upon reaching end-of-tape, shall rewind and immediately proceed to record new data over the previously recorded data. Whenever the alternate recorder is unavailable for on-line utilization following either manual or automatic switchover, this information shall be provided to the ERDIRS Equipment Status and Alarm Panel and in turn to the SMMC so that action can be taken by maintenance personnel to minimize the loss of recorded data. Such action could include replacing the failed recorder with the Training Recorder. See status reporting requirements specified in paragraph 3.2.1.2.2.

3.2.1.1.3 Time Code.

A Coded Time Source (CTS) is available at each proposed ERDIRS site and will provide time code data for recording purposes. This time code shall be recorded on a single dedicated track and used for locating data during playback (reference paragraph 3.2.2.1.3.3) and synchronizing display data tapes and voice tapes (reference paragraph 3.2.2.1.3.4). The CTS generates an IRIG-E serial code, modified to use a 600 Hz carrier, and has an output impedance of 600 ohms. Further detailed information on the CTS is available in the instruction manual referenced in paragraph 2.2.3.

3.2.1.1.4 Auxiliary Recording

Three auxiliary high-density digital data tracks shall be provided on each recorder for future expansion purposes. These auxiliary tracks shall occupy the same track positions on all machines utilized in the ERDIRS.

3.2.1.2 Operational Monitoring.

The Recording Subsystem shall allow an operator to visually monitor the sampled display data at both the inputs and outputs of the Recorders. In addition, status and alarm information concerning the operation of the subsystem shall be provided for maintenance purposes.

3.2.1.2.1 Display Data Monitoring Equipment.

The Playback Interface Equipment, as described in paragraph 3.2.2.1.1, shall be used to perform display data monitoring. It shall be capable of interfacing both the input and output of all the Recorders in the Recording Subsystem with a single dedicated DCVG which will be used to drive both the SMMC See-All PVD and the Maintenance PVD. Although the requirement is to monitor display data to any operational or Training PVD (one at a time), the data must be displayable on either one or both monitor PVD's. At each of these positions, an operator shall have the ability to select for display either the data normally provided to that PVD by the display computer (normal mode), or the display data being collected and recorded by the ERDIRS (ERDIRS mode). At the SMMC See-All PVD this will be accomplished using the Normal/ERDIRS Selector; at the Maintenance PVD this will be accomplished by means of connecting the existing display cable to a plug (contractor supplied) on the ERDIRS equipment when ERDIRS display data is desired. When either PVD is monitoring ERDIRS data, the operator shall be able to select at either position the data being sampled from any of the on-line PVD's either before or after the data has been recorded. However, if both positions are monitoring ERDIRS display data, they must both be monitoring the same data since only one playback DCVG is used. In this situation the SMMC See-All PVD shall have priority when selecting data to be monitored. If priority control is desired at the Maintenance PVD position, the SMMC See-All PVD must be switched back to the normal mode. All necessary electronic circuitry located at the SMMC See-All and Maintenance PVD positions shall be packaged in a unit external to the PVD and easily attached and detached to ensure ease of replacement of PVD's for maintenance purposes. The design of this external unit shall be submitted to the Government for approval. This monitoring function is a visual check for obvious degradation of the data by either the Record Interface Equipment or the Recorder. A more comprehensive check of the data shall be made via the status and alarm indicators described in paragraph 3.2.1.2.2.1.

Besides providing the capability to view sampled display data on a real-time basis, the monitoring equipment shall also provide the capability to freeze (i.e., hold and refresh for an indefinite time period) a single frame of data for detailed review. When the freeze function is terminated, the monitoring equipment will continue to refresh the display with the frozen frame until it has acquired a complete new frame for the display being monitored. At this point, the real-time monitoring operation will resume. This freeze function is similar to that required in the Playback Subsystem as discussed in paragraph 3.2.2.1.3.2.

3.2.1.2.1.1 Monitoring Controls.

Controls shall include as a minimum a freeze control switch, a normal/ERDIRS mode select switch, switches for addressing a specific air traffic control sector to be displayed and for designating the source of the display data — either the input or output of an Operational or Training Recorder. Also any reset controls necessary to initialize the Plackback Interface Equipment or DCVG shall be provided. Visual indications of all selections shall be provided at the location of the controls. Selection of any on-line PVD to be monitored shall be done using air traffic control sector numbers.

There shall be a set of controls/indicators for each of the two PVD positions, one for the SMMC See-All PVD and one for the Maintenance PVD. These controls/indicators shall be contained in a unit that may be mounted adjacent to, or on the PVD.

3.2.1.2.2 Status Monitoring Equipment.

The equipment design shall include all features necessary to monitor the performance of the Recording Subsystem and to derive detailed status, alarm, and failure information. This information shall be displayed on a panel or panels located with the Recording Subsystem equipment in the display computer equipment room. Also based upon this detailed data, general system status information shall be derived for each major piece of equipment and displayed at a panel located with the Recording Subsystem equipment and at the SMMC which is located in the air traffic control room. Further detailed information on the SMMC is contained in the instruction manuals referenced in paragraph 2.2.3.

All indicators used shall be replaceable from the front without requiring the use of special tools. An indicator test switch shall be provided on each panel as a means of detecting indicator failures. Each audible alarm shall be tested in a similar manner.

3.2.1.2.2.1 Equipment Room Indicators.

Detailed equipment status information from the Record Interface Equipment, the Recorders, and the Playback Interface Equipment shall be provided via indicators on a panel or panels located in a rack adjacent to the recorders. Status information from the Training Recorder shall be displayed at this panel only when in the record mode. When not in the record mode, this panel shall indicate a "not recording" status.

Detailed equipment status information shall be provided using both momentary and resettable latching indicators. The momentary indicators shall be used to show

current operation of the equipments and errors on a real-time basis. The resettable latching indicators shall be used to show errors that may otherwise be missed because of operator absence or because they may occur too rapidly to be seen. Certain errors that occur as a part of the detailed equipment status information shall be counted per unit time and the various counts shall be weighted and summed together on an individual equipment basis to generate equipment error rate figures. Each error rate figure shall be compared with two threshold values to determine whether the equipment is in a degraded or failure state. The two threshold limits shall be designated Limit 1, the minimum limit, and Limit 2. If the equipment error rate figure lies below Limit 1, the equipment shall be in the operational state; if it lies between Limits 1 and 2, the equipment shall be in the degraded state; if it lies above Limit 2, the equipment will be in the failed state. These limits shall be adjustable so that optimum values may be established and manually setable by maintenance personnel. The weighting factors for each type of error shall also be adjustable.

The detection of any hard failure within the equipment shall be used to declare a failed or degraded state, dependent on the impact on the associated equipment. This system status information shall be made available via indicators and alarms on a separate panel in the equipment room and remoted to the SMMC position as specified in paragraph 3.2.1.2.2.2.

As a minimum, the following conditions shall be monitored and indicators provided:

a. Record Interface Equipment.

1. Parity Error. Parity shall be generated on a byte basis at the input and compared at the output. Errors shall be detected and indicated. The generated input parity shall also be recorded along with the display data to be used by the Playback Interface Equipment. For purposes of developing system status information, the number of errors shall be counted per unit time and weighted.

2. Memory Overflow. This shall be detected and indicated whenever the memory capacity has been exceeded while storing a given frame of data. When this conditions occurs, an EOD shall be forced so as to truncate the refresh operation on playback. For purposes of developing system status information, the number of consecutive overflows per sample period shall be counted per unit time and weighted.

3. Input Status. This information shall be provided by detecting that data from each DGU interface are being received by the Record Interface Equipment. Indicators shall light when data are being received. A "no data" condition shall exist from an individual DGU interface whenever data are not received for the display being sampled during any 20-millisecond time period.

4. Input Error. An input error condition shall exist whenever during a 20-millisecond time period data are being received by the Record Interface Equipment and are not being processed. For purposes of developing system status information, the number of input error conditions shall be counted per unit time and weighted.

5. Output Status. This information shall be provided by detecting that data are available at the output of the Record Interface Equipment for transmission to the Recorders. Indicators shall light when data are available at the output. A "no data" condition shall exist whenever during a 20-millisecond time period data are not available at the output.

6. Output Error. An output error shall exist whenever one of the following conditions occur during a 20-millisecond time period: (1) If the status of the input section of the Record Interface Equipment implies that data should be available at the output, but no data are available, an output error condition shall exist; (2) If data are available at the output but are not being transmitted to the Recorders, an output error condition shall exist. For purposes of developing system status information, the number of output error conditions shall be counted per unit time and weighted.

7. Clock Failure. As a minimum, all clocks which are critical to the operation of the Record Interface Equipment shall be monitored and any intermittent or continuous clock failure shall be detected and indicated. An intermittent clock failure shall exist whenever 1 percent or less of the total number of clock cycles in a 100-millisecond time period are abnormal. An abnormal clock cycle is one whose time period deviates from the nominal by ±10 percent. A continuous clock failure shall exist whenever more than 1 percent of the total number of clock cycles in a 100-millisecond time period are abnormal or whenever the time period between clock pulses exceeds 1 millisecond. For purposes of developing system status information, the number of errors shall be counted per unit time and weighted.

8. Power Supply Malfunction. Any out-of-tolerance condition of the power supplies shall be detected and indicated (i.e., overvoltage, undervoltage, overcurrent, thermal shutdown, etc.).

9. Over Temperature. Any over temperature condition within the equipment cabinet where the temperature exceeds 122° F (50° C) shall be detected and indicated.

b. Recorders.

1. Parity Error. Parity shall be generated for each track of data as it is being recorded and this parity shall be compared at the output of the reproduced electronics using a read-after-write configuration. At least one parity bit shall be generated for each 512 bits recorded on a track. Detection of an error shall be indicated. For purposes of developing system status information, the number of errors shall be counted per unit time and weighted.

2. Deskew Error (if applicable). Failure of the recorder to align data bits properly on playback shall be detected and indicated. This operation shall be accomplished for each track using a read-after-write capability with the detection of errors being indicated. For purposes of developing system status information, the number of errors shall be counted per unit time.

3. Tape Breakage. The breakage of tape shall be detected and indicated.

4. Vacuum Loss (if applicable). The loss of vacuum used within the Recorder shall be detected and indicated.

5. Power Supply Modification. Any out-of-tolerance condition of the power supplies shall be detected and indicated (i.e., overvoltage, undervoltage, overcurrent, thermal shutdown, etc.).

6. Over Temperature. Any over temperature condition within the equipment cabinet where the temperature exceeds 122° F (50° C) shall be detected and indicated.

c. Playback Interface Equipment.

1. Parity Error. Parity generated on a byte basis at the input of the Record Interface Equipment shall be recorded with the data and compared at the input of the Playback Interface Equipment. In addition, parity generated on a byte basis at the input of the Playback Interface Equipment shall be compared at the output of the Playback Interface Equipment. Any errors shall be detected and indicated. For purposes of developing system status information, the number of errors shall be counted per unit time and weighted.

2. Memory Overflow. Overflow shall be detected and indicated whenever the memory capacity has been exceeded while storing a given frame of data. Asynchronous refreshing of the display shall also be indicated. For purposes of developing system status information, the number of overflows shall be counted per unit time and weighted.

3. Clock Failure. As a minimum, all clocks which are critical to the operation of the Playback Interface Equipment shall be monitored and any intermittent or continuous clock failure shall be detected and indicated. An intermittent clock failure shall exist whenever 1 percent or less of the total number of clock cycles in a 100-millisecond time period are abnormal. An abnormal clock cycle is one whose time period deviates from the nominal by ±10 percent. A continuous clock failure shall exist whenever more than 1 percent of the total number of clock cycles in a 100-millisecond time period are abnormal or whenever the time period between clock pulses exceeds 1 millisecond. For purposes of developing system status information, the number of errors shall be counted per unit time and weighted.

4. Power Supply Malfunction. Any out-of-tolerance condition of the power supplied shall be detected and indicated (i.e., overvoltage, overcurrent, thermal shutdown, etc.).

5. Over Temperature. An over temperature condition within the equipment cabinet where the temperature exceeds 122° F (50° C) shall be detected and indicated.

There shall be a group of indicators for each Operational Recorder, a group for the Record Interface Equipment, a group for the Playback Interface Equipment used for monitoring, and a group for the Training Recorder. Each group shall contain indicators for displaying the above listed error, status, and failure conditions plus indicators for displaying the three-system status states — operational, degraded, and failure. In addition when a failure state is detected, an audible

alarm shall be sounded. Whenever a change in state occurs, the appropriate indicator shall be blinked, halting only after an acknowledge button has been depressed. If the equipment is returned to the operational state from either the degraded or failure state before acknowledge occurs, the indicators shall continue to report both the previous state and the operational state so that the systems engineer will be aware that a change of state had occurred. The same shall be true if the subsystem goes from the failure to degraded state.

3.2.1.2.2.2 System Maintenance Monitor Console Indicators.

The three indicators for each equipment group, which will display system information (operational, degraded of failure) in the equipment room and as described in paragraph 3.2.1.2.2.1, shall be remoted to the SMMC located in the control room of the ARTCC. Separate independent controls used to acknowledge a change in status shall also be provided.

3.2.2 Playback Subsystem.

The functions of the Playback Subsystem are to play back operational and training display data and to duplicate tapes. These functions will be described in detail in the following subparagraphs.

3.2.2.1 Data Playback.

The capability shall exist to play back previously recorded display data including the ability to play back data from any two displays simultaneously where the data are contained on either one or two tapes. This playback function shall be accomplished using a two-channel Playback Interface Equipment, two dedicated playback DCVG's, two designated playback PVD's, and one or two reproducers, depending upon whether one or two tapes are to be played back simultaneously. The Playback Reproducer and the reproducer portion of the Training Recorder will be utilized when the desired display data are contained on two tapes. Simultaneous playback on two playback PVD's is required, including the capability to time synchronize a voice data tape with either one or two display data tapes or to time synchronize two display data tapes together.

Controls and indicators similar to those used for the monitoring function in the Record Subsystem (paragraph 3.2.1.2.1.1) shall be provided as applicable in the Playback Subsystem. In addition, controls necessary to operate two reproducers simultaneously and controls necessary to provide the time synchronization capability shall also be provided at each of the two playback PVD positions.

3.2.2.1.1 Playback Interface Equipment.

This equipment shall provide the interface between the digital reproducers and the DCVG's. It shall store each frame of data as it is received from tape and refresh the PVD via the DCVG at a nominal rate of 55.025 frames-per-second, ±0.05 percent. The update rate shall be nominally the same as the sample rate of the Record Interface Equipment. The Playback Interface Equipment shall use the sync word generated by the Record Interface Equipment to delimit groups of data and shall use the sector address label to select the appropriate data to be displayed. Hardware logic is preferred but a processor with firmware logic will be considered.

All necessary interfacing signals shall be generated by the Playback Interface Equipment. The interface shall generate the 4.4 MHz clock necessary to clock data into the DCVG and a variable blink clock required by the DCVG to provide blinking data. The blink clock shall have the capability of being manually adjusted by an operator in order to match the blink rate associated with the host display computer. The interface shall also supply the words per blank (W/B) signals which shall be set at one W/B regardless of the setting of the host display computer. The VAD, master reset, and DCVG parity error signals shall also be provided.

Power supplies within the interface equipment shall power both the Playback Interface Equipment and the associated DCVG's.

3.2.2.1.2 Digital Reproducer Equipment.

This equipment shall consist of two reproducers capable of playing back previously recorded display data. The primary reproducer for operational display data shall be a stand-alone unit (Playback Reproducer) that is identical to all other recorders used in the ERDIRS except it shall have no record electronics or record heads. It shall be as described in paragraph 3.2.3 with the exception of the record function which is not required. Should the Playback Reproducer be unavailable or if a two-reproducer configuration is required, the reproducer portion of the Training Recorder shall be used. This unit is further described in paragraph 3.2.3. Normally, training display data will be played back on the Training Recorder. However, if this Recorder is being used to record a training mission or is otherwise unavailable, the Playback Reproducer shall be used.

3.2.2.1.3 Playback Modes.

The following subparagraphs describe the various configurations, playback speeds, and time synchronization requirements for playing back display data.

3.2.2.1.3.1 Configuration.

The normal configuration used by the Playback Subsystem to play back operational display data from one operational display tape to either one or two playback PVD's simultaneously shall consist of the Playback Reproducer, the two-channel Playback Interface Equipment, and the two designated playback DCVG's/PVD's. Should the Playback Reproducer be unavailable, an alternate configuration utilizing the reproducer portion of the Training Recorder shall be possible. If the desired operational display data should be contained on two separate tapes (data from one PVD on one tape and data from a second PVD on another tape), the Playback Subsystem shall use both the Playback Reproducer and the reproducer portion of the Training Recorder and shall time synchronize the simultaneous playback of these two data tapes. In the two-reproducer configuration, it shall be possible to select independently from either playback PVD, data from either reproducer. In addition, it shall also be possible to play back display data independently from each reproducer to a playback PVD, without using time synchronization and without causing interference between the two independent playback configurations.

By means of switch control from the two playback PVD positions, either of the two reproducers may be selected as the playback data source. The operator at each of these two positions shall also have the ability to place the PVD in the normal mode in order to participate in a training mission and view training display data

prior to being recorded or to place it in the ERDIRS mode in order to view the recorded training display data. This mode selection capability shall be accomplished independently from either position so that either a one or two playback PVD configuration may be established.

3.2.2.1.3.2 Playback Speeds/Freeze.

When playing back previously recorded display data, there shall be two playback speeds and a freeze capability. These shall be available to the operator via control switches at each playback PVD. The two playback speeds shall be as described below:

NORMAL SPEED - This would be the same speed at which the data was recorded and would be used for normal playback.

TWICE SPEED - This would be twice the speed at which the data was recorded and would be utilized when a quick review via a fast update is desired.

Speed selection controls at either position will affect the reproducer selected from that position. When the same reproducer is selected at both positions, a lock-out feature will allow the speed controls at either position to control the speed of the reproducer. When a different reproducer has been selected from each position, the speed controls will only affect the reproducer selected.

A freeze capability shall be provided which shall refresh for an indefinite time period a single frame of data. When a single PVD is being used for play back, activating the freeze control shall result in the Playback Interface Equipment freezing the current frame being used to refresh the PVD. At the same time, the selected reproducer will halt. When released from the freeze condition, the reproducer shall start and the Playback Interface Equipment shall proceed to operate in a normal playback mode. However, no new data shall be displayed until a complete frame is available. When two playback PVD's are being utilized and both have selected the same reproducer and when the freeze control is activated from either PVD, the data on that playback PVD shall freeze while the reproducer shall continue to run and send data for the second playback PVD. When the freeze control at both positions is activated, the data on both PVD's shall freeze and the reproducer will halt. Deactivating the freeze control from either position shall result in the reproducer starting and updating the one playback PVD. The second playback PVD will remain in the freeze condition until the freeze control at that position is deactivated. Should a separate reproducer be selected from each of the two playback PVD positions, the freeze controls shall operate independently.

3.2.2.1.3.3 High-Speed Search.

Both the Playback Reproducer and the Training Recorder shall have a high-speed search capability. It shall be possible to select, either from the playback PVD position or from the reproducer, a desired time in hours and minutes, and proceed to start a high-3peed search at a minimum of 240 inches per second. The Reproducer shall automatically search the tape and stop at the desired time.

3.2.2.1.3.4 Time Synchronization Unit.

As specified in paragraph 3.2.1.1.3, during the recording of display data, a time code shall be recorded on a single dedicated recorder track. On playback, this time code shall be used to locate specific time periods on tape via high speed search and to enable the Playback Subsystem through the use of a Time Synchronization Unit to synchronize multiple tapes during playback to within a maximum of one-half second of each other.

There are three configurations where time synchronization of tapes shall be required: (1) synchronizing one display data tape with a voice data tape, (2) synchronizing two display data tapes with a voice tape, and (3) synchronizing two display data tapes. Whenever synchronization with a voice tape is required, the Voice Reproducer shall act as the master unit. The Voice Reproducer is existing government-furnished equipment; information concerning this equipment is available from the FAA.

3.2.2.1.3.4.1 Time Code Reader.

As a part of the time synchronization function the contractor shall provide Time Code Readers that are compatible with the recording equipment. These shall be capable of reading and displaying the time code (reference paragraph 3.2.1.1.3) from the Playback Reproducer, Training Recorder and Voice Reproducer at all forward and reverse tape speeds, and shall provide sufficient data to the Time Synchronization Unit for proper operation.

3.2.2.1.4 Operator Controls and Indicators.

As a minimum, the playback controls shall include the normal/ERDIRS select control, sector select controls, reproducer select controls, start/stop controls, speed controls, freeze controls, time synchronization controls, and reset controls. In addition, a master freeze control shall be provided to perform a freeze operation on both displays simultaneously. This control shall also provide the capability of releasing both displays from the freeze mode simultaneously, even if they were placed in the freeze mode independently.

All controls and indicators shall be provided at both of the designated playback PVD positions and shall be physically contained in units similar to those used in the display data monitoring equipment as described in paragraphs 3.2.1.2.1 and 3.2.1.2.1.1.

The Start/Stop, Speed and Rewind Controls shall be paralleled from the Training Recorder and Playback Reproducer to both playback positions with no priority. An end-of-tape (EOT) interlock shall be provided to prevent an operator at a remote position from exceeding the EOT limits while controlling either recorder. In addition, whenever the Training Recorder is used to spare a failed operational recorder, the above recorder remote controls shall be locked out, thus preventing any inadvertent interference during a recording mission. Using the time synchronization control, the operator at each position shall have the option of switching control of the recorders from the playback controls, located at the playback PVD position, to the Time Synchronization Unit. The initiating operator shall be capable of regaining control at any time, but it shall not be possible for the other remote position to control the Time Synchronization Unit once it is under

control of the first operator. The Time Synchronication Unit, the Playback Reproducer, and Training Recorder shall be independently controllable from either operator position on a first-come, first-serve basis with an indicator showing which units are being controlled at which position and a lockout feature to prevent inadvertent interference. Lockout shall exist until the operation is complete or until control is relinquished.

In conjunction with the above controls, as a minimum, the following indicators shall also be provided:

1. Normal/ERDIRS mode
2. Selected sector
3. Selected reproducer
4. Reproducer tape speed and direction
5. End of tape indicator
6. Freeze mode selected
7. Selected sector has been reconfigured. Indicate operating on spare DCVG.
8. Data refreshed asynchronously
9. In time-synchronized condition
10. Time code readout
11. Viewing Record Interface Equipment truncated data
12. System status information on Playback Subsystem
13. Rewind mode

3.2.2.2 Playback Monitoring.

The capability shall be provided to monitor the operation of the equipment used to play back display data. This monitoring shall be accomplished using status and alarm indicators similar to those used in the Record Subsystem to monitor the record operation (paragraphs 3.2.1.2.2 and 3.2.1.2.2.1).

3.2.2.2.1 Status Monitoring Equipment.

The equipment design shall include all features necessary to monitor the performance of the major units of the Playback Subsystem and to derive detailed status, alarm, and failure information. This information shall be displayed on a panel or panels located with the major units of the Subsystem. Status information derived from the Training Recorder during either the record or playback mode of operation shall be displayed at this panel.

Utilizing the detailed information, system status information shall be derived and displayed at the status panel and an audible alarm sounded when degraded or failure states are detected (reference paragraph 3.2.1.2.2.1).

All indicators used shall be replaceable from the front without requiring the use of special tools. An indicator test switch shall be provided on each panel as a means of detecting indicator failures. Each audible alarm shall be tested in a similar manner.

3.2.2.2.1.1 Playback Equipment Indicators.

Status, alarm, and failure information from the Playback Reproducer, Training Recorder, and Playback Interface Equipment shall be provided via indicators on a panel located with the playback equipment. The same conditions described in paragraph 3.2.1.2.2., and as applicable to the playback equipment shall be monitored and indicators provided.

3.2.2.3 Tape Duplication.

The duplication of tape (display data and time code) shall be accomplished the stand-alone Playback Reproducer as the playback unit and the Training Recorder as the recording unit. Duplication shall be performed at either normal speed, twice speed, or at a high speed of no less than 120 inches per second. In addition to the normal duplication of display data tapes, the capability shall exist to time synchronize the Playback Reproducer to a government furnished Voice Reproducer and to record, using the Training Recorder, a minimum of two voice channels from the Voice Reproducer. This duplication of voice data shall be accomplished simultaneously with the duplication of display data with edge track, used for the voice data. Both the Training Recorder and the Playback Reproducer shall be capable of playing back duplicated tapes containing these voice channels.

3.2.3 Digital Recorder Requirements.

The Recording Subsystem shall use high density digital magnetic tape recorders with the capability of accurately recording up to 33 kilobits per inch of tape per track. The Playback Reproducer used in the Playback Subsystem shall also be a high density unit, however, no record electronics or record heads shall be included in this unit.

Track configuration and other technical parameters shall be in accordance with Inter-Range Instrumentation Group Standards 106-80 and 118-75. These recorders shall be off-the-shelf equipment and shall be capable of meeting the requirements of this specification without major modification.

It is desirable that the transport and all electronics be contained in a single equipment cabinet. If more than a single cabinet is required, each recorder shall be physically independent so that there are no shared cabinets.

There shall be no onboard erase feature incorporated in any of the recorders or the reproducer.

Ease of maintenance, including a minimum of adjustments, and preventative maintenance not to exceed an average of 1.5 hours per recorder per week is required.

3.2.3.1 Capacity.

Each recorder shall have the capacity to record all the data being provided to a minimum of 72 PVD's for a minimum of 4 hours using a single 9,200-foot reel of 1-inch-wide, 1-mil thick tape (reference paragraphs 3.2.1.1.1.3).

All digital data tracks shall be capable of recording up to 33 kilobits per inch of tape per track of serial or parallel formatted data. This total shall include all user and overhead bits. A separate track, intended for time code, shall be provided. The three auxiliary data tracks (reference paragraph 3.2.1.1.4) shall be digital tracks with the same bit packing density and shall be independent of those digital tracks used to record the display data. The auxiliary tracks shall also have the capability of recording at an independent clock rate.

3.2.3.2 Transport.

The tape transport utilized in the recorders and the reproducer shall be an off-the-shelf assembly. It shall contain all the necessary mechanical electrical and electronic hardware for proper tape control. It shall also be capable of using tape reels up to 15 inches in diameter.

3.2.3.2.1 Tape Guidance.

The guidance portion of the tape transport shall be high quality hardware capable of providing a constant tape tension at a given tape speed. It shall ensure proper tape packing at all forward and reverse speeds and eliminate stretching, poor packing, and/or looping of tape.

Tape guides shall be such that differences between machines will not adversely affect the playback of a tape on a machine other than the one on which it was recorded.

3.2.3.2.2 Servo.

The servo systems utilized to determine capstan motor speed and to control reel motors shall use electronic feedback techniques and the capstan(s) shall be crystal controlled with the capability of using an external servo reference for time code synchronization.

Measured in accordance with IRIG Standard 118-75, the following parameters for Flutter, Dynamic Skew (ITDE), and Time Base Error (TBE) shall be maintained as a minimum when using the internal crystal reference:

Tape Speed (in/sec)	Flutter (pk to pk) (%)	ITDE* (Outside Tracks-0 to pk) (μsec)	TBE** (0 to pk) (μsec)
120	0.13	±0.8	±0.4
15	0.20	±6.4	±1.0
7.5	0.25	±12.0	±1.5
3.75	0.30	±24.0	±3.0

*Interchannel Time Displacement Error
**Time Base Error

3.2.3.2.3 Controls.

The transport shall have all the controls necessary for proper operation of the recorder or reproducer as detailed in paragraph 3.2.2.1.4. In addition, a remote control feature, with the capability of accepting control signals from multiple sources, shall exist so that the Playback Reproducer and the Training Recorder used in the Playback Subsystem may be remotely controlled by the operator at either of the two designated playback PVD positions or the Time Sync Unit as discussed in paragraph 3.2.2.1.4.

3.2.3.2.4 Footage Counter.

An electronic tape footage counter shall be provided on the front panel of each tape transport. It shall be a five-digit display with the display blanked when the recorder power is off; however, with power off, the counter shall have count retention for a minimum of 100 hours. The counter shall indicate the amount of tape utilized to the nearest foot. The counter shall be manually resettable but the reset button or switch shall be protected against accidental activation. The recorders shall be capable of operating in the shuttle mode (cycling tape between two preset footage limits automatically) on playback with the ability to set shuttle limits manually via the footage counter.

A cumulative footage counter with a seven-digit display shall also be provided which will count the total amount of tape crossing the heads in 10-foot increments in either direction and at all speeds. It shall have an indefinite count retention when the recorder line power is on and a count retention of at least 30 days with line power off. The cumulative footage counter display need not be visible from the front panel of the recorder.

3.2.3.3 Electronics.

The electronics shall be of solid state modular design.

All digital data channels shall use a self-clocking code. Error detection signals shall be generated on a per track basis and as a minimum shall consist of parity and, if parallel data, failure to deskew properly. Parity generation shall take place at the recorder input logic and shall consist of checking for odd parity every 512 (maximum) user bits and generating the appropriate bit (if odd, add a "0," if even, add a "1"). Parity checking shall occur at appropriate points thereafter.

As a minimum, parity errors, deskew errors, power failure, tape breakage, vacuum loss (if applicable), and any other condition that could adversely affect the recording of data shall be electronically detected and an alarm indicator set on the recorder. In addition, these alarm conditions shall be provided to the status and alarm monitoring equipment in the equipment room (reference paragraph 3.2.1.2.2.1). An audible alarm on the recorder shall be provided for catastrophic failures; i.e., tape breakage, vacuum loss, etc.

3.2.3.4 Packing Density.

The packing density (number of bits per inch of tape per track) used, including all data and overhead bits, shall not exceed the currently established industry

standard of 33 kilobits per inch per track unless it can be shown to be a part of a manufacturers published specification standard in existence at least 6 months prior to the request for proposals.

3.2.3.5 Error Rate.

The error rate on all digital tracks, determined during an off-line test, shall not exceed 1 bit error in 10^6 user data bits (excluding overhead bits) per track when measured and averaged over a randomly selected 100-foot section of tape (reference paragraph 3.2.3.8) and when operated at all record and playback speeds specified by the contractor as meeting the requirements of this specification for recording and reproducing digital data.

3.2.3.6 Reliability.

The reliability/maintainability requirements for the recorder shall be as specified in paragraph 3.4.1.

3.2.3.7 Head Life.

The magnetic heads shall be unconditionally guaranteed to have a life sufficiency to permit passage of at least 23 million feet of tape over the heads (in either direction and at all stated speeds) as measured using the cumulative footage counter (specified in paragraph 3.2.3.2.4) before replacement of heads becomes necessary.

The warranty on each set of heads shall be in effect for 2 years following the delivery.

3.2.3.8 Tape.

The error rate as specified in paragraph 3.2.3.5 shall be met using Ampex 795/797 tape or equivalent. The tape used shall not exceed 1 inch in width with a nominal thickness of 1 mil.

3.3 DESIGN AND CONSTRUCTION.

3.3.1 General Requirements.

The ERDIRS shall be designed and constructed to provide high operational availability (reference paragraph 3.4.1) and good accessibility (per MIL-STD-454, Requirement 36) for maintenance and repair. The hardware shall also be designed so that all alignments, adjustments, and maintenance can be performed by one technician. No replaceable module, subassembly, or assembly shall weigh over 50 pounds.

All ERDIRS equipment shall conform to the requirements of FAA-G-2100 and subsidiary applicable documents referenced therein except for off-the-shelf equipment. Each item of off-the-shelf equipment shall conform to those design and quality standards established by the manufacturer (in effect on the closing date of the bid proposals) and all other requirements of this specification.

3.3.1.1 Solid-State Design.

The contractor shall design the circuitry of the ERDIRS using semiconductor devices in accordance with FAA-G-2100/3 and micro-electronics (integrated circuits) in accordance with FAA-G-2100/5. Off-the-shelf equipment shall not be required to meet paragraph 5 - 3.1(b) of FAA-G-2100/5.

3.3.1.2 Printed Wiring.

Single and multilayer printed circuit boards shall be fabricated in accordance with FAA-G-2100/4b. Adjustments required for alignment shall be held to a minimum; however, when required, such adjustments shall be made on the circuit board. Where test points (FAA-G-2100/1) are provided on the circuit board (reference paragraph 3.6.1.1.2) they shall be easily accessible. No sockets shall be used except where high failure rate or high cost items exist. Test extender boards shall be furnished to interface printed circuit boards with external test equipment.

3.3.1.3 Controls and Alarms.

Controls, calibration adjustments, and alarms shall be provided on each equipment or group of equipments to permit maintaining peak system performance, to monitor system performance, and to indicate malfunctions. All controls and adjustments required to operate the equipment shall be readily accessible from the front without the use of extenders or other temporary means of access. All alarm signals shall be capable of energizing an audible alarm via suitable drivers.

3.3.1.4 Environmental Service Conditions.

The equipment herein shall operate (power on) in an attended facility in accordance with the requirements of this specification under the following service conditions:

1. Elevation: 0 to 10,000 feet above sea level
2. Temperature: 50° to 122° F (10° to 50° C)
3. Humidity: 30 to 70 percent relative humidity

3.3.2 Electrical Requirements.

The following subparagraphs cite electrical requirements of the ERDIRS equipment.

3.3.2.1 Electrical Service Conditions.

Design center values and ranges of the primary power source shall be as follows:

AC Line Parameter Design Center	Service Condition Range
120 volts	102 - 138 volts
208 volts	177 - 239 volts
60 Hertz line frequency	57 - 63 Hertz

3.3.2.2 Electrical Service Conditions; Transient State.

All ERDIRS equipment, including any off-the-shelf equipment, shall perform its specified function in accordance with the requirements of paragraphs 1-3.3.4 and 1-3.3.5 of FAA-G-2100/1 pertaining to AC power source transients. No false output signals shall be generated by transients within the defined limits or by in-rush currents caused by the ERDIRS.

3.3.2.2.1 Startup Surges.

The peak in-rush current during start-up shall not exceed five times the normal operating current. The duration of the in-rush current shall not exceed 8 seconds where the duration is defined as the time from input power application to the time at which the power returns to its steady state.

3.3.2.3 Electrical Design.

Electrical design shall conform to the requirements of FAA-G-2100 parts 1, 3, 4, and 5 with exceptions or modifications as contained herein. Energy conservation practices shall be used in the electrical design of the system in order to minimize total electrical power consumption. Twin convenience outlets, in accordance with paragraph 1-3.6.4 of FAA-G-2100/1, shall be provided on the front and rear of each cabinet for 120 vac test equipment, soldering tools, etc. These outlets shall be powered from an electrically separate power cable brought out of the cabinet for connection to a separate noncritical AC power source. The ground terminal of all convenience outlets shall be electrically isolated from the equipment cabinet and connected by a green insulated conductor to the ground terminal in the power distribution panel serving the outlet.

3.3.2.4 Circuit Isolation.

All circuits shall be designed so that no damage will occur when the equipment is operated with the controls and maintenance adjustments set to any possible configuration of settings. No failure shall occur due to activation of any controls.

3.3.2.5 Grounding.

A uniform system grounding design shall be used for the ERDIRS. This design shall be submitted as a part of the technical proposal with the contractor being responsible for interfacing the ERDIRS grounding with the grounding system used in an ARTCC. The grounding system design must ensure the safety of all personnel when operating or testing the ERDIRS and the design must be compatible with other equipment with which the system will interface.

For all contractor developed equipment which is not off-the-shelf equipment, the grounding design shall be in accordance with the guidelines provided in FAA-STD-020 (paragraphs 4 and 5). When equipments are off-the-shelf they shall be compatible with the newly developed equipment and shall be included in the overall grounding design.

3.3.2.6 Conducted and Radiated Interference.

The equipment specified herein shall satisfy the basic requirements for interference and susceptability as provided in FAA-STD-020 (paragraph 6) or MIL-STD-461. Should any proposed equipment have been built to comply with a military interference control specification other than MIL-STD-461 (e.g., MIL-I-16910), the FAA will accept that specification in lieu of FAA-STD-020 or MIL-STD-461 provided requirements are equal and equivalent.

3.3.2.7 Power Supplies.

All power supplies shall be self-protecting, such that, without the use of fuses, circuit breakers, or other protective devices, a continuous short across the power supply output will not damage circuit components and the output voltage will return to normal upon removal of the short circuit. The electronic short circuit protection circuit shall allow capacitive loads to be switched on without causing any circuit protection devices to be falsely triggered or including any other undesired side effects. All power supplies shall also be equipped with over-voltage protection and shall be set so as to preclude any damage to the device it powers.

All power supplies shall contain front panel test points where possible for measuring the various voltage outputs and their corresponding load currents. Front panel AC circuit breakers that can also be used as ON-OFF switches shall also be provided.

In the critical Recording Subsystem redundancy shall be provided in the Record Interface Equipment power supplies. This redundancy shall be either a standby power supply or dual power supplies operating simultaneously with either one capable of automatically assuming the total load should the other fail. In the case of a standby power supply, there shall be no interruption of the logic operation when the standby supply is switched on line.

3.3.3 Mechanical Requirements.

The following subparagraphs cite mechanical requirements of the ERDIRS equipment.

3.3.3.1 Cabinet Construction.

The structural strength and rigidity of the cabinets shall be such that normal handling in loading, shipping, unloading, and setting into position for installation shall not result in any permanent set or deformation that would impair or interfere with the removal of units or components, ease of maintenance, operation of access doors, or ventilation. The structural strength and rigidity of all cabinets shall be independent of any strength or rigidity provided by access doors.

The design shall provide good accessibility for maintenance and repair or replacement of units or modules. With the exception of off-the-shelf equipment, each subassembly shall be removeable from the cabinets without requiring the partial or complete removal of any other subassembly. The cabinets shall be of high quality, sturdy material, and be accurately and carefully fabricated. All cabinet assemblies shall be designed with an anti-tilt feature so that it will not be necessary to bolt or fasten the equipment to the floor. A lockable dolly system

is required for all recorders while adjustable leveling pads shall be provided at each corner of all other cabinets. All access doors shall be mounted so that the cabinet doors may be removed and reinstalled easily.

Latches shall be provided to hold cabinet doors in the open position. Panels shall be adequately braced and of sufficiently small size and weight so as not to exceed 50 pounds (22.65 kilograms) in order to permit removal and replacement by one unassisted technician. Removal of units for maintenance or repair or interchanging of units shall not cause any deformation to the cabinet. If lifting devices, such as hooks or rings, are installed temporarily for convenience in handling, such devices shall be replaced by the contractor after removal with suitably painted cap bolts. All cables and wires, harnessed or single, shall be protected against chaffing, and such protection shall be independent of the individual wire or cable insulation jacket. All surfaces of items on the front of panels shall be at cabinet ground potential. Cabinets shall be designed for side-by-side installation with no open space between cabinets. Lights for general illumination of the cabinet interiors shall be provided behind the access doors. Such lights shall be adequately shielded to prevent any adverse effects due to electromagnetic interference. Lamps shall be easily accessible for replacement. The various units or modules mounted in each cabinet shall be accessible for servicing from either front or rear. These units shall be provided with slides where necessary to permit withdrawal for servicing. Where components or test points are only accessible from the bottom, a suitable tilt or hinge arrangement shall be provided to permit easy and comfortable accessibility. If any subassembly is partially removed for maintenance by use of slide or hinged devices, such partial removal shall not result in a drastic change in the center of gravity such that the cabinet becomes unstable. Except for off-the-shelf equipment, all cabinet cable entrances shall be as specified in the contract.

The overall design of the cabinets shall be subject to FAA approval.

3.3.3.1.1 Moisture Pockets.

The ERDIRS equipment design with respect to moisture pockets shall be in accordance with FAA-G-2100/1, paragraph 1-3.4.6.

3.3.3.1.2. Wiring Practices.

Except where otherwise specified herein, all equipment, with the exception of off-the-shelf equipment, shall meet requirements of FAA-G-2100/1, paragraph 1-3.10.

3.3.3.2 Cabinet Ventilation and Cooling.

Ventilation and cooling of all cabinets shall be in accordance with FAA-G-2100/1, paragraph 1-3.9. Each cabinet requiring forced ventilation shall contain its own blower system and shall have no external ducts. Ventilation air intake shall be from the bottom of the cabinet with input air filters being removable from the outside of the cabinet without the necessity of opening the cabinet doors.

Ventilation exhaust shall be at the top of the cabinet with outlets designed so that foreign objects dropped from above cannot enter the cabinet through exhaust outlet openings. The equipment shall not overheat or develop hot spots exceeding 122° F (50° C) with access door and plates open for servicing.

3.3.3.2.1 Overheat Warning.

A thermal warning device shall be provided in each separate cabinet to indicate when the temperature exceeds the maximum safe operating temperature of 122° F (50° C) within the cabinet. A warning indicator readily visible from the cabinet exterior shall be provided on the cabinet. In addition, the over temperature condition shall also be provided to a centralized status and alarm panel.

3.3.3.3 Module Removal and Insertion.

All equipment shall be designed to enable the removal and insertion of modules and printed circuit boards without causing any damage to the module, printed circuit board, or any other equipment external to the module or printed circuit board. Provisions shall be made so that a module or printed circuit board cannot be inadvertently inserted into the wrong module or board position or in the wrong orientation.

3.3.3.4 Cabling.

Cabling in general shall be provided in accordance with FAA-G-2100/1, paragraph 1-3.10.7.

The contractor shall furnish all inter- and intra-connecting cables and cable connectors required for factory and site testing, installation, operations, and maintenance of the ERDIRS. All cables shall be supplied with connectors installed. Any special tools and instructions required for installing cable connectors shall be furnished by the contractor as special test equipment.

3.3.3.4.1 Power Cables.

All AC power cables utilized in the ERDIRS shall be in accordance with FAA-G-2100/1b, paragraph 1-3.6. In addition, all AC power cables and wiring shall be separated from the signal circuits and installed in accordance with the most current National Electric Code.

3.3.3.5 Acoustic Levels.

Noise levels generated by the equipment shall not exceed those of Condition B, FAA-G-2100/1b, paragraph 1-3.5.11.

3.3.4 Parts and Materials.

Except for off-the-shelf equipment, parts and material utilized in the ERDIRS shall be in accordance with FAA-G-2100/1b, paragraphs 1-3.14, 1-3.15, and 1-3.16. Off-the-shelf equipment may employ components and materials not in accordance with FAA-G-2100/1b except that the interchangeability requirements of FAA-G-2100/1b, paragraph 1-3.14.3 shall apply.

3.3.4.1 Castings.

All castings shall be sound, dense, and free from casting defects. Casting material shall be of a hardness sufficient to preclude deformation from cabinet loading.

3.3.5 Finishes.

The finish of all exposed covers, doors, shelves, etc., shall be baked vinyl base paint. Accent panels shall be in complementing colors. The basic color and accent panel colors shall be as specified by the Contracting Officers from colors normally offered by the manufacturer. Preparation for finishing shall be in accordance with FAA-G-2100/1b, paragraph 1-3.8.

3.3.6 Personnel Safety.

All personnel protection requirements shall be in accordance with FAA-STD-020, paragraph 7, and FAA-G-2100/1, paragraph 1-3.5.

3.3.7 Human Engineering.

Human engineering design criteria and principles shall be applied in the system design in accordance with FAA-G-2100/1b, paragraph 1-3.4.13.

3.3.8 Markings.

All equipment, modules, test points, fuses, connectors, switches, etc., shall be properly identified as to nomenclature and signal name. With the exception of off-the-shelf equipment, all markings shall be in accordance with FAA-G-2100/1b, paragraph 1-3.12.

3.3.9 Name Plates.

Name plates on all equipment shall be provided in accordance with FAA-G-2100/1b, paragraph 1-3.13.

3.4 RELIABILITY AND MAINTAINABILITY.

The reliability and maintainability requirements for the ERDIRS, including the basic programs to be conducted by the contractor, are described in the following paragraphs:

3.4.1 Reliability/Maintainability Requirements.

The ERDIRS shall be designed to the meet the following reliability/maintainability requirements in accordance with MIL-STD-470:

1. System Requirements. The system Upper Test (Theta) Mean-Time-Between-Failures (MTBF) for the Recording Subsystem, consisting of the DGU/ERDIRS Interface printed circuit boards (A6), the Record Interface Equipment capable of channeling data from up to 72 displays, and the Operational Recorders shall be not less than 2,500 hours. The system specified Mean-Time-To-Repair (MTTR) for this same group of equipments within the Record Subsystem shall be 0.5 hour with a maximum tolerable of 0.75 hour.

2. Equipment Requirements.

a. Record Interface Equipment. The specified MTBF for the Record Interface Equipment, capable of channeling data from up to 72 displays, shall not be less than 2,500 hours. The specified MTTR of this equipment shall not exceed 0.5 hour with a maximum tolerable MTTR of 0.75 hour. No repairs shall exceed 2 hours.

b. High Density Digital Recorders. The specified MTBF for high density digital recorders shall not be less than 1,000 hours (does not include heads (reference paragraph 3.2.3.7)). The specified MTTR shall not exceed 1 hour with a maximum tolerable MTTR of 1.5 hours. No repairs shall exceed 3.5 hours.

c. Playback Interface Equipment. The specified MTBF for the Recording Subsystem single channel Playback Interface Equipment including all multiplex and control circuitry shall not be less than 2,500 hours. The specified MTTR for this equipment shall not exceed 0.5 hour with a maximum tolerable of 0.75 hour. No repairs shall exceed 2 hours.

d. High Density Digital Reproducer. The specified MTBF for the high density digital reproducer (Playback Reproducer) shall not be less than 1,250 hours. The specified MTTR shall not exceed 1 hour with a maximum tolerable of 1.5 hours. No repairs shall exceed 3.5 hours.

e. Playback Interface Equipment. The specified MTBF for the Playback Subsystem dual channel Playback Interface Equipment including all associated multiplex and control circuitry (excluding the time synchronization unit) shall not be less than 1,250 hours. The specified MTTR for this equipment shall not exceed 0.5 hour with a maximum tolerable of 0.75 hour. No repairs shall exceed 2 hours.

f. Time Synchronization Unit. The specified MTBF for the Time Synchronization Unit shall not be less than 2,500 hours. The specified MTTR for this equipment shall not exceed 0.5 hour with a maximum tolerable of 0.75 hour. No repairs shall exceed 2 hours.

3.4.2 Reliability Program.

The contractor shall develop a reliability program as described in paragraph 3.5.8. This program shall be implemented and the results documented in the Reliability and Maintainability Reports. The reliability program shall be performed by a clearly identifiable organizational element responsible for the effective execution of all reliability requirements and related efforts.

3.4.2.1 Program Tasks.

As a minimum the reliability program shall include the following tasks:

1. Reliability Modeling. A reliability model shall be developed for the ERDIRS. The model shall be of sufficient detail to identify critical paths or items whose failure would cause system failure or degraded operation. Graphical and mathematical techniques may be used to validate model accuracy.

2. Reliability Analysis. Reliability analyses and predictions shall be performed during both the preliminary and final design phase. These analyses shall

be detailed assessments of the design and conducted to a level sufficient to provide assurance that specified reliability criteria will be met. The methods of MIL-STD-756 shall be applied using definitions of MIL-STD-721 and failure rate data from MIL-HDBK-217C.

3. Reliability Testing and Demonstration. A Reliability Demonstration Test Plan in accordance with MIL-STD-781C shall be prepared and submitted to the FAA as a part of the Test Plan specified in paragraph 3.5.5. A one-time system reliability demonstration test shall be performed as specified in paragraph 4.3.2.2. Criteria for successful demonstration of the reliability requirement shall be defined and test results forwarded to the FAA.

4. Failure Reporting, Analysis, and Corrective Action. The contractor shall establish a system of failure reporting for both factory and on-site activity. The method of reporting shall be submitted for FAA approval. As a minimum, failures occuring from the time the design is frozen until the installed system has been accepted shall be reported. The contractor shall analyze each failure to ascertain its cause. Failure data reports to the component level including individual and trend analysis results shall be maintained in a central file to which the FAA shall have unlimited access. Monthly summaries of all failures and their status as to possible corrective action at the design level shall be submitted to the FAA.

3.4.3 Maintainability Program.

The contractor shall develop a maintainability program in accordance with MIL-STD-470. This program shall be detailed in a Plan as described in paragraph 3.5.9. This program shall be implemented and the results documented in Reliability and Maintainability Reports. The maintainability program shall be performed by a clearly identifiable organizational element responsible for the effective execution of all maintainability requirements and related efforts.

3.4.3.1 Program Tasks.

As a minimum, the maintainability program shall include the following tasks:

1. Maintainability Analysis. Maintainability analysis shall be performed in order to develop detailed maintainability design criteria. This analysis shall document trade-offs and the quantitative and qualitative requirements which result in the establishment of these design criteria. Whenever design trade-offs are performed, maintainability must receive appropriate consideration and the effect on the entire system as a result of any compromise of maintainability shall be evaluated, documented, and reflected in the analysis.

2. Maintainability Prediction. The contractor shall predict maintainability values for the system/equipment in accordance with a technique contained in MIL-STD-471. The technique to be utilized shall be specified by the contractor and approved by the FAA.

3. Data Collection, Analysis, and Corrective Action. The contractor shall establish a maintainability data collection system which shall be integrated as much as possible with similar reliability data collection requirements. Data shall be analyzed, summarized, and reported in the same manner as specified in paragraph 3.4.2.1.

4. Maintainability Testing and Demonstration. A maintainability demonstration test plan shall be prepared in accordance with MIL-STD-471 and submitted to the FAA as a part of the Test Plan specified in paragraph 3.5.5. The Plan shall include the scheduling, type, and objective of each test. An overall system maintainability demonstration test shall be performed in accordance with paragraph 4.3.2.3. Criteria for successful demonstration of the maintainability requirement shall be defined and the test results and summaries forwarded to the FAA.

3.5 DOCUMENTATION.

The contractor shall furnish all necessary services and materials to develop and deliver documentation in the quantities and at the times specified in the contract.

All documentation required by this specification shall be periodically updated to reflect the latest design level. In the event that documentation has been submitted to the Contracting Officer, appropriate revision pages in the same quantity as the earlier submission shall be provided, or the document shall be updated in total if 20 percent or more of the total pages in the document require updating.

All reproducibles furnished shall be of such quality as to permit the reproduction of every line and character on the reproduced copy.

All documentation initially produced or updated by the contractor shall show the contract number conspicuously displayed on each document, including drawings, to facilitate identification and association with the contract.

3.5.1 Instruction Manuals.

The contractor shall prepare a System Instruction Manual and Equipment Instruction Manuals in accordance with FAA-D-2494, Part I, and submit to the FAA Contracting Officer for approval. Subsequently, reproducible copies of these manuals shall be prepared in accordance with FAA-D-2494, Part II.

The System Instruction Manual shall be in sufficient detail to enable a thorough understanding of the ERDIRS; including theory, operation, and maintenance. The organization shall be such that system problems and problems concerning the interfaces shall be treated to facilitate system level troubleshooting. Each System Instruction Manual shall contain a section detailing the site configurations and any other information peculiar to any of the sites.

Equipment Instruction Manuals shall be provided on each of the primary equipments in the ERDIRS with sufficient information and detail, including circuit and timing diagrams, assembly drawings, illustrations, complete parts lists and operation, and service and adjustment instructions to enable complete operation, maintenance, and trouble-shooting down to the replaceable unit. Should the recorders or other units be standard off-the-shelf equipments, the manufacturers standard commericial instruction manual may be used, providing the manual generally meets the requirements of this paragraph. Each Equipment Instruction Manual shall contain a section discussing any modifications or options which are required for any of the sites.

3.5.2 Management Reports.

Management Reports, consisting of the following information as a minimum, shall be prepared and submitted to the FAA Contracting Officer on a monthly basis commencing 30 calendar days after contract award:

1. Part I, Program Status. This part shall include a narrative description of work progress during the reporting period.

2. Part II, Schedule. This part shall include an updated Program Evaluation Review Technique (PERT) diagram or current information relative to a computerized PERT network if a PERT computer program is used. The PERT diagram shall be supplemented by milestone charts where necessary. FAA-STD-007 shall be used as a guide for preparation of PERT diagrams.

3. Part III, Problem Areas. This part shall include a discussion of any special problem areas including solutions or progress toward solutions.

The initial management reports shall also include the below listed information; changes and updates to this information shall be furnished in succeeding reports:

1. An overall program plan to encompass design, fabrication, documentation, quality control, factory testing, delivery, installation, site testing, etc.

2. Original schedule PERT chart, including critical path analysis, identifying critical lead times as specified in 3 below.

3. A subcontractor schedule/listing with components to be supplied, including critical items, their lead times, and methods of management control of these subcontractors.

4. A detailed explanation of the control procedures intended to be exercised to assure expeditious completion of all activities related to the program and to provide timely updating of the performance schedule. Included shall be manpower resources by number and required skill for each phase identified in 1 above.

3.5.3 Site Preparation Report.

The contractor shall submit a Site Preparation Report to the FAA Contracting Officer not later than 150 days prior to the first scheduled installation date. This report shall contain general information applicable to all sites and specific information peculiar to each individual site. It will be used by the FAA to prepare the sites for installation of the contractor's equipment and to perform necessary services not required of the contractor. The report shall include, but not be limited to, the following:

1. Physical description of the equipment including size, weight, clearance factors, ventilation requirements, cable entry and exit features, etc.

2. Floor plan layout for equipment placement.

3. Power requirements. Information on type and size of power cabling to be used, type and size of required government-furnished power panels, etc.

4. Cable and duct requirements. Information on quantity and type of cabling to be used, where it goes, etc.

5. Grounding. System and equipment grounding requirements should be detailed.

6. Interface requirements. Information on all interfaces to existing FAA equipment including any required modifications.

7. Any other technical or general item that will be required in order to properly prepare a site for installation.

The contractor shall conduct on-site inspection to become familiar with the environment that will be encountered during installation. Government representation will be available during site inspections and access to the facilities will be arranged by the government. Available copies of drawings covering existing floor spaces will be provided to the contractor prior to these inspections. The objective is to provide the contractor with an opportunity to gather firsthand information to be used in the preparation of this report and the Installation Plan (reference paragraph 3.5.4). Coordination between the contractor and the government shall take place to determine optimum placement of all equipment, cables, etc., prior to completion of the Site Preparation Report.

3.5.4 Installation Plan.

The contractor shall submit an Installation Plan to the FAA Contracting Officer for approval 60 days prior to the first scheduled installation. This document shall contain general information applicable to all sites and specific information peculiar to each individual site. It will contain all necessary information required by trained engineers and technicians to correctly install the equipment and initiate its operation. As a minimum, the following information shall be included:

1. System diagram with short narrative description of hardware and its capabilities.

2. Floor plan layout for equipment placement.

3. Detailed physical description of the equipment including size, weight, clearance factors, ventilation requirements, cable entry and exit features, etc.

4. Step-by-step procedure for installing all equipment, cables, etc.

5. Any other technical or general information that will be required for installation should be discussed.

3.5.5 Test Plans.

The contractor shall submit to the FAA Contracting Officer for approval a Test Plan which outlines the acceptance testing program required to demonstrate compliance of the ERDIRS with the requirements of this specification. This Plan shall be submitted 120 days prior to the start of the tests. The FAA will review the Plan and provide comments to the contractor within 30 days after receipt. These tests shall

consist of factory testing, including preliminary tests, design qualification tests and production tests (as defined in FAA-G-2100/1), reliability tests, maintainability tests, and on-site testing. The Plan shall include, but not be limited to, the following:

1. The Plan shall provide an overview of all proposed test activities. The overview shall clearly identify all test activities required to demonstrate compliance with this specification, list tentative start and completion dates, define the elements and numbers of elements involved in each test activity, describe the objectives of each test activity, and list the test documentation required.

2. For each test activity identified in 1 above, the Plan shall provide general test requirements. The approved Plan shall be used by the contractor as a basis for developing the test procedures and data sheets.

3.5.6 Test Procedures.

The contractor shall submit preliminary test procedures to the FAA Contracting Officer not later than 90 days prior to start of tests for each test activity defined by the approved Test Plan. The test procedures shall be comprehensive documents including all details necessary to assure that test procedures and testing thereto will satisfactorily demonstrate equipment and system compliance with all functional, environmental, electrical, mechanical, and reliability and maintainability requirements as contained in this specification. The FAA will review the preliminary test procedures and provide comments to the contractor within 30 days after receipt. The contractor shall update the procedures and submit it in final form for FAA approval at least 30 days prior to start of tests. Each test section of the test procedures shall reference the specific requirement of this specification which is being verified by the test described.

The contractor shall notify the FAA in writing of test dates for contractor conducted tests 2 weeks prior to the start of such tests. The FAA reserves the right to witness any and all tests and to require additional testing as may be needed to verify compliance with this specification. Test procedures and data sheets shall comply with all requirements of FAA-STD-010.

3.5.7 Test Reports.

Upon completing each test defined by the approved test plan, the results shall be recorded and submitted to the FAA. The test report shall contain a complete description of the test results. The test report shall also contain, as a minimum, the information specified below:

1. Copies of test data sheets.

2. A indication of the performance of each equipment under test and whether it meets the system requirements.

3. A list of function3 that were tested.

4. Information as to whether the results of the test !re in agreement with the required reliability of the unit or system.

5. A record of any engineering changes found necessary to correct design deficiencies.

6. Copies of all discrepancies noted during the test with the FAA accepted dispositions.

7. Copies of all deviations from the approved test Procedures required during the conduct of testing.

3.5.8 Reliability Program Plan.

The contractor shall prepare and submit to the FAA for approval a Plan to implement a reliability program in accordance with MIL-STD-785. The Plan shall be submitted in accordance with the schedule contained in the contract. This program is specified in paragraph 3.4.2.

3.5.9 Maintainability Program Plan.

The contractor shall prepare and submit to the FAA for approval a Plan to implement a maintainability program in accordance with MIL-STD-470. This Plan shall be submitted in accordance with the schedule contained in the contract. This program is specified in paragraph 3.4.3.

3.5.10 Reliability and Maintainability Reports.

The contractor shall prepare and submit quarterly Reliability and Maintainability Reports to the FAA. These reports shall contain results of all analysis, predictions, etc., as required in the Reliability and Maintainability Program Plans.

3.6 LOGISTICS.

3.6.1 Maintenance Requirements.

Preventive maintenance on the ERDIRS shall normally be performed on standby units, however, on-line units may be serviced provided no interruptions to recording occurs. The average time allowed for preventive maintenance shall not exceed 1.5 hours per recorder per week and 1 hour per week for the balance of the system. The hardware maintenance features as stated herein shall provide the means to meet maintainability requirements as set forth in paragraph 3.4.1.

3.6.1.1 Maintenance Approach.

The maintenance approach shall be to localize failures and replace the failed module or pluggable unit from spares. The actual repair of the replaced module shall be accomplished in a designated bench repair area. All special tools, special test equipment, etc., required to repair the module shall be furnished by the contractor. Where printed circuit boards are utilized, the replaceable module shall be considered to be the printed circuit board.

In the interface area between the recorders and the display computer, if that portion of the interface physically contained in the DGIO basket assembly of the DGU (i.e., the A6 DGU/ERDIRS Interface Printed Circuit Board) should fail, the normal procedure would be to reconfigure DCVG 6 of the appropriate DGU out

of the operational system, replace the failed A6 printed circuit board, and reconfigure DCVG 6 back on line. The failed board would then be repaired in the designated bench repair area.

3.6.1.1.1 Status Indicators.

The ERDIRS equipment design shall include features necessary to monitor performance and status of each major equipment. This information as specified in paragraphs 3.2.1.2.2 and 3.2.2.2.1 shall use illuminated indicators.

3.6.1.1.1.1 Indicator Lights.

Lights used as indicators of equipment performance or status shall consist of devices replaceable from the front without requiring the use of special tools. A manual test push button shall be provided on each panel as a means of detecting indicator light failures.

3.6.1.1.2 Test Points.

Test points shall be provided for measurement and observation of such voltages and waveforms as are needed for installation, calibration, maintenance, and repair of individual equipments. Except where the functioning of circuits would be adversely affected by long leads, test points shall be accessible on the front panels or immediately behind the access doors of all equipments. Test points necessary for alignment and adjustment purposes shall be accessible without a card extender. All test points shall be identified with a number; and where space permits, the voltage value, signal wave form, or descriptive title (if voltage value or waveform would not be particularly significant) shall be indicated ajacent thereto. This information shall be on each schematic diagram. Only descriptive titles or voltage values shall be shown for test points on exterior front panels. Suitable plastic cards may be used to illustrate interior waveforms where the specified methods of interior marking are impractical. The contractor shall provide convenient and sufficient storage for the plastic cards within each cabinet if cards are provided.

The equipment shall provide for connection of such test equipment as may be required for its installation, maintenance, calibration, and repair. Connection of test equipment to the test points shall not degrade system performance. Short circuiting to ground of any test point shall not cause equipment component failures or interfere with system operation.

3.6.2 Spare Parts Provisioning.

Spare parts provisioning shall be determined by the contractor, coordinated with the FAA, and a mutually acceptable list of spare parts approved by the FAA. This provisioning list shall include the part name, part number, manufacturer, cross references, national stock number (where available), and estimated cost. Spare parts peculiar shall be in accordance with FAA-G-1375.

Spare modules, printed circuit boards, assemblies, and component parts shall be of the same quality as originally installed in the equipment and shall be subjected to the same parts selection, testing, and burn-in as the original parts. Wherever possible, the contractor shall fabricate spare modules, printed circuit boards, and assemblies at the same time as the production items. Delivery of spares shall be

coincident with the delivery of each ERDIRS. Warranties applied to modules and assemblies in the original agreement shall be extended to spare modules, printed circuit boards, and assemblies of the same type.

4. QUALITY ASSURANCE PROVISIONS.

4.1 GENERAL.

The contractors quality assurance program shall be a scheduled and disciplined plan of events integrating all necessary inspections and tests required to substantiate product quality during all phases of the contract. The FAA reserves the right to perform or witness any of the inspections or tests which are deemed necessary by the government to assure that equipment and services conform to the prescribed requirements.

For purposes of performing tests on the ERDIRS, the FAA will furnish two PVD's and two DCVG's to the contractor on a loan basis. This equipment shall be returned to the FAA upon completion of the contract.

4.2 QUALITY CONTROL PROGRAM.

The contractor shall provide and maintain a quality control program in accordance with FAA-STD-016. All inspections and tests made by the contractor shall be subject to FAA inspections. An FAA inspector will witness the contractor's inspections and tests and will carry out such visual and other inspections as deemed necessary to assure compliance with the contract requirements.

4.3 ACCEPTANCE TESTS.

All tests shall be performed by the contractor. The approved version of the contractor's Test Plan and Test Procedures shall govern the execution of these tests.

4.3.1 Preliminary Tests.

Prior to the time the contractor notifies the government that the initial production system is ready for inspection, and to demonstrate readiness for inspection, the contractor shall perform Preliminary Tests in accordance with paragraph 1-4.3.1 of FAA-G-2100/1.

4.3.2 Design Qualification Tests.

Design Qualification Tests shall be performed in accordance with paragraph 1-4.3.2 of FAA-G-2100/1 and the following subparagraphs.

4.3.2.1 Functional Qualification Tests.

There shall be a test or series of subtests to verify that all functional characteristics of the ERDIRS are in conformance with the requirements of this specification. Basically, these tests shall demonstrate the ability of the ERDIRS to sample and accurately record display data, and to play back the data from any

two displays simultaneously on two PVD's without exceeding the specified error rate and to properly perform all other functions required by this specification. In addition, these tests shall demonstrate any other functions inherent in the design of the ERDIRS, but not specifically defined as a requirement.

4.3.2.2 Reliability Demonstration Tests.

A Reliability Demonstration Test shall be performed on the ERDIRS in accordance with Test Plan IVC of MIL-STD-781C using the accept/reject criteria therein, corresponding to decision risks of 20 percent and a discrimination ratio of 2.0:1. The test shall be used to verify the system reliability requirements as detailed in paragraph 3.4.1 and shall be conducted on the equipment at the Technical Center.

The contractor shall develop the plan for this one-time Reliability Demonstration Test based upon the requirements in MIL-STD-781C and it shall be included in the Test Plan as specified in paragraph 3.5.5. The plan shall include a section stating the contractor's proposed method of incorporating design changes found necessary during reliability testing. Test procedures shall be prepared in accordance with MIL-STD-781C and submitted to the FAA for approval.

4.3.2.3 Maintainability Demonstration Tests.

Maintainability Demonstration Tests shall be performed on the ERDIRS in order to verify the MTTR requirements for the major equipments as stated in paragraph 3.4.1 of this specification. MIL-STD-471A shall be used in the selection of maintenance tasks and the development of all tests and test procedures. Computation of the MTTR and the accept/reject criteria shall also be performed, using MIL-STD-471A as a guide, and using a consumers and producers risk value of 0.10.

The contractor shall develop a plan for the one-time Maintainability Demonstration Test which shall be included in the Test Plan as specified in paragraph 3.5.5. The plan shall include a section stating the contractor's proposed method of incorporating design changes found necessary during maintainability testing. All test procedures shall be submitted to the FAA for approval.

4.3.3 Acceptance Tests.

Acceptance Tests shall be performed on each ERDIRS in order to demonstrate that each system meets the specification requirements and is ready for FAA acceptance. These tests shall include Factory Tests and On-Site Tests with the tests to be performed as described in the approved Test Plan (reference paragraph 3.5.5).

Factory Tests shall be performed on each system prior to shipment to the scheduled FAA facility. The system shall not be shipped from the factory until it has passed these tests. On-Site Tests shall be performed on each system following shipment and installation at the FAA facility. Successful completion of these tests and any other condition defined in the contract shall be the basis for final acceptance of the system by the FAA. Special attention shall be given in the On-Site Tests to demonstrate proper interface operations and compliance with all requirements. Test requirements to be covered in each category shall include, but shall not necessarily be limited to, those defined in the following subparagraphs.

4.3.3.1 Factory Tests.

Factory Tests as defined in the approved Test Plan shall be performed on each ERDIRS. These tests shall be conducted to ensure by demonstration that the system, using simulated input data, is capable of performing all functions and meeting all requirements contained in this specification.

After the contractor has completed all necessary adjustments to the system in preparation for performing these tests, no further adjustments to the system shall be made until completion of all required tests, unless otherwise approved by the government. A record of all such adjustments shall be kept and made a part of the factory test data. The government reserves the right to require any retesting deemed necessary to assure that the system is meeting all specified requirements, in the event that adjustments were required after the start of the test.

4.3.3.2 On-Site Tests.

Upon completion of the ERDIRS installation at the scheduled FAA facility, the contractor shall perform On-Site Tests to verify that the installation has been accomplished satisfactorily and that the system operates in compliance with all requirements of the specification. These tests shall be the final demonstration prior to acceptance by the FAA.

At a minimum, the contractor shall perform System Functional Tests and a Forty-Eight Hour Test as defined in the approved Test Plan.

4.3.3.2.1 System Functional Tests.

The contractor shall conduct System Functional Tests in accordance with the approved test plan and test procedures to verify that the system as installed in the field meets all performance requirements detailed in this specification. These tests shall provide sufficient checks to confirm the satisfactory performance of all channels, modes, and functions of the system.

4.3.3.2.2 Forty-Eight Hour Test.

Following the satisfactory completion of the System Functional Tests, a Forty-Eight Hour Test shall be performed with the Recording Subsystem operating continuously for 48 hours at all design center values in order to demonstrate the overall operational stability of the system. The plan for this test shall include the proposed pass/fail criteria to be used and it shall be consistent with the specified reliability requirements.

5. PREPARATION FOR DELIVERY.

5.1 SYSTEM PREPARATION REQUIREMENTS.

Shipment of all material and equipment required for each ERDIRS installation at the site shall be the responsibility of the contractor as specified in the Contract. All equipment shall be prepared for shipment in accordance with MIL-E-17555. The contractor shall also be responsible for transportation of all deliverable equipment to the installation site and within the building.

5.2 SPARE PARTS PREPARATION REQUIREMENTS.

All spare parts shall be marked, packaged, and packed for shipment in accordance with the requirements of MIL-E-17555.