DOT/FAA/CT-82-34

TECHNICAL ANALYSIS OF IOCE REPLACEMENT

JUNE 1981

DOT/FAA
CT-82/34

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
TECHNICAL CENTER
Atlantic City Airport, N.J. 08405

Technical Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
DOT/FAA/CT-82-34		

4. Title and Subtitle	5. Report Date
Technical Analysis of IOCE Replacement	June 1981
	6. Performing Organization Code
7. Author(s) Software Engineering Branch, ACT-740	8. Performing Organization Report No. FAA-CT-700-41
9. Performing Organization Name and Address Federal Aviation Administration Technical Center Atlantic City Airport, NJ 08405	10. Work Unit No. (TRAIS)
	11. Contract or Grant No.
12. Sponsoring Agency Name and Address U.S. Department of Transportation Federal Aviation Administration Systems Research and Development Service Washington, DC 20590	13. Type of Report and Period Covered Final
	14. Sponsoring Agency Code ACT-740

15. Supplementary Notes

16. Abstract

This document analyzes the concept of replacing the Input/Output Control Elements (IOCEs) in the NAS Enroute System computer complex with a plug compatible, higher speed processor, the IBM 4341. Projected system improvements to be realized, increased processing power, increased channel capacity, and enhanced reliability, are discussed. Technical feasibility, system impact, projected schedules, and cost estimates are also covered. Two potential software redesign strategies are evaluated, with a potential for increased processing capability estimated between 10% and 40%.

17. Key Words	18. Distribution Statement
	Document is available to the U.S. public through the National Technical Information Service, Springfield, Virginia 22161

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	66	

PREPARED BY

DATA ENGINEERING & DEVELOPMENT DIVISION

ACT-700

EXECUTIVE SUMMARY

The requirement for increased system capacity to meet Air Traffic Control requirements until the replacement system is deployed is under study by the Federal Aviation Administration. A variety of alternative approaches has been proposed to satisfy the interim requirement. One of the more promising alternatives is the proposal to replace the present Input Output Control Element (IOCE) in the 9020 configuration with a plug-compatible, higher speed processing unit. The replacement unit proposed is the IBM 4341 processor. AED-1 has requested the FAA Technical Center, Data Engineering and Development Division, ACT-700, to perform a technical analysis of the IOCE Replacement proposal. The enclosed report contains the results of this analysis.

As of this date, however, there is no formal IOCE Replacement Proposal specifically defining design philosophy or identifying the magnitude of the overall effort. In performing this analysis, ACT-700 relied upon IBM briefing material and the results of in-house NAS/VM-370 testing to formulate an IOCE Replacement design.

There are two major areas in the current NAS 9020 Enroute Air Traffic Control Program where system improvement is required. These areas are increased computer processing power and increased channel capacity. IOCE Replacement, with appropriate software module offloading, appears to offer a significant improvement in processing capability and channel capacity. The proposed IOCE Replacement unit, the IBM 4341 Processor, offers five times the processing power of the present IOCE and double the channel capacity. In addition to these improvements, the following advantages could be realized:

- Retention of functional equivalence to the present IOCE and capability to operate with minor modifications to remaining 9020 elements, interfaces and configurations.

- Programming instruction compatibility.

- Minimum installation complexity (e.g. floor space, power, environment, cables), after integration activity.

- Increased reliability/availability through improved error recovery and correction techniques.

- Availability of VM/370 Operating System.

Two software offloading strategy proposals are identified, Options A and B. Option A, an offloading strategy with primary emphasis on flight plan processing functions, potentially yields a system processing improvement of 10 to 15%. Option B, with emphasis on radar processing, tracking and display, could yield a potential system processing improvement of up to 40%. Option B, however, is a significant software redesign activity with an inherent increased risk factor.

IOCE Replacement design verification, test and implementation would be initially performed at the FAA Technical Center. A Transition Plan for field deployment would be developed and finalized, also at the Technical Center. ATF-1 approval of the proposed transition philosophy would have to be obtained early in the activity based on the procedures developed at the Technical Center.

IOCE Replacement activities at the Technical Center would impact NAS support activities through diversion of hardware configurations and support personnel resources throughout the development and test activities. At the ARTCCs, system down time can be expected when the new IOCE hardware is being cabled into the system. In the transition phase, a daily system test period, of approximately four hours low traffic, will be required during which live traffic is handled manually. The on-going operation is also affected by the unavailability of IOCE and PAM redundancy during the time required for integration of the three replacement IOCEs.

Estimates of cost and schedule can, at best, be rough estimates at this point in time. Very preliminary cost estimates amount to $100 million for implementation of Option A and $115 million for Option B. Schedule estimates indicate 30-32 months from start of effort to initial field site installation and approximately 50 months to completion of installation of IOCE Replacement at all ARTCCs.

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A. INTRODUCTION

The load on the NAS Enroute Air Traffic Control System is nearing its maximum capacity. This is particularly true of those sites having the 9020A Central Computer Complex. The agency has a program to develop a replacement computer system, but this system may not be operational prior to experiencing capacity problems with the present system.

In addition to the long term computer replacement program, there are presently under consideration several interim systems which may be required to extend the life of the basic 9020 Systems before their final replacement is available. These interim systems include:

- Rehosting the NAS Software on a new generation computer.
- Off-loading portions of the NAS Software to other computer systems.
- Enhancing the DARC System to include radar data processing and other functions presently being performed in the 9020 System.
- Replacing the present IOCEs.

These interim systems are presently under investigation by various agency and contractor personnel. AED-1 has requested the Technical Center to support the investigation of the IOCE replacement. This report summarizes the results of this investigation.

Computing power at the present 9020A sites is the most critical resource. At certain sites the computer utilization is approaching 75 percent. Under this condition, the system response time is adversely affected. Off-loading some of the NAS software tasks to the present IOCE has been investigated as an interim solution to improve CPU utilization. Replacing the IOCE with a more powerful unit appears to offer some attractive advantages. These advantages include:

- Increased system flexibility.

- Minimum changes in adapting the operational program.

- Ease of system transition.

- Reduced maintenance.

The replacement for the IOCE considered in this report is the IBM 4341 computer. A 4341 computer is presently available at the Technical Center and is used as an Operating System (OS) Jobshop. Also available are components of the 9020C (360/50) System previously used for Jobshop purposes.

Some actual experiments have been accomplished in rehosting the NAS operational program on the 4341 computer previous to the request by AED-1 for IOCE Replacement support. Although the work was not entirely applicable, certain portions of this work have been used in supporting the analysis contained in this report.

1. PRESENT SYSTEM

The Central Computer Complex is an IBM Model 9020 Computer. The computer is modular in design and can be configured to various numbers of components tailored to the ATC processing requirements. The computer accepts and processes data from remote locations such as radar sites, adjacent Centers, and ATC Terminal facilities. Two prime functions of the computer are to prepare and distribute flight plans via the flight strip printers (FSP) and to provide updated radar information to the display subsystems.

The IBM 9020 systems are solid-state data processing systems which provide the data manipulating versatility to perform the Air Traffic Control functions. Individual 9020 systems, designed for the Central Computer Complex (CCC) environment, are composed of the following types of major self-contained, self-powered elements and units:

Computing Element	(7201-01) or(7201-02)
I/O Control Element	(7231-02)
Storage Element	(7251-08) or (7251-09)
System Console	(7265-02)
Peripheral Adapter Module	(7289-02)
Tape Control Unit	(2803-01)
Storage Control Unit	(2314-A1)

The IBM 9020 system design incorporates the following features:

- Any Input/Output Control Element (IOCE) can access any storage element.
- Each Peripheral Adapter Module (PAM) is connected to the system through two Input/Output Control Elements.
- Each Input/Output line is connected to the system through a subchannel in each of two Peripheral Adapter Modules.

2. IOCE DESCRIPTION

The IBM 7231-02 Input/Output Control Element (IOCE) has two major purposes; the primary, to control I/O devices; the secondary, to process data under control of a computing element (CE).

a. DATA FLOW

The IOCE data flow consists of hardware required to control:

- Information transfers between IOCE and CE.

- Information transfers between IOCE and preferential storage area (PSA) within a Storage Element (SE).

- Data transfers between I/O control devices attached to the Multiplexor Channel and the Storage Elements (SE) or MACH storage.

- Data Transfers between I/O control devices attached to the Selector Channel and the Storage Elements (SE) or MACH storage.

- Transfer of certain IOCE status conditions to the System Console or Configuration Console.

- Information transfers between CLU and MACH and/or main storage.

Figure A-1 shows the general relationship and interfaces between an IOCE and the computing elements, storage elements (SE) and input/output devices.

Common Logic Unit (CLU)

The CLU contains transistor registers, data transfer paths, and controls. The CLU also has twenty-one (21) full-word registers used for channel data and control storage.

Data flow is controlled by a Read-Only Storage Unit. This is a capacitor storage unit operating on a 0.5 usec cycle.

MACH Storage

MACH (maintenance and Channel) storage is a 32K word, 2.0 usec cycle core storage contained in the IOCE. Part of this storage (1024 words) is used to store control words for the multiplexor channel (four words per subchannel). The remainder provides storage facility for processor operations, channel data, and maintenance operations.

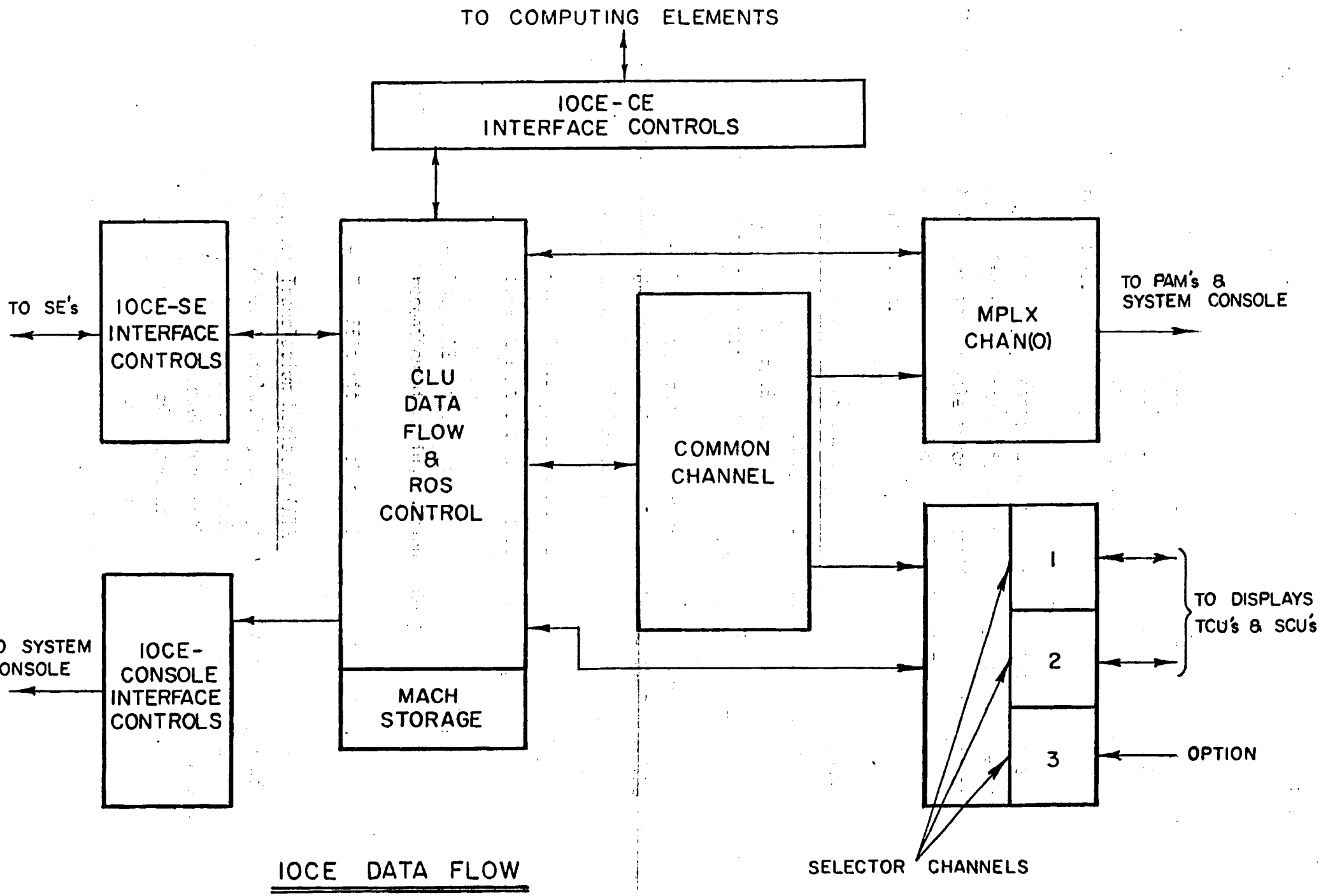

TO COMPUTING ELEMENTS
IOCE-CE INTERFACE CONTROLS
TO SE's
IOCE-SE INTERFACE CONTROLS
CLU DATA FLOW & ROS CONTROL
COMMON CHANNEL
MPLX CHAN(O)
TO PAM's & SYSTEM CONSOLE
O SYSTEM ONSOLE
IOCE-CONSOLE INTERFACE CONTROLS
MACH STORAGE
1
2
3
TO DISPLAYS TCU's & SCU's
OPTION
SELECTOR CHANNELS
IOCE DATA FLOW

FIGURE A-1.

Multiplexor Channel

The 7231-02 is equipped with one Multiplexor Channel. This channel is capable of controlling several low to medium speed I/O units simultaneously in multiplex mode or a single higher speed unit in burst mode.

Selector Channel

The 7231-02 is equipped with two Selector Channels (expandable to three channels in the first two IOCEs within a 9020 System). A Selector Channel is capable of handling high speed I/O devices.

Selector Channels operate in burst mode. Only one device may be selected at a time, and no other I/O device on the Selector Channel can operate until the activity of the selected unit has been terminated.

b. DESIGN HIGHLIGHTS

The IOCE interfaces with the CE, SE, PAM, and other I/O devices of the 9020 System.

Communication between IOCE and CE is accomplished via cabling between the units. This cabling constitutes the logical boundary (interface) between the IOCE and CE of the IBM 9020 systems.

In general, I/O instructions, IOCE-Processor control signals, interruptions, masks, addresses, condition codes and various other inter-element control functions are transmitted across the IOCE/CE interface. Only control information is transferred between these elements.

In addition, the IOCE accepts signals over the interface to perform various special functions.

Similarly, communication between IOCE and SE is via the IOCE/SE interface cabling. The information passing over this interface is primarily data, protection keys and addresses.

Additional communication between IOCE and System Console or Configuration Console is via the IOCE/System Console or Configuration Console interface cabling. The information passing over this interface is primarily IOCE status information.

Configuration Control Register (CCR) - This is a register in the CLU that is loaded by a SCON instruction issued by a CE via the IOCE/CE interface. The contents of this register define:

- The state that the element is in, which in turn determines which manual controls are enabled on the IOCE Control Panel.

- The CE with which it operates for all functions other than the SCON instruction.

- Those CE's from which the IOCE will accept a reconfiguration instruction (SCON).

- The SE's with which the IOCE can communicate.

Address Translation Register (ATR)

With address translation, a program written for a span of addresses within one SE can, under program control, be relocated and executed from another SE that does not contain the original span of addresses. A reassignment of the SE's within the system only requires changing the contents of the address translation registers of the accessing elements.

The ATR in an IOCE is a 48-bit register divided into 12 four-bit positions, each position being assigned to a block of logical addresses. A logical address produced by the program identifies a logical SE, which selects a corresponding four-bit position of the ATR. The bit configuration (hexadecimal character) in this ATR position will change the physical SE selected although the logical SE does not change.

3. 4341 DESCRIPTION

The 4341 Processor is an intermediate-scale, general purpose processor. The processor provides arithmetic, logic and control functions, storage, channels, and system diskette drive.

The 4341 design is based on System 370 architecture. Compatibility with existing NAS 9020 architecture will require certain hardware modifications to the base 4341 machine. These include:

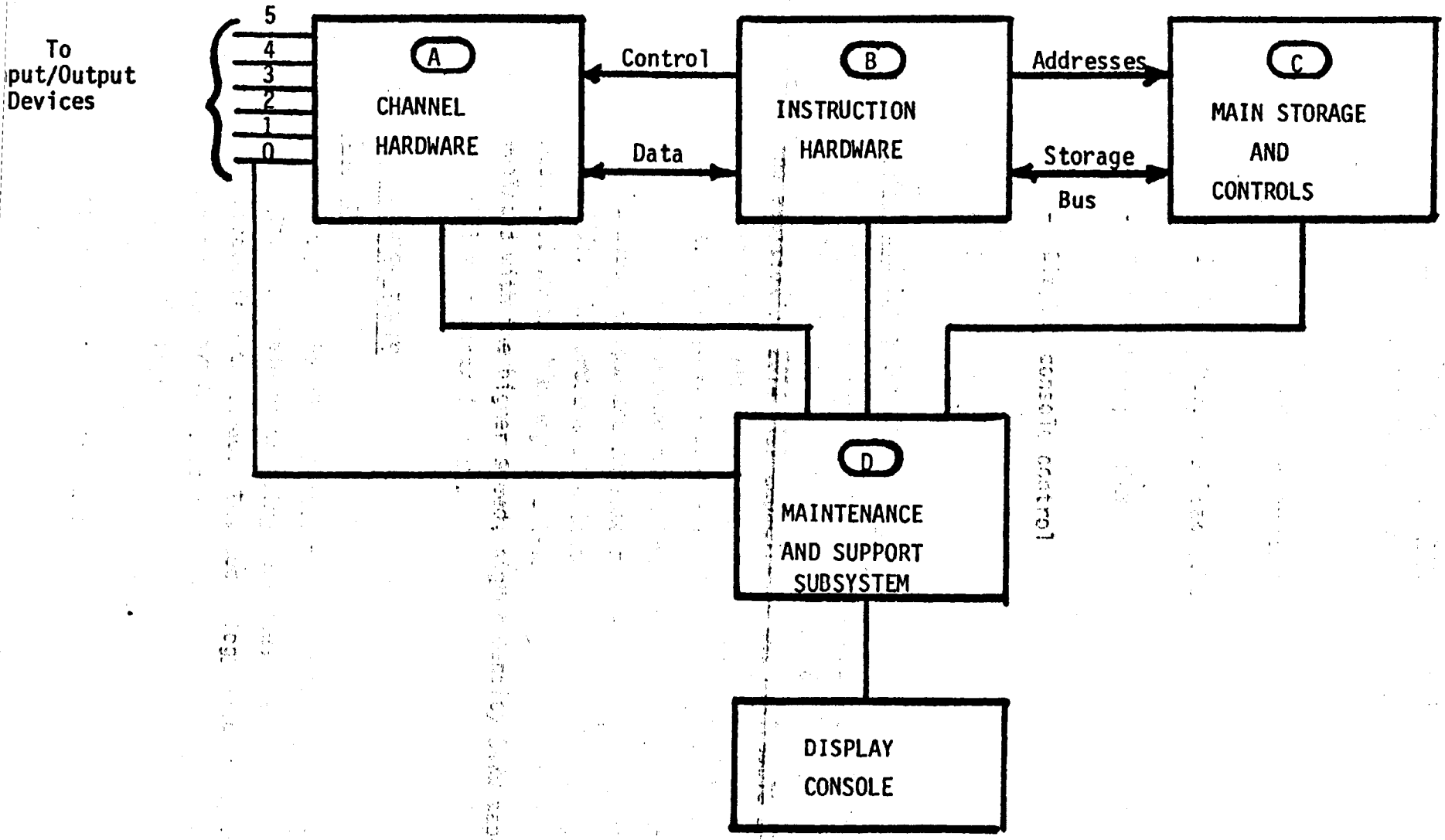
- Inter-element communication interfaces (including 9020 System Console interfaces).
- Inter-element interrupt capabilities.
- Set Configuration (SCON) instruction operation.
- Storage Element access by the replacement IOCE.

a. DATA FLOW

The functional operations of the 4341 processor use hardware registers called external registers that are located throughout the hardware. The external registers are data links between the user programs, microcode and the 4341 processor hardware. Figure A-2 shows the data flow for the 4341 processor.

Channel Hardware

The channel hardware contains the interconnections and controls



4341 - BLOCK DIAGRAM

FIGURE A-2.

to communicate with and obtain data from the input/output (I/O) devices. The 4341 can have up to six channels (two byte-multiplex channels and up to four block multiplex channels). The channel includes:

- Interface Adapters Section
- Interface Controller Section
- Channel Control Section
- Channel Data Buffer Section

Instruction Processor

The instruction processor is the hardware unit that processes the data and programs. It contains the hardware and microcode to interpret and execute the source programs and to control the channels and main storage. The instruction processor includes:

- Arithmetic Logic Unit Local Storage/Data Flow Registers
- Shifter Circuits
- Storage Addressing and Update Registers
- Control Storage

Main Storage and Controls

Main storage and controls is the unit that contains the processor storage. It also contains the address control circuits to address and control each area of the processor storage. The main storage and controls includes:

- Storage Address Control Section
- High-Speed Buffer Section
- Main Storage Section

Maintenance and Support Subsystem

The maintenance and support subsystem (MSS) is the unit that performs:

- Power control and monitoring
- Initial microcode load (IML)
- Test and diagnostics
- Display console control
- Error logging

High Speed Input/Output Equipment

The required DASD capacity for the replacement IOCE is not available with the present complement of 2314 disk equipment. The addition of 2314 disk capacity is not desireable since its operating speeds would not match those of the 4341 I/O channels. State-of-the-art disks (3350s) would provide significantly increased speed and capacity. System reliability should also be enhanced because of the fixed media design of the 3350s. The present Disk Control Units would be replaced with 3830 DCUs. The magnetic tape subsystem should also be replaced with the higher speed, higher density 3420 tape drives and 3803 tape control units.

b. DESIGN HIGHLIGHTS

Storage

All storage in the 4341 (processor, control, high-speed buffer, and local) is implemented using monolithic technology instead of discrete ferrite cores. The technology used for processor storage in the 4341 processor provides a much denser storage chip (64K bits per chip) than is used in most System/370 processors (2K bits per chip) and a new bipolar technology is used for control storage and high-speed buffer storage.

A two-level storage system is implemented, consisting of large processor storage used as backup storage for a smaller high-speed buffer storage. The instruction processing functions works mostly with the buffer so that the effective processor storage cycle is a fraction of the actual processor storage cycle. 8K bytes of high-speed buffer storage are standard. Data is fetched from the buffer at a rate of 225 nanoseconds for a doubleword.

Microcode

Reloadable control storage to contain all the microcode required by the instruction processing function of the 4341 processor is standard. Use of writeable, instead of read-only, control storage offers the advantages of improved system serviceability and ease of optional feature and engineering change installation.

Error checking and correction (ECC) hardware automatically corrects all single-bit processor storage errors and detects (but does not correct) all double-bit and many multiple-bit errors.

Channels

The following channel features are provided for the 4341 processor: Two channel groups are available for the 4341 processor, each consisting of one byte multiplexer and two block multiplexer channels.

The byte multiplexer channel has a 16 kb/sec maximum data rate in byte mode of single-byte transfer operations and 64-kb/sec maximum byte mode data rate for four-byte transfer operations. For burst mode operations, a maximum data rate of 1 mb/sec is possible for a buffered device. Functionally, the byte multiplexer channel for the 4341 processor is equivalent to that for System/360 and System/370 processors.

The standard block multiplexer channels have a maximum data rate of 2 mb/sec each. The maximum aggregate data rate for the 4341 is approximately 7 mb/sec.

Optionally, one Channel-to-Channel Adapter can be installed in a 4341 processor and attached to any block multiplexer channel. The adapter can be used to connect the channel in the 4341 processor to a channel in a System/360, a System/370 or another 4341 processor.

Display Console

A 3278 Model 2A Display Console, consisting of a cathode ray tube keyboard, and operator control panel, is required as the operator console. The display console is used to perform manual operations that for System/360 processors are performed using switches and pushbuttons on a control panel located on the front of the processor unit. The display console is also used for operator-to-operating system communications and for diagnosing processor malfunctions.

4. COMPARISON OF 4341 AND IOCE (7231-02)

Increased Instruction Execution Performance

The cycle time of the 4341 processor varies from 150 to 300 nanoseconds with an 8-byte parallel data flow. The cycle time of the 7231-02 IOCE is 500 nanoseconds with a 4-byte parallel data flow.

Improvements in the number of functions performed during the instruction cycle of instruction execution result in the faster execution of many instructions, most of which are among the more frequently used instructions. The standard instruction set for the 4341 processor includes many new general purpose and control-program-oriented instructions in addition to the powerful System/370 instruction set.

Larger, Faster Processor Storage

Processor storage sizes of 2048K bytes and 4096K bytes are provided. The 7231-02 IOCE has a maximum of 128K bytes. The effective access time to processor storage in the 4341 processors is faster than that of Models 50 and 65 (two microseconds for four bytes for the Model 50 and 750 nanoseconds for eight bytes for the Model 65 versus 225 nanoseconds for eight bytes for the 4341 processor). The effective access time to processor storage in the 4341 processor is lower because of the implementation of a high-speed buffer. This improved access time increases internal performance and permits faster I/O devices to be attached to the 4341 processors.

Greatly Expanded I/O Capabilities

The fast internal performance of the 4341 processor, together with the expanded use of multi-programming, requires that more data be available faster than the 7231-02 IOCE. The 4341 processor support more and faster concurrent high-speed I/O operations than the 7231-02. It also provides block multiplexing capability, which is not available for the 7231-02.

The I/O features of the 4341 processor provide:

- Two more channels than are available for the 7231-02 (six versus four).

- Attachment of high-speed, high capacity, direct access devices.

- Attachment of higher speed tape units.

- Potential increases in channel throughput via use of block multiplexing and rotational position sensing to improve effective data transfer rates.

- A significantly higher attainable aggregate I/O data rate than the 7231-02 IOCE to balance the higher performance capabilities of the 4341 processor (maximum 7 mb/sec for the 4341 processor versus .8 mb/sec for the 7231-02).

Pertinent features of the 4341 and 7231-02 are summarized in Table A-1.

TABLE A-1

HARDWARE FEATURE	7231-02	4341-L1
Processor Storage (kilo bytes)	128	4096
Processor Storage Cycle (nanoseconds)	2000 for 4 bytes	225 for 8 bytes
Type of Processor Storage	Ferrite Core	Monolithic
Instruction Time Add (nanoseconds)	3250	375
Selector Channels	3	4
Maximum Aggregate Data Rate for Channels (megabytes/sec)	0.8	7.0

B. ASSUMPTIONS/REQUIREMENTS

For the proposed IOCE replacement to be a viable interim system improvement, the following assumptions/requirements must be satisfied:

1. The present NAS Enroute System is in a condition of stability, and will continue to provide the required system support until it can be replaced. System "stability" connotes a normal level of software fix activity (PTRs) and hardware maintenance, and also the absence of any major software or hardware change activity. The stability must be such that hardware component replacement or program element offloading can be efficiently accomplished.

2. IOCE replacement considerations will not be in competition with plans and activities of the Computer Replacement Program. The scope of the IOCE Replacement effort must be such as not to impact the design, schedule, implementation, test or funding of the Computer Replacement activity.

3. Implementation of the IOCE replacement at the ARTCCs must be accomplished with minimum impact to Center operations. An ARTCC deployment plan must be included as part of the overall IOCE Replacement Design Plan.

C. EVALUATION CONSIDERATIONS

1. TECHNICAL FEASIBILITY

One of the primary considerations in evaluation of an interim system is that it must be usable in significantly less time than it would take to implement and install the ultimate computer replacement system. For this to be achievable, this interim system implementation depends on the ability to limit the impact by utilizing the existing software. While it is practically impossible to achieve an interim system without impacting software at all, it becomes highly desirable to minimize the amount of code to be written or redesigned to accommodate hardware updates. The software impact then must be limited to those module changes required to assimilate the new architecture and selected modules to take advantage of the new architecture.

Toward this end, a System Control Program should be available to be implemented, with minimal modification, to operate in the IOCE replacement hardware. It would need to provide the mechanisms to control the increased number of channels and support the reliability, availability and serviceability features of the IOCE replacement. It would also need to support the selected software modules to be offloaded for processing. For the IOCE replacement activity, this system control program is the Virtual Machine Facility (VM/370).

The VM/370 System Control Program is the 370 oriented program supplied and supported by IBM. In some respects, VM performs the same system control tasks as does NAS. For example, both NAS and VM -

a. Schedule work (applications) to run on the systems they control.

b. Allocate the CPU to tasks, using an algorithm designed

to accomplish scheduled work in priority sequence.

c. Manage storage resources, I/O, the CPU and data.

d. Attempt to recover from or limit the impact of hardware and software failures.

e. Provide a coherent set of interfaces (Macros or high-level languages) to shield applications programmers from many of the rigors of machine-level coding.

VM is, however, unlike NAS in several important respects.

a. Main storage management.

b. Operating systems as applications.

c. Work scheduling.

d. I/O resource sharing among multiple users.

e. Error recovery.

Main Storage Management

VM, or rather its predecessor, was originally designed for use on a modified 360/65, which is the same technology base as that of the 9020. The key system modification is a hardware unit sometimes referred to as the DAT (Dynamic Address Translation) box, which turns the machines from a fixed-memory to a virtual-memory system. This unit permits a part of a program running in memory to reference a part of the same program located on a disk device--having been put there because it was idle and not profitable using the main storage it occupied. Recognizing that a segment of a running program is not in main storage, the

DAT box notifies system control software to read in the temporarily "missing" page (4096 bytes). Wherever the page is placed in main storage, the DAT box will locate it through tables it maintains describing the contents of all of main storage. These same tables point to pages on auxiliary (disk) storage containing parts of programs that have been "paged out" due to lack of use. By constantly monitoring program demands on real (main) storage, and by paging programs in and out as necessary, VM gives its users the impression of having available a quantity of main storage far exceeding the amount physically attached. The theoretical foundation for this implementation of "virtual" storage is the "locality-of-reference" concept. This says that a given program will use only a subset (perhaps 20%) of its total code in a given slice of time, while the remainder will not require execution until somewhat later. NAS/9020 and other pre-virtual systems can concurrently run programs equal or less than the size of the system's physical storage. VM and other "virtual" systems eliminate this constraint.

Operating Systems as Applications

The single, unique aspect of VM among virtual operating systems is that the "applications" that run under it are, in reality, other operating systems. These other operating systems schedule and perform work as if they were running standalone in a CPU. Through a very simple description of the I/O and memory resources alloted to each virtual machine, VM creates a directory, by name, of the subset of total system resources each user is alloted. Each of these guest operating systems and application programs is, in effect, independent and is called a "virtual machine." Any system 360 or system 370 operating system will run under VM in a virtual machine, concurrent with a number of other virtual machines. Performance is, of course, the limiting factor in determining how many virtual machines can be run at one time. NAS uses special instructions not present on standard processors, and therefore presents a special problem to VM. A combination of hardware, NAS and VM modifications can resolve the known conflicts.

Work Scheduling

VM, unlike NAS, is not an event driven system. Rather, each virtual machine is "time sliced", or given a limited time (measured in thousandths of a second) to run, after which use of the CPU is passed to another virtual machine. Numerous system programmer and operator options exist to bias performance in favor of a designated virtual machine. The basic time-slicing mechanism, however, remains in effect.

I/O Resource Sharing

VM achieves a level of I/O device sharing surpassing that of other operating systems. By segmenting a single disk into multiple uniquely addressable units (minidisks), the virtual machines running under VM perceive a number of disk drives far in excess of those actually installed. Non-sharable devices, such as tape drives, are dedicated to specific virtual machines until no longer needed. In addition to virtual storage and virtual disks, VM provides a virtual channel-to-channel adapter--functionally equivalent to that connecting a 9020D to a 9020E--but implemented through software to connect two virtual machines running under VM.

Error Recovery

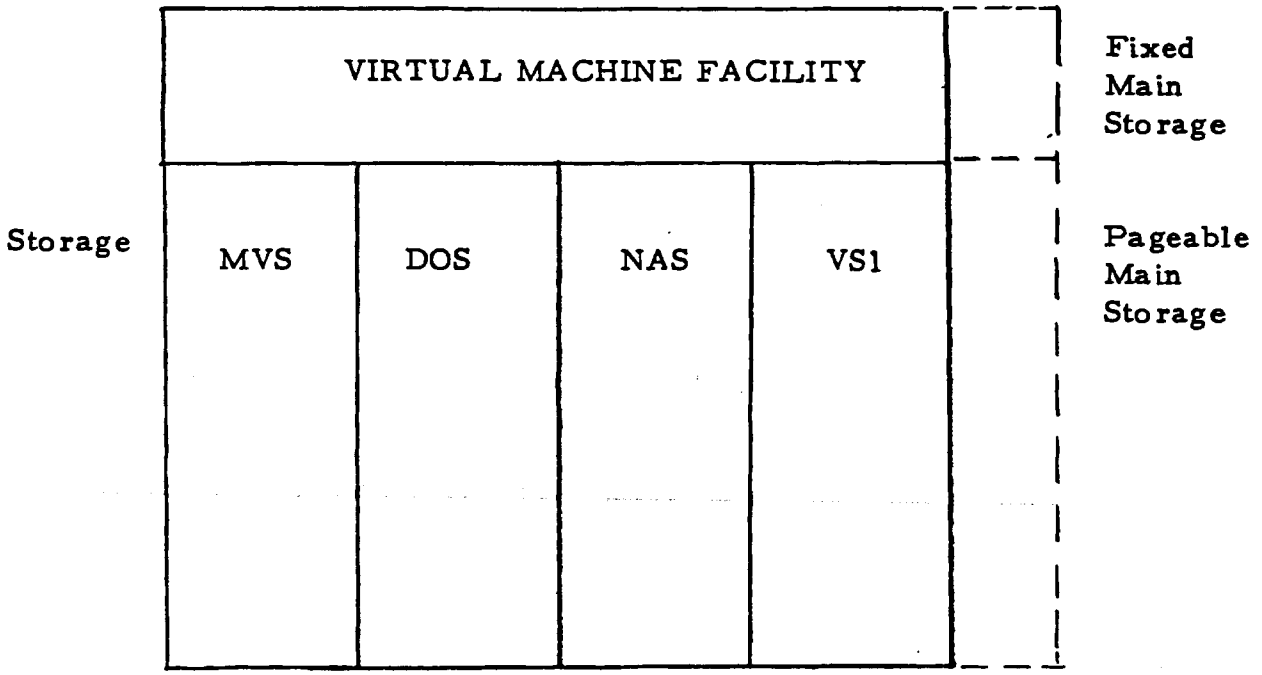
Since VM is in control of the real hardware resources of the system, it will handle and attempt to recover hardware error conditions relating to the active virtual machines. If an error condition proves unrecoverable, the related virtual machine will be terminated. Except in the case of real CPU hardware failures, this termination will normally not impact other active virtual machines. VM will attempt to recover its own software failures. When an abnormal software condition occurs in a virtual machine, VM traps the error and passes it to the operating system under which the failing application is running. Thus the native software error recovery capabilities of the guest operating systems are not diminished when executed under VM.

Assuming the necessary VM and NAS modifications (the hardware problems are not addressed in this section), NAS would communicate with VM--like most other operating systems--only in a passive sense. That is to say, VM would determine when NAS was to have control of the CPU, would pass relevant interrupts to NAS for processing and would field or forward hardware and software errors according to a standard set of rules. A higher level of communication, one with significant performance and functional implications, is possible. By using the "diagnose" instruction (seldom used except by NAS and VM), VM could be made aware of NAS's specific support needs and could satisfy them in a timely fashion. While the VM architecture provides the base for communications using "diagnose", enhancements to both the NAS and VM code would be required to take full advantage of this capability.

To summarize, VM is an operating system with the capability of interfacing with the NAS Operational program. Under VM's control, virtual machines (processors) are defined as having a given amount of main storage and a specified number of I/O resources. Within any virtual machine, any 360 or 370 operating system can be loaded (assuming sufficient memory and I/O devices) and can then run application programs with no awareness that they are, in a sense, under the control of VM. Pictographically, this capability can be represented by the following diagram of main storage in a VM system: (Figure C-1)

2. SOFTWARE IMPACT

The VM/370 System Control Program is a feasible choice as the operating system for the IOCE replacement. Differences in architecture, however, dictate the need for generation of changes to the VM software as well as the NAS Operational software. The overriding consideration would be to limit the amount of change that would be required to the NAS program.



VM ARCHITECTURE

FIGURE C-1.

Where possible, "common" changes would be made to the VM/370 System Control Program. Changes to overcome instruction set differences between the two software systems would be accommodated in VM/370. The NAS program changes required are in the area of Operation Error Analysis Program, Configuration Control, Startup/Startover, and Input/Output operations. The specific changes are discussed below.

Software Changes to VM

The initial set of changes would involve instruction set differences between the 9020 and System 370. These include:

Write Direct	WRD
Read Direct	RDD
Start I/O	SIOP
Move Words	MVW
Load Data Address	LDA
Delay	DLY
Insert Address Translator	IATR
Load Identity	LI
Load PSBAR	LPSB
Set Configuration	SCON
Set ATR	SATR
Store PSBAR	SPSB
Set PCI	SPCI

In some cases, the above 9020 unique instructions are not recognized by VM. In other cases, the OP code is a different instruction under VM. Changes to the above, however, can be reconciled within VM. The modifications can be performed through changes to the microcode and operating philosophy of the base machine. The final design of the functional changes would need be determined in a separate activity.

It should be noted that the VM/370 System Control Program is a widely-used program supported through IBM central support software maintenance on a 24 hour, 7 days a week basis. This assistance at VM installations is required due to the complexity of the system control program. Deviations or modifications to VM/370 System Control Program, as a result of required NAS changes, would however, result in a non-standard system which would probably not be supported by IBM. In that case, the FAA would be required to assume VM support responsibilities. A core of VM trained system programmers could provide adequate support to the modified VM/370 System Control Program. It would be centrally supported at the FAA Technical Center.

Software Changes to NAS

IOCE Replacement and offloading of software will require modifications to the current NAS Enroute Operational Software. The modifications are required, first, to provide compatibility between the 9020 system architecture and the VM/370 architecture. The instruction set differences addressed above are an example of some of the compatibility modifications required. These instruction set changes have been identified at the FAA Technical Center in NAS/VM experimental runs. Modifications were performed at the Technical Center to achieve a form of compatibility for the purposes of the experimental runs. These modifications took the form of op code changes, simulating the instruction and tie-off of functions. Final resolution of these compatibility modifications would have to be studied to

arrive at an optimum method or design(software changes, microcode, etc.) to overcome the anomalies.

Other incompatibility changes that will entail changes to the NAS program are in the areas of:

a. Operational Error Analysis Program (OEAP)

b. Configuration Control

c. Startup/Startover

d. I/O Operations

e. Data Tables Integrity

Operation Error Analysis Program (OEAP)

The IOCE Replacement Processor contains a significant error logging and analysis function that is used by VM to perform retries and to recover from intermittent failures. Data relative to catastrophic failures is retained in a special purpose error logging storage for use in off-line fault analysis.

Error handling within the IOCE is accomplished by VM. Upon detection of an error the IOCE attempts instruction retry and data repair prior to generating a machine check interrupt to the CEs. Since the machine check interrupt is generated only if the IOCE has unsuccessfully attempted self correction, the interrupt is tantamount to declaring the IOCE is down and the NAS system must reconfigure and restart. Thus the present IOCE logout diagnostic capability in OEAP can be removed.

Configuration Control

Configuration control of tape and disk I/O devices will be shared between the IOCEs and CEs.

Supervisory manual configuration and re-configuration of the system's TCUs and DCUs would remain under control of the NAS monitor executing in the CE. During processing of supervisory messages calling for re-configuration of TCUs and DCUs, the CE will initiate the actual configuration by direct control communication with the appropriate IOCE. When completed by the IOCE, an indication is returned to the CE describing the results of the request.

Automatic re-configuration in response to an error condition is performed by the NAS monitor in the IOCE. The result of the reconfiguration is communicated to the appropriate CEs to update system status data and report to supervisor positions.

Startup/Startover

The startup of the proposed system would remain essentially equivalent to the existing system. Additional software coordination between CEs and IOCEs would be required to initialize VM and configure appropriate TCUs and DCUs. The initialization of IOCE related control data and data base would be performed in the IOCE storage while CE related control data and data base would be performed in the system storage.

Startover and recovery recording would necessarily be reorganized to reflect the split between Flight Data Processing (FDP) and Radar Data Processing (RDP) startover requirements. Additional startover software coordination and re-establishment of data bases from the recovery recording will be required when the system is encountering an outage. Overall startover can be accomplished in a time comparable to the current system.

Input/Output (I/O) Operations

Monitor I/O operations must be handled by the replacement IOCE in order to capitalize on the increased capacities of the IBM 4341. In this environment, input/output operations would be supervised in the 4341. This I/O processor operating under VM in the 4341

will handle all aspects of the I/O operations and communicate status back to the NAS monitor in the CE via a direct control protocol.

The I/O processor would communicate in a similar way with the NAS monitor running under VM in the 4341. VM would only simulate the direct control communications. This means that only one set of modifications to the common NAS monitor code would be needed to function in both the 9020 and the 4341 under VM.

The I/O processor performs the normal I/O functions in moving data between the devices and storage, be it 9020 SE or 4341 virtual storage. For data transfers to and from the 9020 SE, all channels, except the block multiplexor channel, transfer data directly into or out of the 9020 SE. Due to the high speed of the block multiplexor channel, the I/O processor buffers this channel's data in the 4341 before transferring it. This buffering prevents any channel overrun condition on this channel.

In addition to controlling all NAS I/O operations, the 4341 would, of course, also perform the processing associated with the offloaded NAS functions (Option A or Option B). Further, since VM has the capability to set up multiple virtual machines, each operating under its own operating system, it is possible to perform other, non-NAS, software tasks in the 4341 concurrent with the NAS operation.

Data Table Integrity

Relocating FDP or RDP functions and their related data base to the IBM 4341 involves the sharing of some common data base between the IOCE and CE executed functions. The data tables unique to the software functions offloaded to the IOCE replacement will be made resident in the IOCE. This will minimize SE interaction and

allow the IOCE replacement to perform at its individual speed. Relocation of non-unique data tables (i.e. access required by both IOCE and CE resident subroutines) will be dependent on the level of activity required. High level of activity would predicate the non-unique data tables to remain in SE storage. Access to these tables in the current NAS system is regulated by locking concepts controlled by the accessing CE/IOCE. Lower level of activity could dictate relocation of the data table(s) to the IOCE. Additional application subprogram(s) will be required to ensure data table integrity in the ultimate multi-location design.

3. SYSTEM IMPACT

Test and implementation of the IOCE Replacement must be accomplished with a minimal impact on the on-going operations of the NAS Enroute Operational System. A transition plan would have to be developed and approved minimizing the resources required and the inherent disruption to the on-going operation. To achieve this, the initial hardware and software checkout would have to be accomplished at the FAA Technical Center. Key activities to be performed at the Technical Center include:

- Hardware test of the IBM 4341 as an IOCE replacement.
- Hardware test of the total hardware system.
- Development and test of software modifications.
- Integration and test of software modifications with hardware configurations.
- Preparation and verification of procedures for deployment to a test ARTCC.
- Finalization and approval of Transition Plan.

The above activities would be dependent on the following assumptions:

- The 9020C system at the FAA Technical Center is available for initial hardware system test.

- The 9020A system at the FAA Technical Center is dedicated to the IOCE Replacement for initial system integration tests. Checkout of the deployment and transition procedures would be accomplished on this system.

- The Transition Plan for integration of the IOCE Replacement would have to be approved prior to any testing at the FAA Technical Center.

The Transition Plan to be developed would have to address several areas:

a. ARTCC OPERATION

The major impact to be considered is the disruption of system operation due to unavailability of the NAS automation system. This occurs twice during the IOCE replacement effort; when the first IOCE is removed from the system and the 4341 cabled in, and again when the remaining IOCEs are physically replaced. At present, estimates of the length of each period range from eight hours to a maximum of 48 hours. The backup system would be used to control live traffic in these periods. Test efforts at the Technical Center will be oriented toward minimizing the down time.

In the period following physical IOCE Replacement, the NAS system is available, but without IOCE or PAM redundancy. During this phase of integration and testing, there is a requirement for a daily system test period of up to four hours. These tests should be scheduled during low traffic hours. Live traffic will be controlled manually during these

test periods, but if required, the normal NAS automation system can be instantly reconfigured into operation. The allotted time is expected to vary between ARTCCs based on each Center's unique traffic flow and operational limitations.

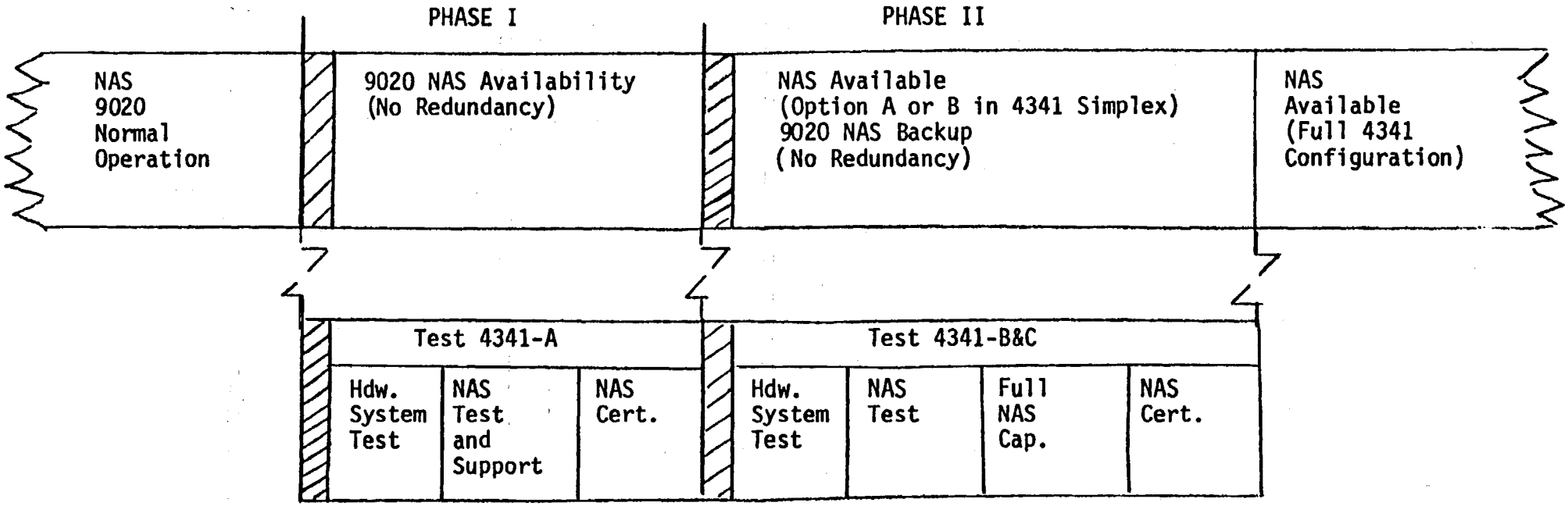
Another area of impact to field operations is the loss of IOCE and PAM redundancy for the duration of the installation, test, and commissioning time period. The off-line 9020 Simplex feature would be lost with the installation of the first replacement IOCE in the redundant Simplex. The length of time to integrate all three new IOCEs could be from two to 12 weeks depending on the type of transition approach developed and accepted. The approach will be determined by:

- Total testing required.
- Certification requirements.
- Resources available.
- Operational restrictions and demands.

Figure C-2 indicates the various phases of IOCE Replacement activity at each field site.

b. ARTCC RESOURCES SUPPORT

The IOCE Replacement will physically fit within the 7231-02 floor space, so that upon completion of the retrofit, floor space requirements will not be increased. However, during the integration and checkout phase, approximately 200 square feet of additional floor space will have to be made available for each IOCE replacement unit. In addition, technical support capability to install, integrate, operationally test and maintain the IOCE upgrade would have to be provided.



IOCE REPLACEMENT INSTALLATION

Replace IOCE
with 4341
NAS not avail.
Backup used

FIGURE C-2.

c. FAA TECHNICAL CENTER SUPPORT

The bulk of software and hardware integration testing would be performed at the Technical Center on system configurations currently dedicated to other on-going NAS programs. As an example, dedication of the 9020A system to IOCE Replacement testing limits its use in the on-going maintenance and development of the NAS Enroute Operational Program. This results in a major change in operation for the AAT, AAF and ARD organizations who fully utilize the 9020A system today. Additionally, FAA Technical Center resources would have to be reprogrammed from existing technical programs to support of the IOCE Replacement.

D. RATIONALE FOR IOCE REPLACEMENT

1. OBJECTIVE

The overall objectives of providing an interim upgrade to the NAS 9020 system configuration by substituting a modified IBM 4341 processor for the current 7231-02 IOCE are:

- Reduction of 9020 CE Load
- Response Improvement
- Provision of Discretionary Reserve

The method of accomplishing the objectives is to exploit the capabilities of the IBM 4341 processor as a replacement IOCE, and to transport selected FDP and/or RDP software modules to execute in the new IOCE. The selection criteria of the modules would include frequency of execution, high CPU utilization, and low storage element (SE) intercommunication. In addition to the increased processing power and improved response, the software offload should result in a reserve potential for implementation of planned Air Traffic Control functions or features.

2. ADVANTAGES

Implementation of the IOCE Replacement proposal could provide several operational and system advantages. The advantage potential of the replacement would be determined by the amount of code (functions) and data (tables) that can be offloaded into the 4341 storage. Due to the great difference in storage speed between the current 7251 Storage Element and the 4341 machine the maximum gain in processing power can be achieved only by offloading program functions and associated tables to the 4341 processor. There are several optional groupings of functions and tables that are prime candidates for this offloading. These will be identified and covered below under item 3., "Options."

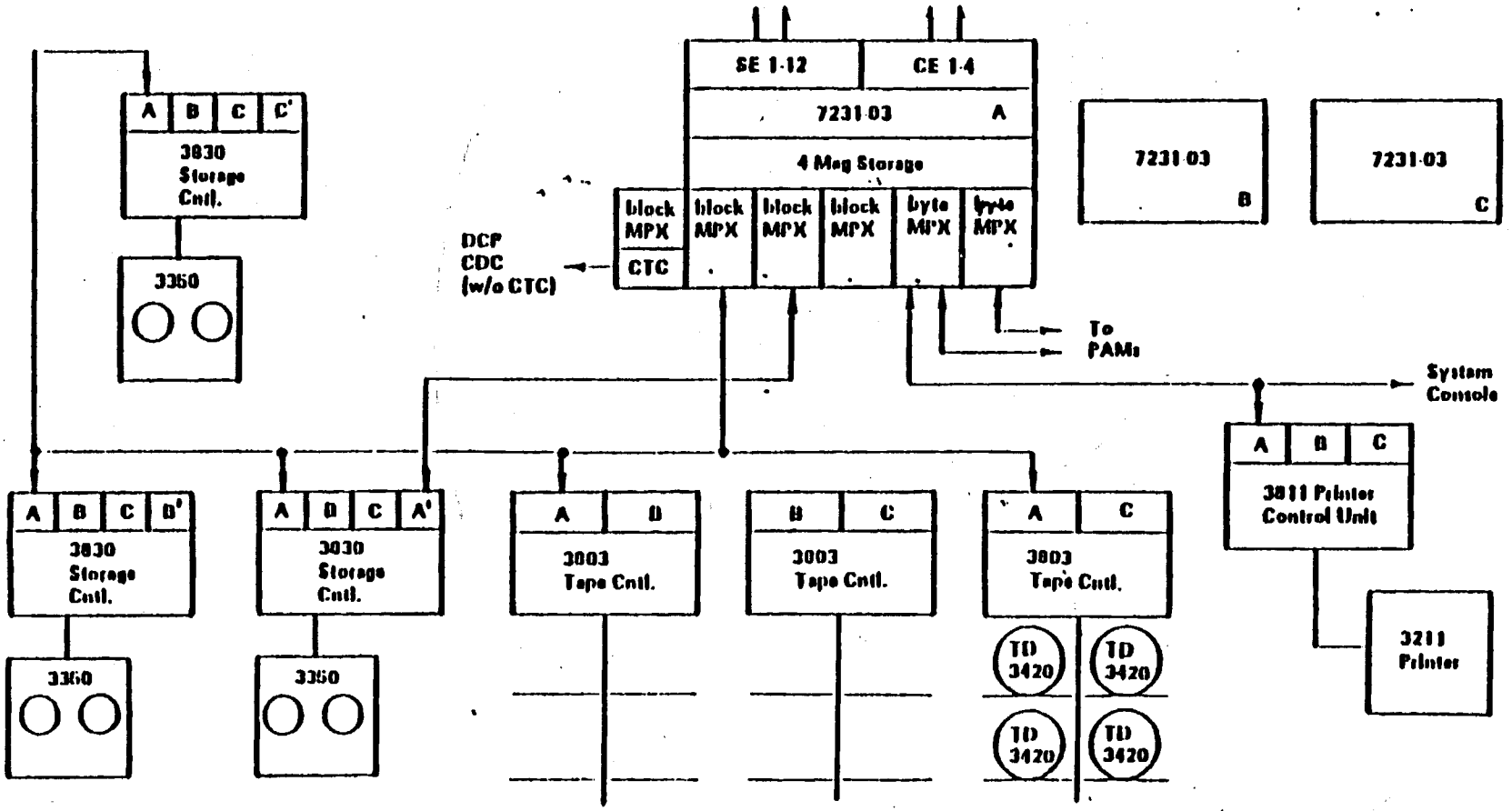
Increased channel capacity can be achieved through IOCE Replacement. Each 4341 has two byte multiplexor and four block multiplexor channels available, twice the number of channels in the present IOCE. The aggregate data rate of the present channels is 800k bytes/second. The aggregate data rate for the 4341 is 7m bytes/second. This capacity increase would relieve the channel saturation experienced at 9020D sites. The increased capacity and increased speeds, however, cannot be fully realized using presently available 2314 disk storage units and 2400 series tape drives. To take advantage of the increased channel capacity and speeds, software module offloading (Option A or B) and connection to high speed 3350 disk units and 3420 tape drives are required. Figure D-1 illustrates an optimum configuration of channels.

3. OPTIONS

a. CONSIDERATIONS

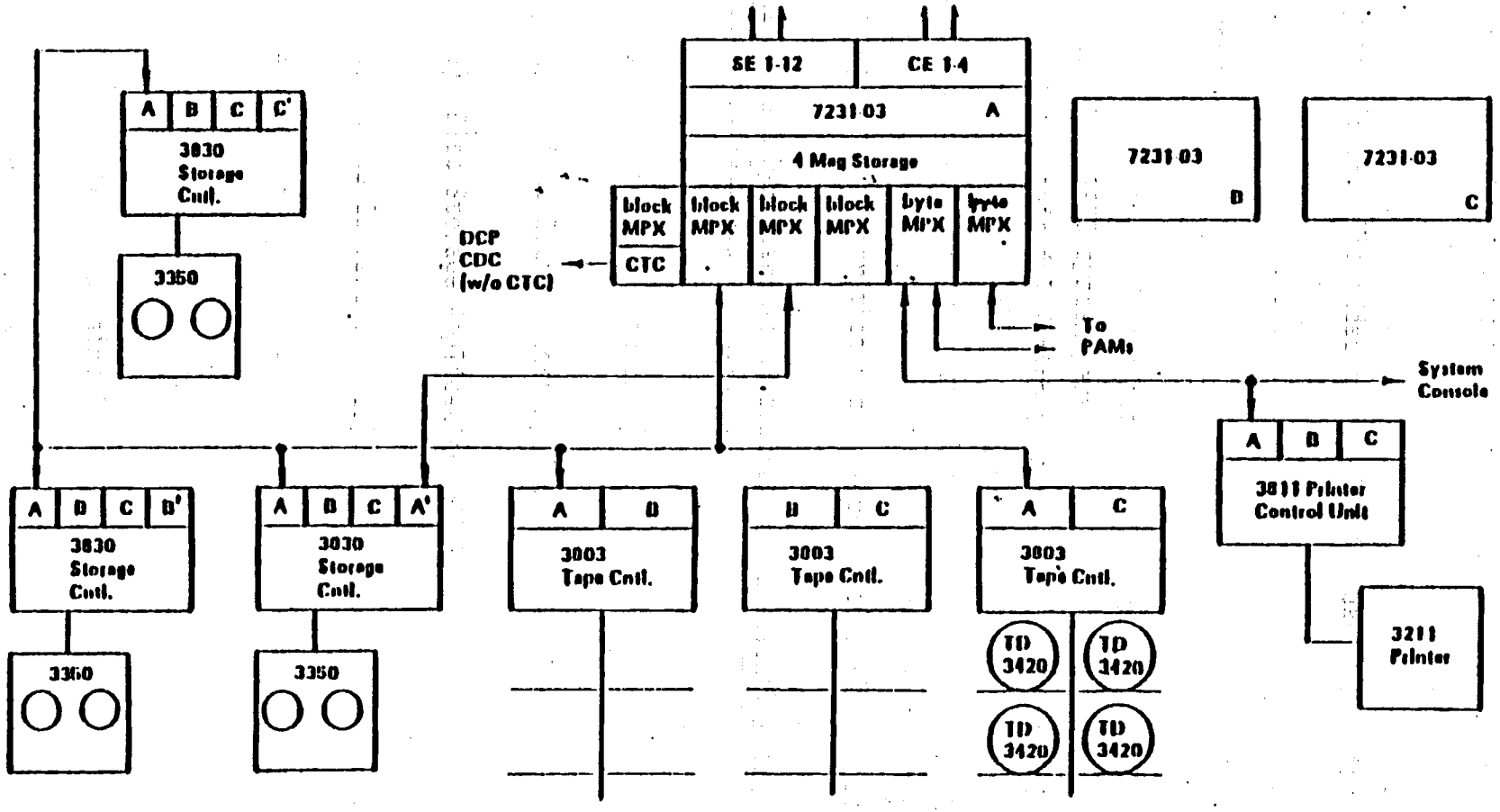
The replacement of 9020 IOCEs with newer, higher speed 4341 processors and retaining the current operational software structure would probably result in an increase in NAS system performance. This would primarily result from the increase in device, channel and instruction processing speeds of the 4341. However, any consideration given to replacement of IOCEs would have to consider a software offloading strategy that will provide a significant increase in system throughput and system response. The software offloading strategy would have to be structured around program modules that reference a localized data base or static portions of the global data base. See Section 3.b for estimates of software development costs for both options.

There is a significant mismatch in speed between the current IOCE/SE interface and the internal 4341 memory access speed. Requiring the higher speed 4341 to continually access data in the current SE configuration would slow the 4341 to the speed



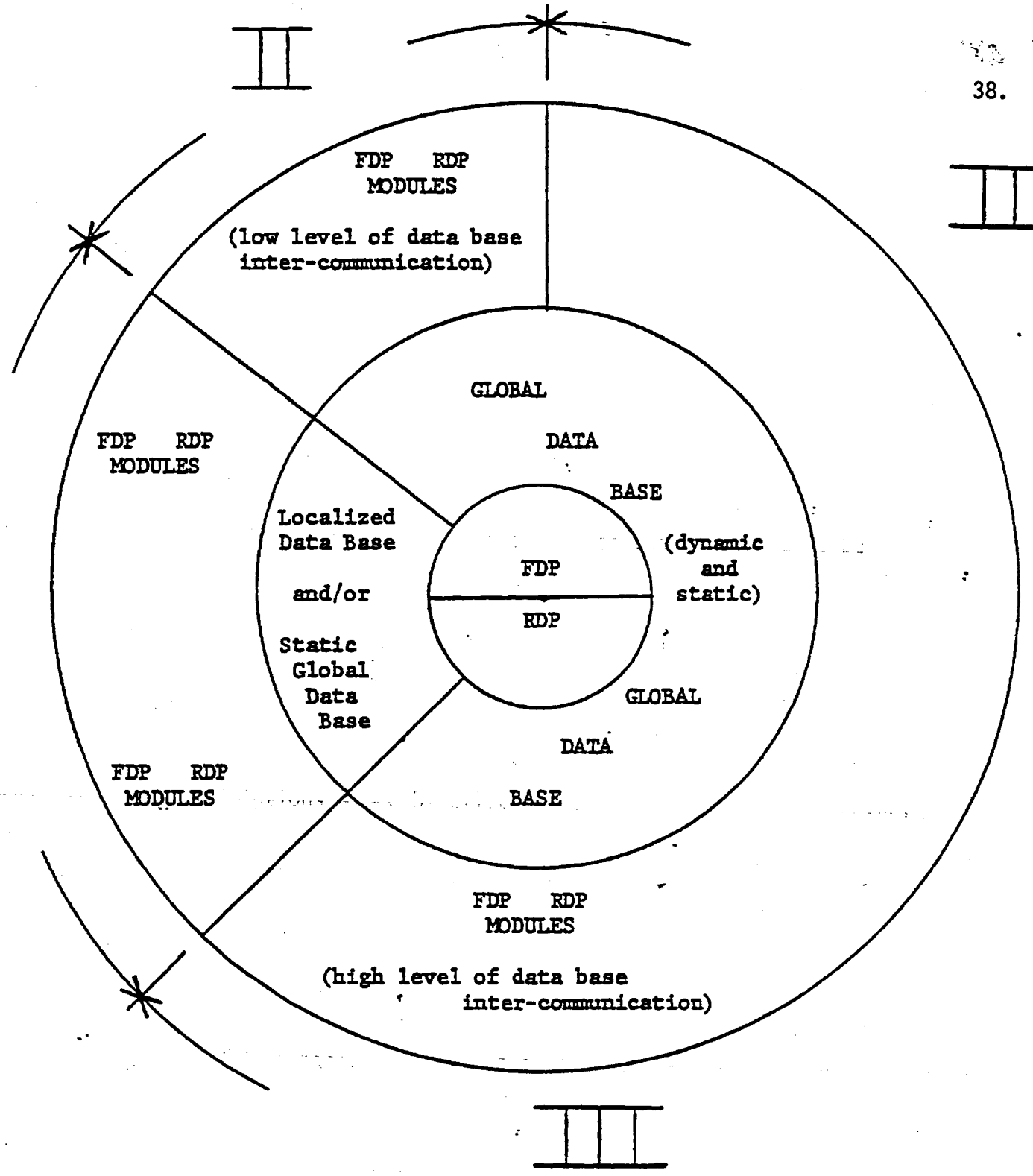
CHANNEL CONFIGURATION

FIGURE D-1.



CHANNEL CONFIGURATION

FIGURE D-1.



I. Most probable migration candidates

II. Possible migration candidates

III. Least probable migration candidates

LEVELS OF INTERCOMMUNICATION

FIGURE D-2.

accomplished sequentially, however, the display channel output would be initiated from the IOCE as opposed to the CE. An additional application subprogram is required for coordinating radar processing functions between the IOCE and the CE/SE. The added complexity increases the risk in selecting Option B as well as increasing the cost. However, the potential in CPU capacity recovery is correspondingly greater.

Since calculations of benefits derived from each software option are based on 1975 system performance data, it should be understood that meaningful design consideration, with regard to offloading software, can only be made after a thorough analysis of the current field operational system is completed. Consequently, the two options presented should be viewed as offloading possibilities rather than recommended functional approaches.

The current NAS operational program is functionally organized into 14 application subsystems:

1) Preliminary Processing (PREP)

2) Flight Data Processing (FDP)

3) Disc Storage Application (DAP)

4) Route Convertion (RCS)

5) Post Determination (POST)

6) Flight Status Alerts (FSAS)

7) Inquiry Processing (INQP)

8) Supervisory and Interfacility Outputs (SIOS)

9) Hardware Error Processing (HEP)

10) Track Data Processing (TDP)

11) Display Channel Outputs (DCO)

12) Real-Time Quality Control (RTQC)

13) Radar Processing and Tracking (RPAT)

14) Flight Plan Analysis (FPAS)

With regard to flight plan processing, it should be recognized that the entire processing to be performed on a single flight plan can fall into the realm of several of the above mentioned 14 subsystems. No one subsystem performs all of the processing on a single flight plan.

Options A and B reflect subsystems that are candidates, either whole or in part, for migration into the new IOCE. They are independent of each other.

Broadly defined, Option A is that set of operational software functions and associated data tables which process flight plan related inputs and produce an internally useable flight plan data base. Option B encompasses the software subsystems, in whole or in part, related to radar processing, tracking, and display output, in addition to real time quality control of radar data. Figure D-3 and D-4 show functional relationships between Options A and B and the balance of the operational software system. It must be borne in mind that the interconnections depicted do not show actual control or data lines between subsystems.

b. OPTION A

Option A will migrate the following subsystems into the new IOCE.

1) Radar Preprocessing (Filtering)

OPTION A FUNCTIONAL DIAGRAM

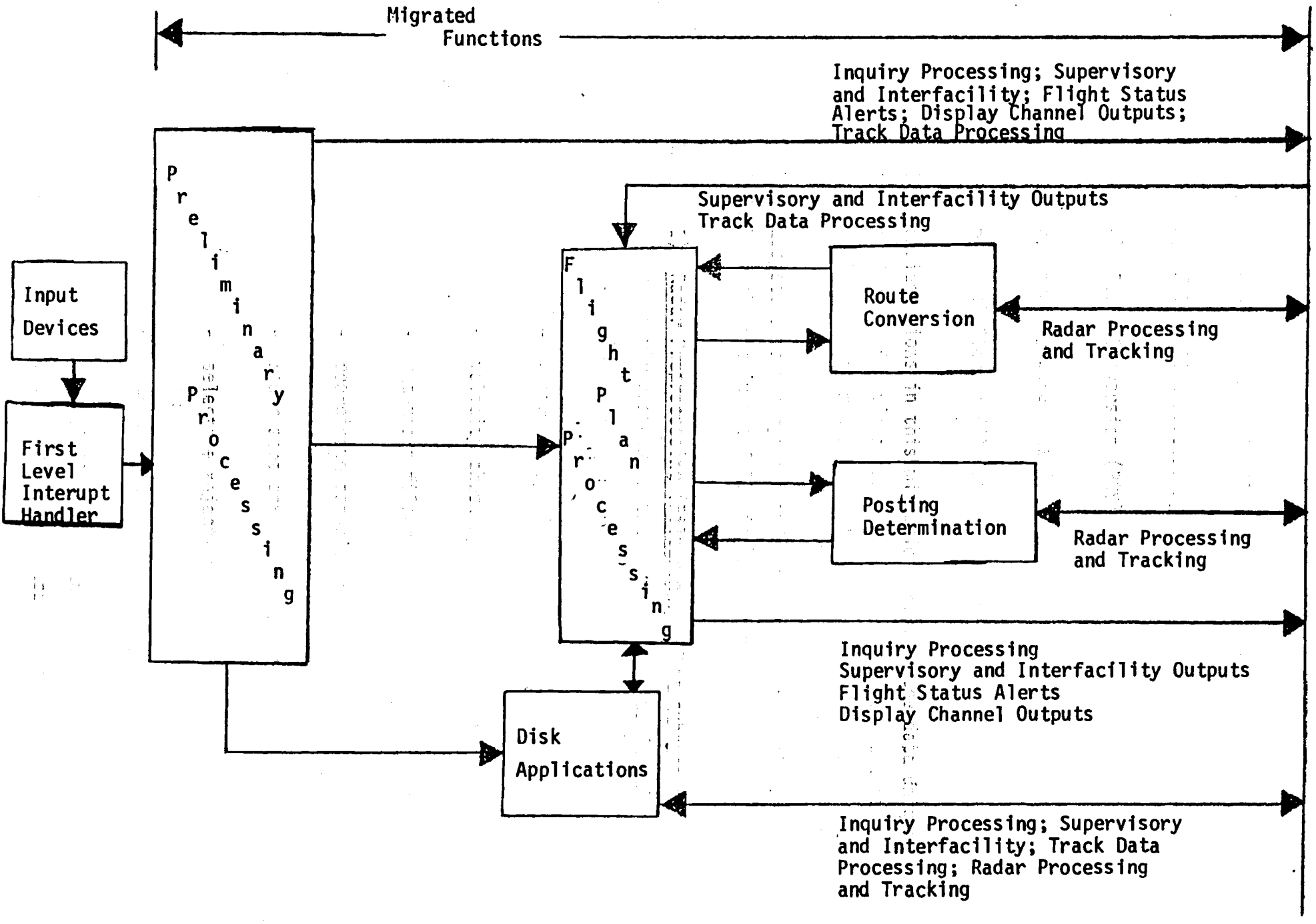


FIGURE D-3.

OPTION B FUNCTIONAL DIAGRAM

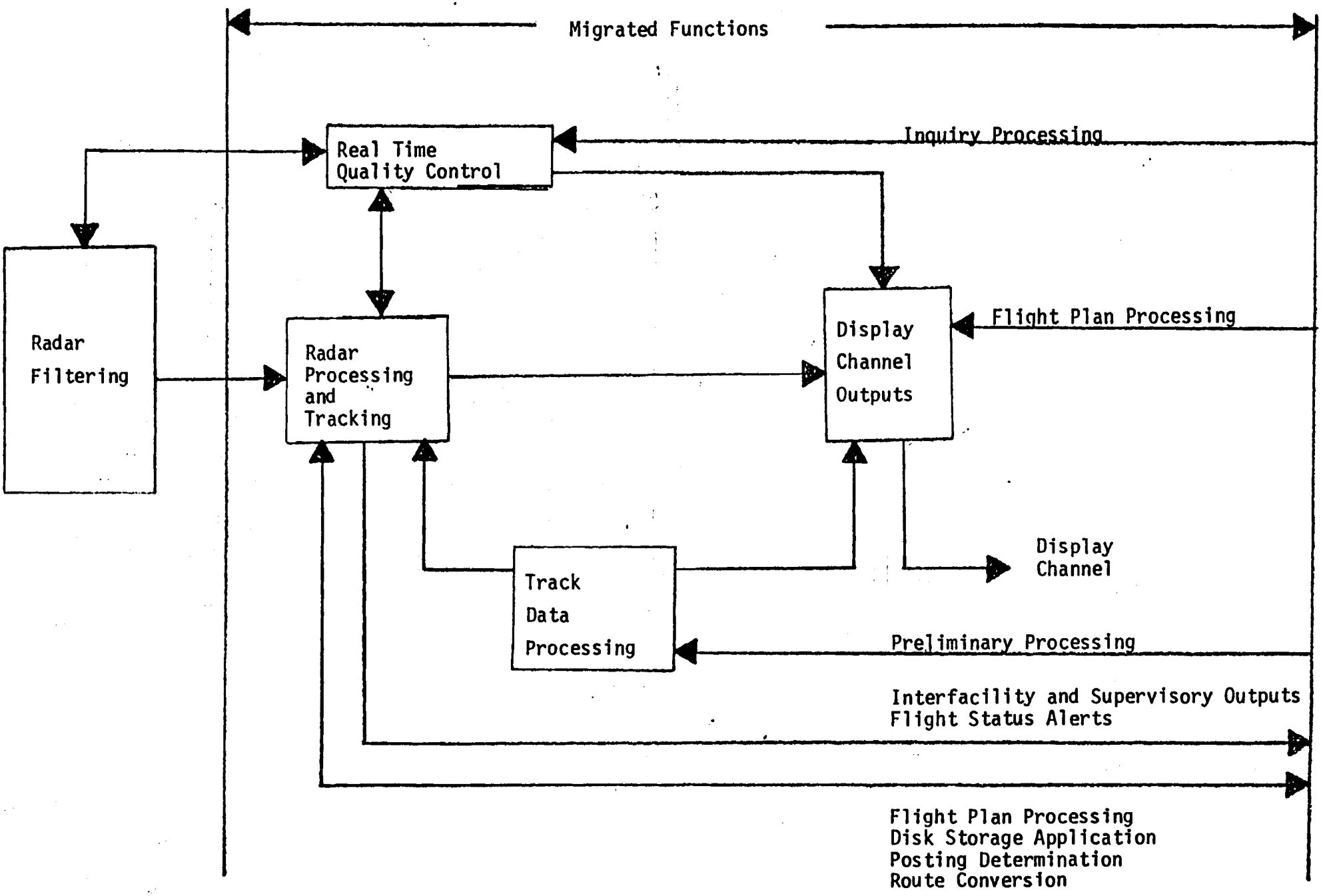


FIGURE D-4.

2) Preliminary Processing (PREP)

3) Flight Plan Processing (FPP)

4) Route Conversion (RCS)

5) Posting Determination (POST)

6) Disk Storage Allocation (Partial) (DAP)

Key considerations in this migration are that the data unique to the migrated functions resides in IOCE storage and that principal flight plan processing tables remain in SE storage.

The subsystems to undergo migration under Option A will be briefly explained in the following sections.

1) Radar Preprocessing (Filtering) - This subsystem currently resides in the 9020 IOCEs. Its function is to perform:

   - radar message identification
   - validity checking
   - rho-theta filtering
   - coordinate conversion
   - radar sort box determination
   - selective rejection
   - mode C pressure correction
   - compatibility between rho-theta filtering and radar sort box assignments

2) Preliminary Processing - The Preliminary Processing Subsystem performs startup and startover function, preliminary processing for all input messages, and table maintenance function required for various program communications tables and for the Flight Plan Index table. Preliminary processing is performed by the following input device processing subprograms and subroutines:

PAS	PDE	PNA
PCD	PFD	PTO
PCR	PIT	PTY
PDC	PKO	SDC
SAC	SAF	SAK
SAD	SAG	SAM
SAE	SAH	SAN

3) Flight Plan Processing - The Flight Plan Processing Subsystem performs functional processing for the messages that build or modify flight plan data base. Functional processing of the flight-plan-related messages is performed by the following flight data message processing subprograms

DAM	DHM	DRS
DDM	DMP	DSP
DFA	DPR	DVZ
DFP	DRF	

and by subroutines that provide for common function processing. These subroutines are:

CRP	SCG	SCR
LNM	SCH	SCU
SCA	SCJ	SDD
SCB	SCK	SDE

SCD	SCM	SDG
SCE	SCN	SDU
SCF	SCP	

4) Route Conversion- The Route Conversion Subsystem translates the route segments as received from the Flight Plan Processing Subsystem into a series of fixes that make up the route. The programs currently being considered for migration are:

RAA	RFL	RPR
RAL	RGS	RRD
RAM	RJJ	RTD
RAP	RKR	SHA
RDP	RPA	STB

5) Posting Determination - The Posting Determination Subsystem receives all the intermediate route records, with associated tables, for the completely converted route of flight from the Route Conversion Subsystem. Through the use of posting rules, the intermediate route records are transformed into aircraft route records and the associated tables are adjusted. Modules that are being considered for migration in this subsystem are:

PAM	PLT	PPS
PAP	PJJ	PRT
PAT	PMO	PSB
PCD	PPD	PTC
		PTM

6) Disk Storage Application - The Disk Storage Application Subsystem performs all functions necessary to establish, modify and maintain the integrity of the bulk storage file and the flight plan record file on disk storage devices. The subsystem performs all processing of

bulk storage file maintenance messages. The programs of this subsystem that are being considered for migration are:

DBC	DDV
DBM	SFC
DBS	SIO

Figure D-5 is a list of the data tables that must be migrated along with all of the above mentioned programs.

c. OPTION B

Option B will migrate the following functions to the new IOCE.

1) Radar Preprocessing (Filtering)

2) Radar Processing and Automatic Tracking (RPAT)

3) Track Data Processing (TDP)

4) Display Channel Outputs (DCO)

5) Real Time Quality Control (RTQC)

Key considerations in this migration are that data unique to the migrated functions must be resident in the IOCE storage and shared data will be resident in SE storage. Filtered radar data will be communicated from one IOCE to the other via SE storage.

A brief description of the subsystem to be migrated under the Option B plan is as follows.

Option A - Tables Migrated

AR	Airway Table
AS	Adapted Line Segment Index Table
AZ	Aircarrier/Airtaxi Identification Table
BB	B-line Table
BQ	Beaming Sensitive ARTS Coordination Reference Table
BS	Recovery Recording Begin/End Table
CB	Center Boundary Composition Table
CN	Coordination Fix Table
DD	Double-word Boundary Table
DZ	Disk Extents Table
EA	External Airport Table
EF	External Fix Table
FF	Fix Stratification Table
GT	Geographic Trace Communications Table
JU	Junction Identification Table
JV	Junction Pointer Table
KK	Intermediate Route Table
LI	Line Segment Trace Table
MV	Mnemonic Device Table
NG	Preliminary Field Descriptor Table
PN	PDT Index Buffer Table
RD	Adapted Direct Route Application Table
RI	Altitude Transition Processor Intercommunication Table
RO	Route Segment Input Table
RV	Arrival Fix - Coordination Fix Array
RX	Bulk File Record Control Data Table
SL	S-line Table
SQ	Subroutine SIO Interface Table
SX	MSX Working Area Table
SZ	SID/STAR Table
TA	Airport/Fix Off Airway/Coded Route Table
TN	Transition Route Control Fix Table
TP	Transition Route Pointer Table
TS	Stereo Data Table

FIGURE D-5

1) Radar Preprocessing (Filtering) (RPP) - This subsystem currently resides in the 9020 IOCE, and is already described under Option A.

2) Radar Processing and Automatic Tracking (RPAT) - This subsystem processes all radar data that enters the CCC and performs all radar surveillance and automatic tracking functions. The subprograms and subroutines to be migrated are:

RAT	RCC	RDE
RIN	RRC	RSL
RTG	RWD	SOC
VRT	RBC	RBR
RFA	RFM	RML
SDW	SFI	SFL
SPF	VBF	

3) Track Data Processing (TDP) - Track Data Processing performs functional processing for the messages that build or modify the flight plan, track and/or the display data base. The subprograms and subroutines to be migrated are:

CBC	JQB	JQD
JQN	JQP	JQR
JQT	JQU	JTA
JTI	JTU	KSM
SCV	SRA	SRC
SRF	SRG	SRN
KSI	KSU	

4) Display Channel Outputs (DCO) - Display Channel Outputs maintains track numbered displays and associated beacon codes for R positions, generates outputs for all displays and system status indicators at the R positions,

and performs all processing related to geographic map displays. The subprograms and subroutines to be migrated are:

CRJ	FDA	HCD
HCI	HHM	HJM
HRD	HTI	HTM
HTR	RDA	RGM
SHF	SHL	SHM
SHV	SIL	SOD
STM	STO	VHF

5) Real Time Quality Control (RTQC) - This subsystem monitors the status and test messages received from each radar site, maintains radar data counts and signals error conditions. In addition, RTQC calculates registration and collimation errors and reassigns radar sort boxes in the event of radar failure and/or recovery. The subprograms and subroutines to be migrated are:

RCA	RFR	RRA
RSO	SOU	

Figure D-6 is a list of the data tables that must be migrated along with the Option B subprograms and subroutines.

d. OFFLOAD BENEFITS

Present indications are that implementation of the new IOCEs will provide the following primary benefits:

	Option A	Option B
- CCC Computer Capacity Recovered	10-15%	40-45%
- SE Storage Words Recovered	88K	92K

As stated earlier, Options A and B are independent of each other.

Option B - Table Migrated

AB	RDAM Base Address Control Table
AL	Altimeter Data Table
AM	Altitude Display Filter Table
BE	Beacon Code Array
BR	Weather/Strobe Formatting Control Table
BT	Beacon Code Replacement Lists Array
BX	Weather/Strobe Data Index Table
CM	RTQC Corrections Factors Table
CN	Coordination Fix Table
CQ	Category/Function Communication Table
CS	RTQC Communications Table
DH	Radar Target Batching Table
DJ	Display Data Availability List Table
DM	Selected Beacon Code DCC Addressing Table
DN	Selected Beacon Code DCC Index Table
DW	RDA Delete Control Array
FG	Failed Radar Sort Box Table
GA	Extended Sector Array
GB	Sector Boundary Pairs Table
GC	Extended Sector Boundary Table
GW	Extended Sector Boundary Work Table
HA	Radar Sort Box FPA Chain Array
HF	Track-Numbered Display Table
HO	Track Control/Display Table
HP	Plan View Display Table
HR	Registration Data Table
IR	Automatic Track Initiation Point Table
IT	List Display Data Table
JA	Radar Data Counts Table
JB	Beacon Test Message Table
JT	IOCEP Pointer Table
JI	CBC Request Table
JN	PVD Constant Table

FIGURE D-6

JO	PVD Code List Table
JR	RIN Beacon Code History Synchronization Table
QA	Quick Action Key Translation Table
QE	Registration Error and Constants Table
RG	Radar Sort Box Table
RM	Radar Simulation Table
RQ	Correction/Tracking Radar Sort Box Table
RS	RSO Site Work Area Table
RT	Radar Data Table
RTD	Dynamic Simulation Radar Data Table
RU	Radar Site Data Table
RW	Simulation Miscellaneous Table
SG	Simulation Radar Sort Box Array
SS	Strobe Message Display Table
TE	Track Sort Box Index Array
TH	Tracking Data Table - Part 2
TK	Tracking Data Table - Part 1
TW	Tracking Miscellaneous Table
WR	Radar Formatting Control Table
WS	Weather Data Table
WX	RDAM Radar Index Table

FIGURE D-6. (continued)

In addition, some other gains that would be achieved are:

- Increased Availability for Additional Functions
- Increased CE Availability for Scheduled Maintenance
- Supports Configuration Options for Transition
- Low Buffering for CE Executed Functions

Calculations for storage and capacity recovered are based on 1975 data. Storage recovery estimates are based on the Resource Buyback System and on Site Adapted Data for the UDS. Capacity estimates are based on "SYSTEM PERFORMANCE ANALYSIS REPORT, SPAR 70" 10 October 1975.

SPAR 70 contains measurements relative to CPU utilization for the Houston ARTCC. Measurements include number of executions per minute and mean time per execution (in milliseconds) for each NAS Program Element. From these measurements the percent CPU utilization for each NAS Program Element was calculated as follows:

$$\% \text{ CPU/PE} = \left(\frac{\text{EPS} \times \text{MTE}}{1000}\right) \times 100$$

where: EPS = Executions per second per program element

MTS = Mean Time per Program Element Execution (msec)

The percent CPU utilization thus calculated can then be used to determine the total CPU utilization for the sample period as follows:

$$\text{Total \% CPU} = \sum_{i=1}^{n} (\% \text{ CPU})_i$$

where: n = total number of Program Elements Executing during the sample period.

In the case of the Houston ARTCC, total % CPU utilization was found to be 173.71%. This can be interpreted to mean that the NAS operational program required 1.73 computational seconds per second of real time. Obviously those could only have been accomplished through the use of multiple compute elements. These measurements and calculations obtained from the Houston ARTCC were used as a basis for estimating the CPU capacity saving that could be realized due to offloading NAS program elements into the new IOCE.

As previously stated, the criterion used for a software offloading strategy (Options A or B) was to select subsystems that logically shared a common purpose and given data bases. This was done in order to minimize the new IOCE's accesses to main (SE) memory and, hopefully, minimize the number of programs that will require major modifications.

The algorithm used to estimate CPU saving for each option is as follows:

$$\% \text{ CPU Savings} = \left(1 - \frac{TCPU - \sum_{i=1}^{n} (PECPU)_i}{TCPU} \right) \times 100$$

where:

TCPU = Total CPU Time as calculated from SPAR 70 (1.74 sec/sec)

PECPU = Program Element CPU times as derived from SPAR 70 (sec/sec)

n = Number of Program Elements in each Option

Main (SE) memory saving was estimated by summing the number of words for each program and table migrated to the new IOCE.

See Appendix A for pertinent calculations.

E. IMPLEMENTATION

1. SEQUENCE

Upgrade of the field systems would be determined by order of need as determined by ATF-1. The initial testing of 4341 replacement units would require hardware system test at the FAA Technical Center. Software conversion and checkout would also be accomplished at the FAA Technical Center. The software conversion and checkout would include checkout of instruction set differences.

In addition, a field deployment transition plan would be developed and tested at the FAA Technical Center for eventual use at the field sites. The sequence of field deployment would be 9020A sites followed by the 9020D sites.

The following major actions can be anticipated in the IOCE replacement effort:

Hardware

- Detail design of 4341 IOCE modifications
- Design verification and component release
- Component manufacture
- 4341 IOCE fabrication and factory test
- Receive 4341 IOCE at FAA Technical Center
- Integrate with 9020 at FAA Technical Center
- System test at FAA Technical Center

Software

NAS

- Design changes
- Code changes
- String test
- System test--FAA Technical Center
- Site adaptation, integration
- Site test

VM/370

- Design changes
- Code changes
- String test
- System test--FAA Technical Center
- Site adaptation, integration
- Site test

Education

- Service engineer training
- Software engineering training

Documentation

- Hardware
- Software

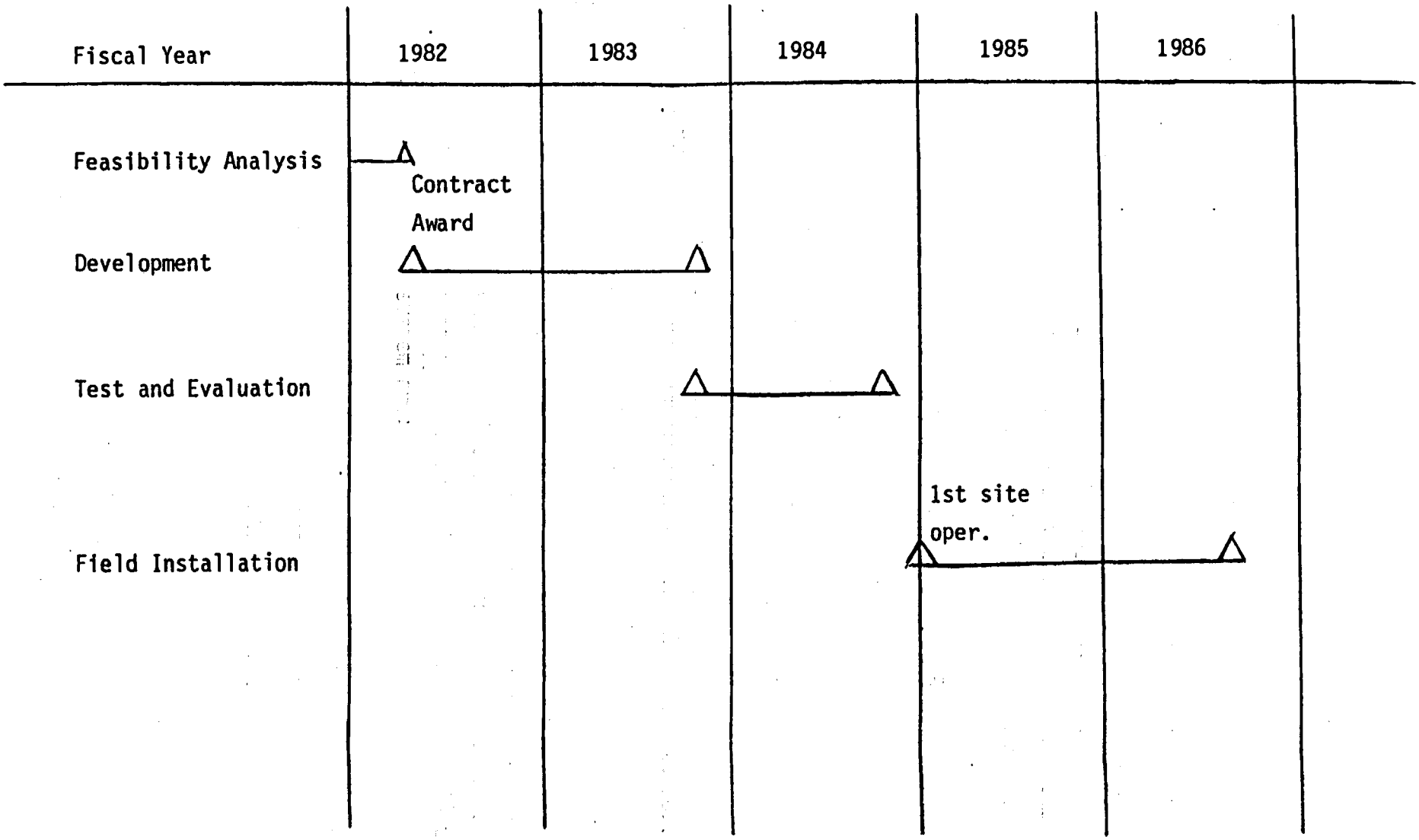
2. SCHEDULE

A tentative schedule for implementation is shown in figure E-1. It indicates a time span of approximately 33 months from contract award until the first ARTCC would become operational. The schedule also assumes a site per month becoming operational thereafter. It is assumed that Option B could be accomplished in the same time frame if substantial additional software resources were applied to the effort.

3. COST

The cost of the replacement of the IOCEs at 20 centers plus provisions for two systems each at the Technical Center and at the FAA Academy is estimated at $100.9 million for "Option A" and $113.3 million for "Option B."

A breakdown of the total cost estimates is as follows:



IOCE Replacement Schedule

FIGURE E-1.

	Option A	Option B
Hardware Cost	$62.6M	$62.6M
Development Cost	16.8M	25.8M
Initial Site Costs	12.5M	12.5M
Technical Center Costs	9.0M	12.4M
Total Costs	$100.9M	$113.3M
CCC Computer Capacity Recovered	10-15%	40-45%

a. HARDWARE COST

The total IBM hardware costs will be the cost of 24 complete systems: 20 (Centers) and two (FAA Academy) and two (FAA Technical Center). Each of these complete systems requires the hardware units in the quantities indicated in table E-1. The cost of a modified 4341 IOCE is estimated at 500K. The cost of the basic IBM 4341 is $350K. The additional cost is for the hardware modifications to the basic IBM 4341 to perform the functions of the IOCE, and any hardware modifications to other system units which might be necessary to work with the modified 4341 or the higher speed/capacity disks and tapes.

Table E-1: Hardware Cost Breakdown Per System(ássumed configuration)

Quantity	Model	Description	Unit Cost	Extended Cost
3	IBM 3830	Disc Control Unit	$70K	$210K
12	IBM 3350	Disc Drive	$40K	$480K
3	IBM 3803	Tape Control Unit	$40K	$120K
12	IBM 3420	Tape Deck	$25K	$300K
3	IBM 4341	IOCE	$500K	$1500K
			Total per system	$2610K
			Cost of 24 systems	$62.6M

b. DEVELOPMENT COST

The development costs are composed of one-time contract engineering changes for hardware and software development

and initial site installation charges. Table E-2 shows the development costs for Option A and Option B.

The software development costs for Option A were derived from the migration of 77,000 program words and 11,000 table words for a total of 88,000 words. For Option B there are 30,000 program words and 62,000 table words, for a total of 92,000 words. However, the effort of migrating the code for Option B is much more complex than for Option A. Therefore, the cost of accomplishing Option B is significantly higher than the cost of accomplishing Option A.

The installation costs are estimated at $200K per site. This figure assumes a five man installation team at a site for one month.

Table E-2: Development Cost Breakdown

	Option A	Option B
Engineering Charges		
Hardware	$3M	$3M
Software	$9M	$18M
Installation Costs	$4.8M	$4.8M
Total	$16.8M	$25.8M

c. INITIAL SITE COSTS

The initial site cost is composed of one-time charges for site preparation, start-up maintenance, and training. A breakdown of these costs are shown in Table E-3.

The site preparation costs are broken down on a per site basis, of $30K to modify the environmental system (humidification, ventilation, and air conditioning) and $5K to modify the

electrical power and grounding. Thus, there is a cost of $35K for each of 23 installations.

The start-up maintenance costs include the cost of initial spares at each center and the academy and the cost of developing a repair test bed and documentation updates at the Depot. The initial spare costs are estimated at 10 percent of the hardware cost of each site, and the initial Depot costs are estimated at 16 percent of the hardware cost at one site. There is no start-up maintenance cost at the Technical Center. The spares are provided under the IBM support contract already in existence.

The training costs are based on training 46 Airway Facilities personnel from each center and 75 personnel from the Academy and Technical Center for a period of 10 weeks. The cost is estimated to be $250K per site for 22 sites.

Table E-3: Breakdown of Initial Site Cost

	Option A	Option B
Site Preparation	.8M	.8M
Maintenance Cost	6.2M	6.2M
Training	5.5M	5.5M
Total	$12.5M	$12.5M

d. TECHNICAL CENTER COST

The Technical Center costs are composed of manpower charges for project personnel and direct support personnel. The project personnel would be involved with feasibility analysis, contract technical administration, test and evaluation, and field support during implementation. The direct support

personnel would be involved in operations of the current 9020 system and the IOCE replacement system, and in supporting the test and evaluation activity by providing data reduction and analysis software and in developing simulation software. Table E-4 is a summary of the Technical Center manpower required to support the IOCE replacement effort.

The estimated cost for the Technical Center personnel is $9.0 million for Option A and $12.4 million for Option B.

Table E-4: Technical Center Manpower Requirements

Project Support Skills

	FY82	FY83	FY84	FY85	FY86
EE	8	12	6 (8)	2 (4)	2 (4)
CSA	9	15	13 (20)	7 (12)	7 (12)
Programmer	3	3	3 (6)	3 (4)	3 (4)
Technician	2	2	2		
ATCS		3	3		
Math		2	2 (4)		
Direct Support Personnel	4	5	12 (16)	12 (20)	12 (20)
Total	26	42	41 (54)	24 (40)	24 (40)

*Numbers in parenthesis ( ) represent requirements if Option B is selected.

F. SUMMARY

Technical Analysis of the IOCE Replacement philosophy indicates a potential improvement in NAS system operation in the following specific areas:

- Reduced CE Load - Increased processing capabilities of 10-15% for Option A and up to 40% for Option B. Options A and B are stand alone software strategies and can be implemented independently. While the yield of Option B (40%) is significantly greater, the implementation effort and risk are also significantly greater.

- Increased Channel Capacity - Channel capacity can be doubled with a potential aggregate data rate increase of ten times the present I/O data rate.

- System Reserve - Offloading of software modules for processing in the IOCE Replacement unit will provide a potential reserve for implementation of new NAS System functions (ETABS, DABS, etc). The extent of the reserve would depend on the software strategy chosen (Option A or B) and the results of an additional study to calculate the effect of the migrated software features.

Schedule and cost estimates can, at this point, be only rough calculations based on assumptions. Preliminary costing would indicate a cost in the neighborhood of $100 million for acceptance and implementation of Option A. Due to increased complexity, and risk, Option B costs would be approximately $115 million. Time estimates range from 30-36 months from implementaiton at first site to 50 months for total implementation.

APPENDIX A

Option A
Offloaded Tables

Name	Words Per Entry	Number of Entries	Size (words) Fixed	Site Adapt. Var.
AR	3	338		1014
AS	1	24		24
AZ	1	35		35
BB	1	5		5
BQ	1	40		40
BS	3	1	3	
CB	1	127		127
CN	1	550		550
DD	1	1		1
DZ	20	50		1000
EA	3	14		42
EF	1	36		36
FF	1	1521		1531
GT	7	1	7	7
JU	1	142		145
JV	1	71		73
KK	9	550		4950
LI	9	2		KK Overlay
MV	3	328		984
NG	1	550	550	
PN	1	121	121	
RD	5	15		75
RI	4	1	4	
RQ				KK Overlay
RV	½	48		24
RX	11	1		N/A
SL	2	15		30
SQ	8	1		N/A
SX	300	1		N/A
SZ	1	39		39
TA	2	104		208
TN	2	42		84
TP	1	43		43
TS	3	1		N/A
			685	11060

Total 11,745 Words for Table Migration
Total 77,255 Words for Program Migration
Based on RBB Development Plan
1975
Site Adapted Data: Based on UDS
Total Words Migrated (Programs and Tables) = 88,000 Words

Option "A" Programs
Percent CPU Utilization

PDC	0.710
DUZ	13.268
DAM	1.295
DDM	0.656
DFP	1.327
DRS	0.357
PDE	2.013
PAS	1.101
PNA	0.642
PCE	1.019
PTY	0.273
	20.648 = .206 Sec/Sec

Total CPU Utilization 173.71 = 1.74 Sec/Sec

Savings Due to Offloading

$$\left(1 - \frac{1.74-.206}{1.74}\right) \times 100 = 11.83\%$$

Based on SPAR 70 available data

Option B
Offloaded Tables

Name	No. Words Per Entry	No. Entries	Size (words) Fixed	Site Adapt Var.
AB	15	1	15	
AL	26	24		624
AM	1	8	8	
BE	½	4096	2084	
BR	2	4	8	
BT	1	16	16	
BX	1	144		144
CM	3	12		36
CN	1	550		550
CQ	8	1	8	
CS	10	12		120
DH	1	13	13	
DJ	38	1	38	
DM	3	605		1815
DN	1	2048		2098
DW	¼	3328		82
FG	1	1394		1394
GA	½	29		15
GB	1	406		406
GC	2	921		1842
GW	2	921	1842	
HA	½	711		356
HF	2	1050		2100
HO	16	700		11200
HP	15	12		180
HR	2	240		480
Subtotal			3996	24142

Option B (Continued)

Offloaded Tables

Name	No. Words Per Entry	No. Entries	Size (words) Fixed	Site Adapt Var.
IR	1	60		60
IT	6	320		1970
JA	6	60		380
JB	3	100		300
JT	2	200		400
JI	9	50		450
JN	2	15		30
JQ	43	12		516
JR	30	2	60	
DA	15	1	15	
QE	1	339	339	
RG	1	1394		1394
RM				1500
RQ	1	1394		1394
RS	80	12		960
RT	7	1210		8470
RTD	7	100		700
RU	22	13		286
RW	8	1	8	
SG	¼	1394		349
SS	4	100		400
TE	½	1470		735
TH	9	700		6300
TK	9	700		6300
TW	22	1	22	
WR	2	14	28	
WS	3	100		300
WX	1	364		364
	Subtotal		1012	33008
	Total (first and second pages of Option B)		5008	57150

Total 62,158 Words for Table Migration
Total 29,845 Words for Program Migration
Based on RBB Development Plan
1975
Site Adapted Data Based on UDS
Total Words Migrated (Programs and Tables) 92,000 Words

Option "B" Programs

RAT	4.638
RFA	3.697
RSL	1.414
RTG	8.471
RRA	0.702
RSO	0.519
CRJ	3.394
HCI	0.934
HHM	4.291
HRD	0.196
HTI	22.496
HTM	0.732
RDA	12.196
CBC	2.386
JQB	0.277
JGN	2.573
JQP	0.297
JQR	0.355
JQU	0.561
JTA	0.299
JTI	0.244
JTU	0.466
	71.499 = 715 Sec/Sec

Total CPU utilization 173.71 = 1.74 sec/sec

Saving due to offloading

$$\left(1 - \frac{1.74 - .715}{1.74}\right) \times 100 = 41.09\%$$

Based on SPAR 70 available data