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AUTOMATION EQUIPMENT DEVELOPMENT FOR THE EN ROUTE AUTOMATED RADAR TRACKING SYSTEM (EARTS) DISPLAY RECORDING

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PROJECT PLAN

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1. OBJECTIVES.

Determine what is required in order to interface a radar display recording and playback system with En Route Automated Radar Tracking System (EARTS) offshore centers.

Develop, fabricate, and test a breadboard model at the Federal Aviation Administration (FAA) Technical Center.

Provide a coordination draft specification, a compilation of test data, and a technical data handoff package to ARD-113.

2. BACKGROUND.

Because the FAA has a need to re-create or replay on demand air traffic histories for operational or incident analysis, a breadboard model of a subsystem to record, store, and reproduce air traffic control data displayed on the National Airspace System (NAS) en route Plan View Display (PVD) was designed, fabricated, and tested at FAA Technical Center by ACT-230 personnel. The successful completion of the breadboard model was followed by the design and fabrication of an engineering model of the system called En Route Radar Display Recording/Playback System (ERDIRS).

The same requirements for a recording and playback system exist for the EARTS. Interfacing the existing ERDIRS system with EARTS would require such an extensive redesign that this approach would be impractical. It was decided, that the design and fabrication of a separate breadboard record/playback subsystem for EARTS would be the best approach.

3. RELATED DOCUMENTATION/PROJECTS.

3.1 RELATED PROJECT: ERDIRS

3.1.1 ERDIRS Documentation:

"A Breadboard Model Used To Demonstrate The Feasibility of Recording National Airspace System En Route Display Data," FAA-RD-78-97, September 1978.

"ERDIRS Engineering Model System Design Data," April 1980.

"Draft Specification: ERDIRS," April 1980.

3.1.2 EARTS Documentation:

"Specification: EARTS," FAA-E-2592a.

"EARTS System Design Manual," ATC 24,000.

"ATC Hardware Design Data," ATC 21,000.

"EARTS IBAG Technical Manual," Volume 1, PX12103-1.

"EARTS IBAG Technical Manual," Volume 2, PX12103-2.

"EARTS IBAG Technical Manual," Volume 3, PX12103-3.

"IOP-B Technical Manual," Volume 1, PX12096-1.

"IOP-B Technical Manual," Volume 2, PX12096-2.

"Preliminary General System Manual for the Alaska EARTS," PX10753.

"Integrated Circuit Technical Manual," PX12107.

"EARTS Coding Specification," ATC 24007.

"Technical Manual for EARTS DPS," PX12094-0-1.

4. SYSTEM EQUIPMENT DESCRIPTION.

The first task in the design of a record/playback system for the EARTS display data is to determine a pickoff point (1) from which it is feasible to take data and (2) from which all of the display data is available. Each Interface Buffer Adapter Generator (IBAG) in the system can drive up to six displays. Each IBAG contains three Display Drawers (DD) each of which drive two displays. Each DD contains two Refresh Buffer Memories (RBM) and two Vector Generator and Control (VGAC) units. Each RBM-VGAC combination drives one display. All of the refresh data for one display is available 55 times a second on the RBM bus between the RBM and the VGAC. The beginning of a refresh period can be detected by decoding the Start of Display/ End of Display (SOD/EOD) word on the RBM bus. The bus data and appropriate control lines are available on the wire wrap terminals on the rear of the DD. There are a number of empty card slots in each DD. An interface card can be inserted into each DD and can be used to control the output of refresh data from a selected display without interfering with the normal operation of the system. Each interface card will multiplex data from two RBM buses. By using three-state output drivers, the output of the interface cards from three DD's can be tied together. This provides one common output bus from each IBAG that contains the multiplexed refresh data from six displays.

There is room within each DD to run a cable from the backplane connection of the interface card to the back panel of the DD. A connector mounted on the rear panel of each DD can be used to connect a cable which routes the refresh data to the IBAG chassis. The signal lines from three DD's can be connected together at one common IBAG output connector as shown in figure 1.

In the breadboard model, the portion of the record/playback interface that is external to the IBAG will be designed to receive refresh data from six PVD's through one IBAG.

By adding identical input interface sections, it will be expandable to handle refresh data from up to 24 PVD's through 4 IBAG's (figure 2). However, only one DD in one IBAG will be modified in order to minimize the initial NCP

requirement. Therefore, display data from two displays will be recorded. By simply modifying two additional DD's, the data from six displays could be recorded.

A 4K by 32-bit high speed random access memory (RAM) will be utilized to store a complete refresh from a selected display. The display data will then be output from the RAM at the relatively slow speed required by the magnetic tape recorder.

During the record operation, refresh data will be received through the interface and stored on tape. However, the data will be played back as update information and will be input to the DD through the interface between the Input/Output Module (IOM) and the Display Module (DM), both of which are contained in the IBAG. This interface is accessible on the DD from two external connectors. Data will be reformatted as update data, and the appropriate control words and control signals will be generated during playback. Figure 3 shows the data formats for record and playback. Figure 4 shows a tentative format for tape data. Figure 5 shows the preliminary playback interface.

In addition to the above record/playback interface design, a considerable effort will be required in order to select and acquire a suitable high density (HD) or medium density (MD) magnetic tape recorder.

5. DATA COLLECTION.

A test bed will be established which will simulate the refresh interface contained in the IBAG. Various test patterns will be coded using standard EARTS display word formats, and will be stored in memory. These display patterns will be output to the record/playback interface which will record the data on magnetic tape. Later the data may be played back through a DD to a PVD.

The test bed will utilize the existing direct memory access (DMA) device interface and the TM 990/101M microcomputer located in the display lab (figure 6).

The device select code for the display control vector generator (DCVG) device controller (which is connected to the DMA interface) will be stored in the control byte location in memory. With the DCVG disconnected from the system, the DCVG request line is held at a high logic level. The data is transferred from memory utilizing the DCVG interface. Various control signals from the DCVG interface will be used as inputs to the EARTS tester interface cards. The same device select line will be used for the DCVG and EARTS interface cards. The EARTS tester interface will be transparent to the DMA interface.

The tester interface will be operated in a single or dual update mode which will switch back and forth between two different display patterns at various selectable time intervals.

Data will be output at either a 250 or 720 kilohertz (kHz) word rate.

All data will be checked for parity errors. Output data will be observed on the PVD.

The test bed will have the capability of storing various test patterns either on cassette tapes or on erasable programmable read-only memory (EPROM) for more permanent storage.

6. DATA REDUCTION AND ANALYSIS.

The final product will be a breadboard model of a record/playback system for the EARTS display data. The system will be demonstrated by recording live display data, and then playing it back and reproducing the data on a playback display.

A specification and technical data package will also be provided.

7. INSTRUMENTATION AND FACILITIES.

a. The Display Engineering Lab Facilities including available test equipment and PVD.

b. One IBAG Display Drawer — required to debug, checkout, and test record/playback system.

c. HD or MD Tape Recorder.

d. EARTS System — for final system checkout and demonstration, and for NCP modification and checkout.

8. COORDINATION AND AREAS OF RESPONSIBILITY.

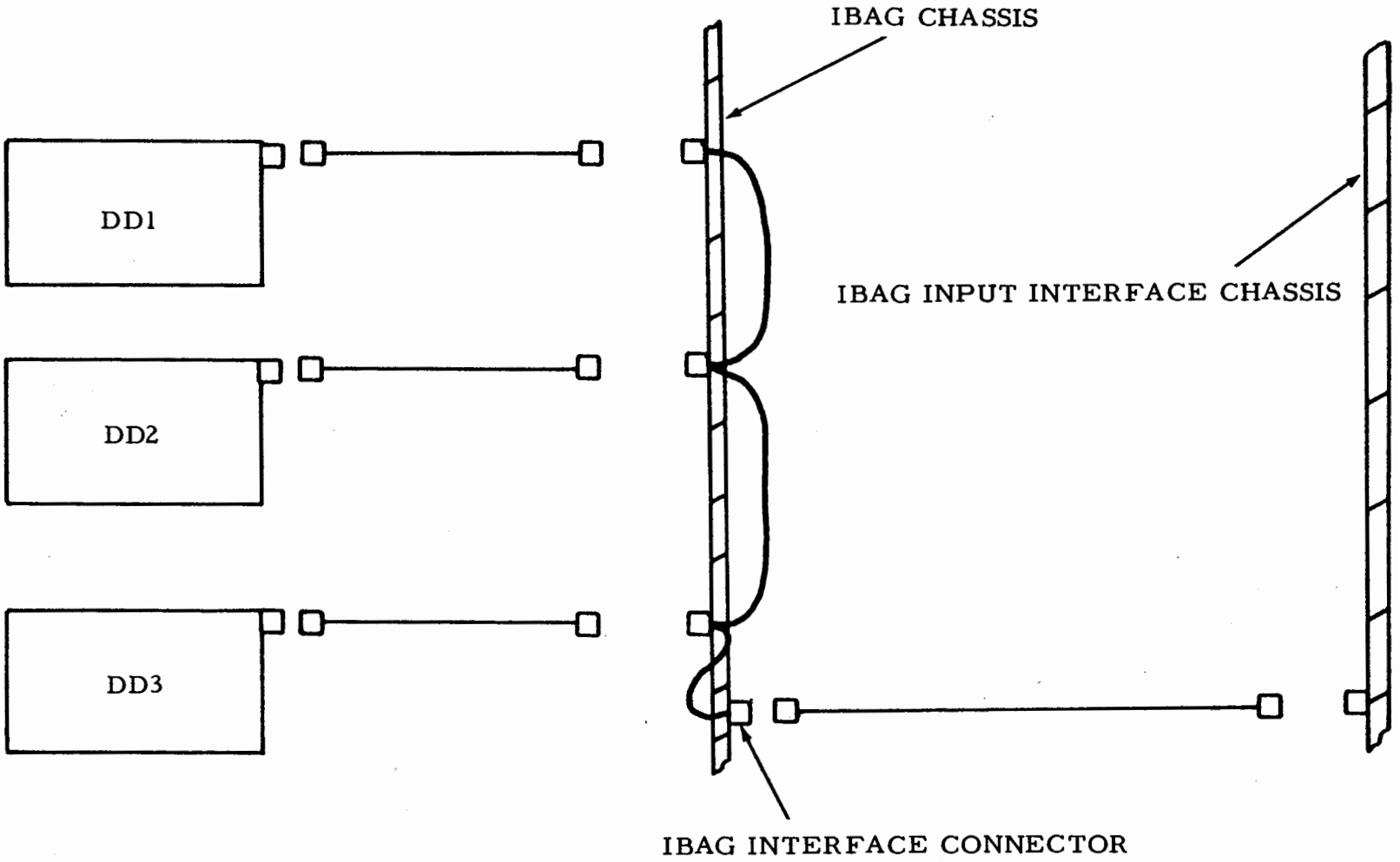
Primary Responsibility: ACT-230

Support: AAF-363, AAF-364, ACT-731, ACT-734, and Univac

Contacts: FAA, Oklahoma City, and EARTS Field Sites

9. MILESTONE SCHEDULE.

The milestone schedule is found in figure 7.



CONNECTOR ADDED TO EACH DD

INTERNAL CABLE ADDED FROM EACH DD TO IBAG CHASSIS

FOUR CONNECTORS ADDED TO IBAG CHASSIS. COMMON LINES WILL BE JOINED AND THEN CONNECTED TO IBAG INTERFACE CONNECTOR.

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FIGURE 1. IBAG INTERNAL CONNECTOR MODIFICATIONS

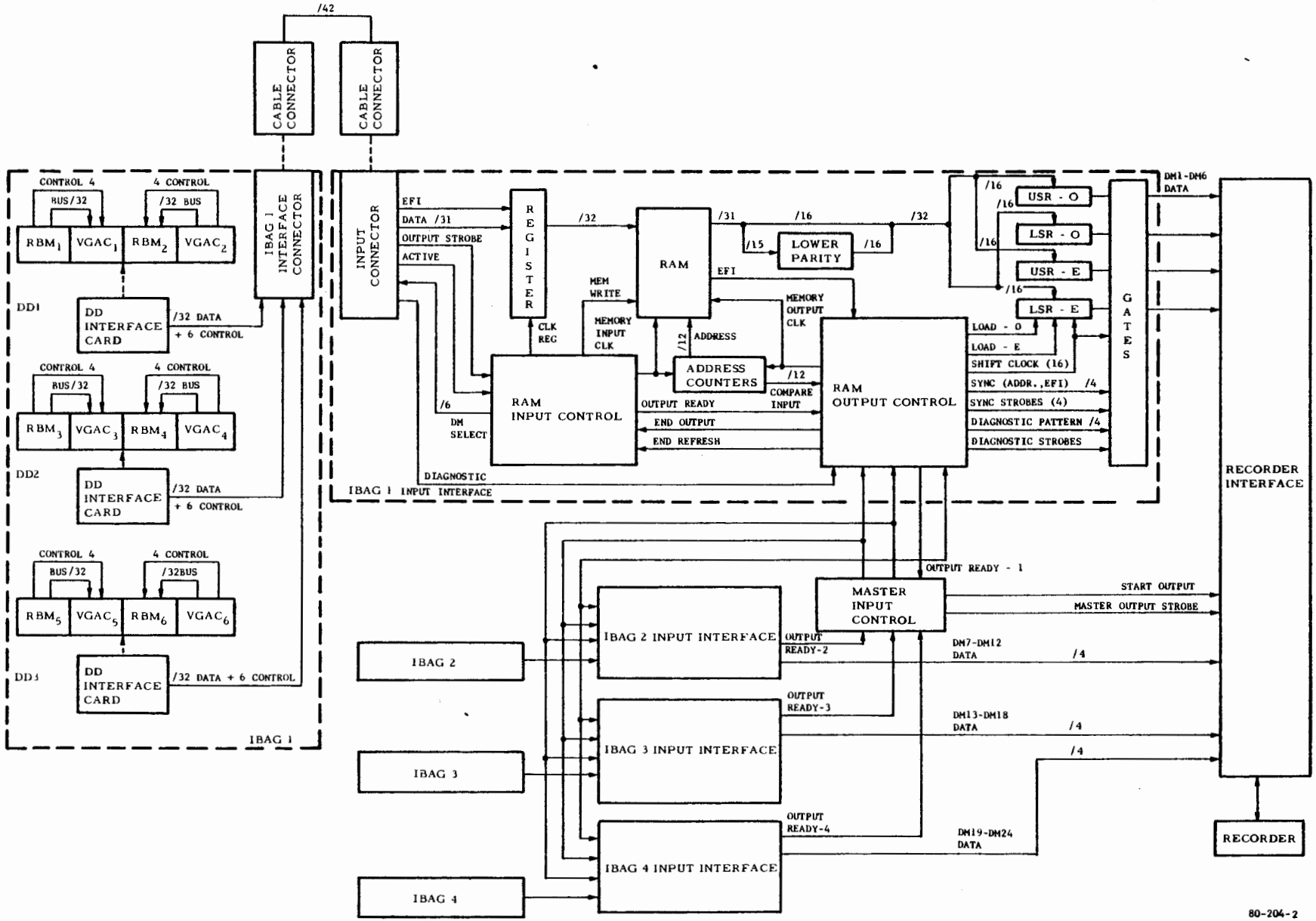

FIGURE 2. EARTS RECORD INTERFACE

STORAGE OF REFRESH DATA ON MAGNETIC TAPE

I. DETECT START OF REFRESH

II. STORE DATA ON DIGITAL RECORDER

BLOCK 1

EOD/SOD WORD
TEST VECTOR
DATA
"
"
"
EOS WORD — REMOVE EOS WORD WHEN DETECTED

BLOCK 2

DATA
"
TO "
"
EOS WORD — REMOVE EOS WORD WHEN DETECTED

(PACK NEXT TO LAST WORD OF PREVIOUS BLOCK)

BLOCK N

DATA
"
"
"
EOS WORD — REMOVE EOS WORD WHEN DETECTED

(PACK NEXT TO LAST WORD OF PREVIOUS BLOCK)

III. DETECT END OF REFRESH

IV. ADD EOS WORD TO END OF REFRESH DATA

NOTE: DURING PLAYBACK THE DATA WILL APPEAR AS ONE LARGE BLOCK

PLAYBACK OF STORED REFRESH DATA ON UPDATE INTERFACE

I. GENERATE EF3 WORD (SETS MEMORY START ADDRESS. ALTERNATES BETWEEEN UPPER AND LOWER MEMORY.)

II. GENERATE P STACK WORD (MEMORY START ADDRESS IS SAME AS FOR EF3 WORD SINCE THERE IS ONLY ONE DATA BLOCK. THIS P STACK WORD REFERENCES ITSELF.)

III. PLAYBACK OF DATA FROM DIGITAL RECORDER

EOD/SOD
TEST VECTOR
DATA
"
"
"
EOS WORD

(THIS DATA IS LOADED INTO THE RBM.)

IV. GENERATE EF5 WORD (THIS WORD STARTS THE REFRESH MODE. DATA IS NOW SENT TO THE UGAC AND THEN DISPLAYED ON THE PVD.)

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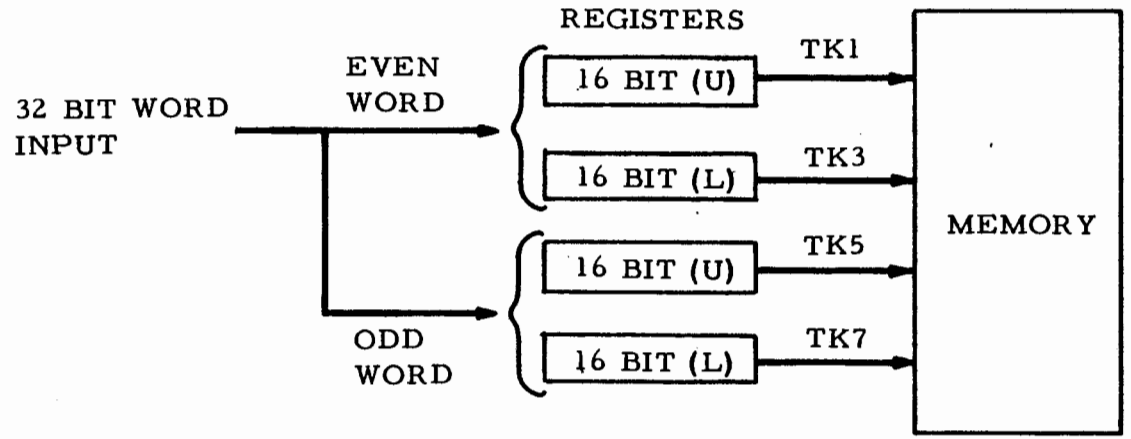
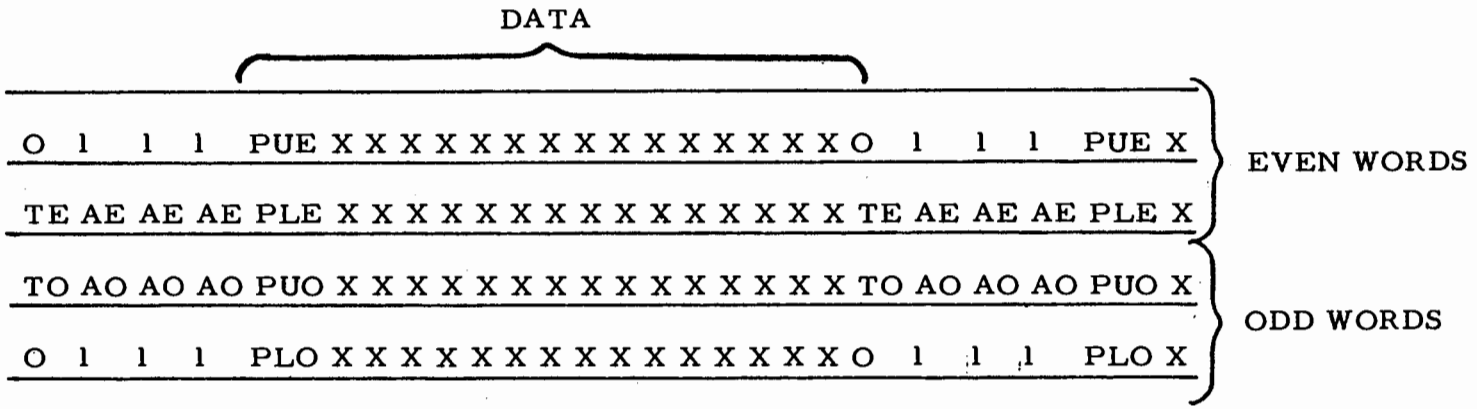
FIGURE 3. DATA FORMAT





AE	EVEN WORD DM ADDRESS
AO	ODD WORD DM ADDRESS
T	WORD TYPE (EF OR DATA)
P	PARITY FOR EACH HALF WORD

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FIGURE 4. TAPE FORMAT

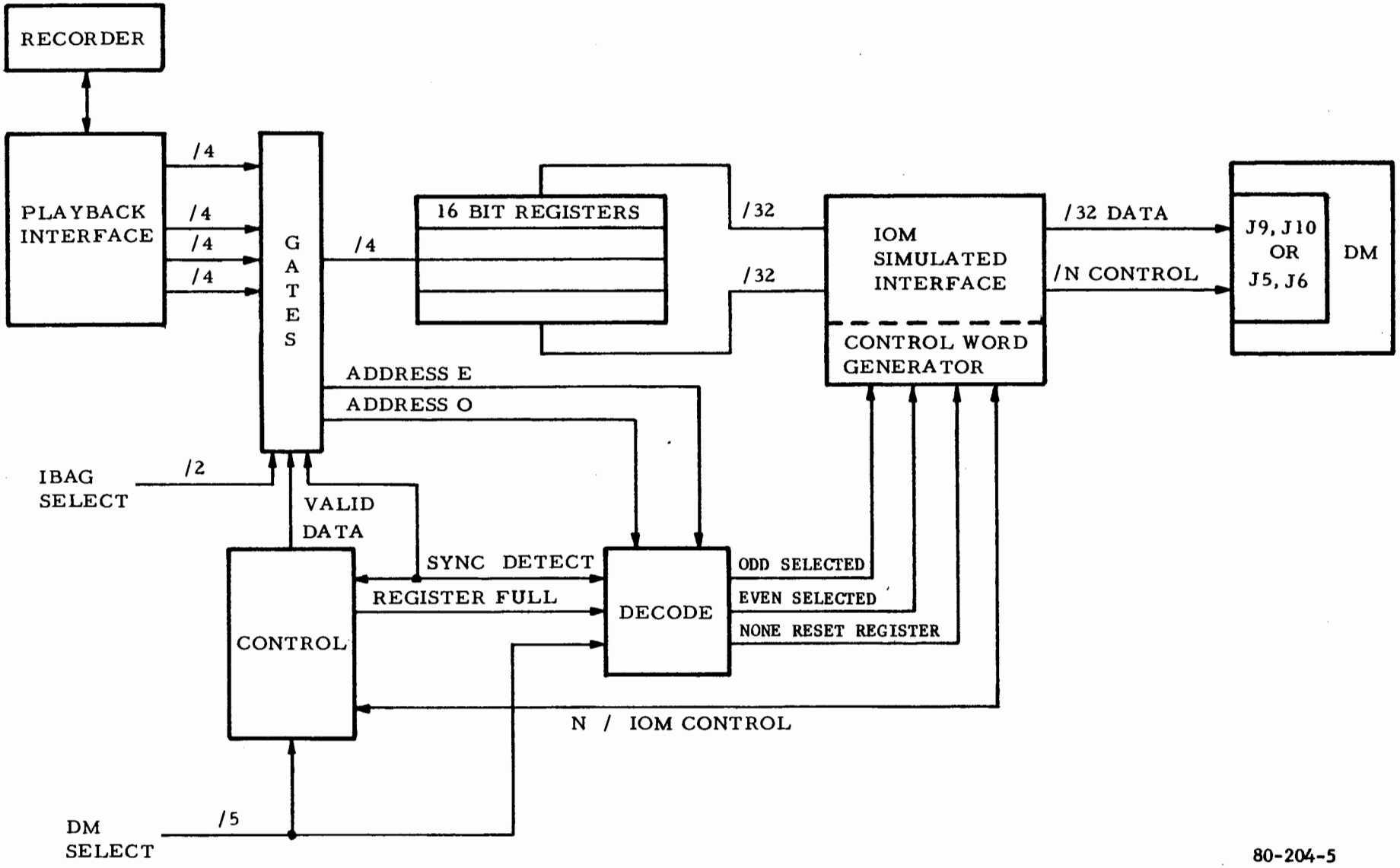

FIGURE 5. IBAG PLAYBACK INTERFACE USING UPDATE DATA

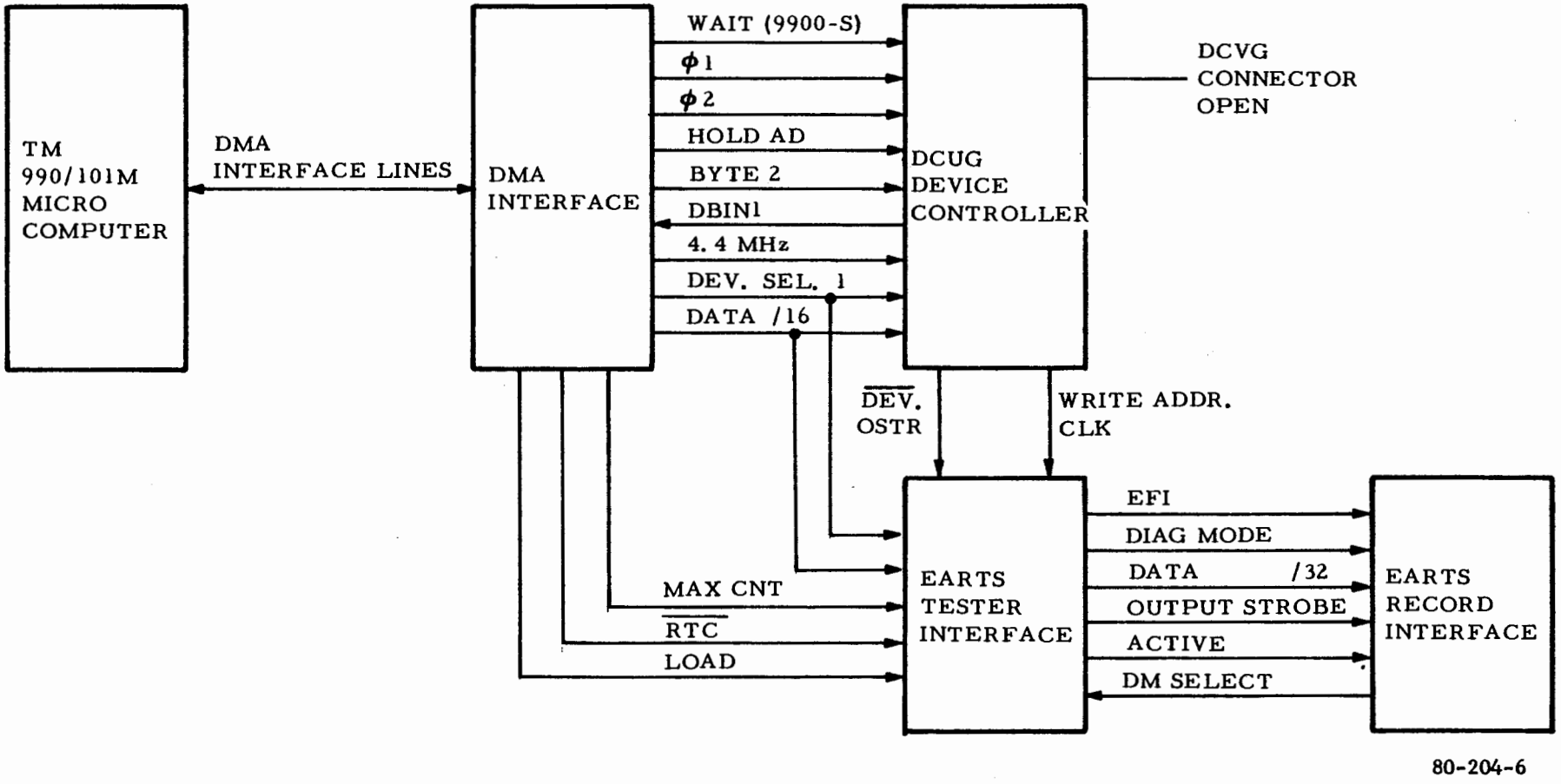

FIGURE 6. TEST BED FOR EARTS RECORDING

SECTION 9 - MILESTONE SCHEDULE

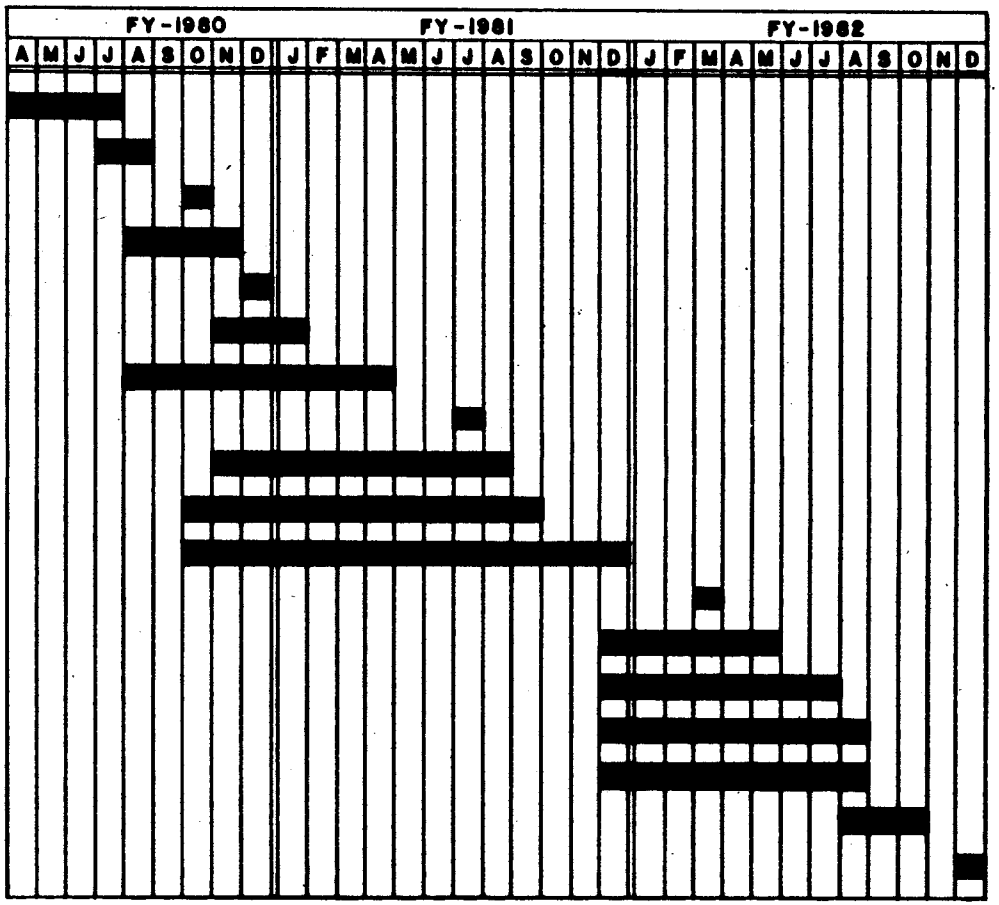

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FIGURE 7. MILESTONE SCHEDULE