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A Report to the ITS Standards Community
ITS Standards Testing Program

FINAL TEST REPORT

For Advanced Transportation Controller Type 2070 (ATC 2070) and the Intelligent Transportation Systems (ITS) Roadside Cabinet as Deployed by Harris County, Texas

By

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Prepared for

USDOT – ITS Joint Program Office

Battelle Work Order: BA34020
Task No.: 6.2

June 27, 2008

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Technical Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle Final Report for ITS Standards Testing of ATC 2070 and ITS Cabinet as deployed in Harris County, TX		**5. Report Date** June 27, 2008 **6. Performing Organization Code**
7. Author(s) Wilton Alston (Battelle) and Thomas Timcho (Battelle)		**8. Performing Organization Report**
9. Performing Organization Name and Address Battelle Memorial Institute 505 King Ave. Columbus, OH 43201		**10. Work Unit No. (TRAIS)** **11. Contract or Grant No.** DTFH61-02-C-00134; Task BA34020
12. Sponsoring Agency Name and Address United States Department of Transportation ITS Joint Program Office 1200 New Jersey Avenue, S.E. Washington, DC 20590		**13. Type of Report and Period Covered** Final Report **14. Sponsoring Agency Code** HOIT-1
15. Supplementary Notes Mr. Steve Sill (COTM) John Augustine (COTR)		

16. Abstract

This Final Report includes all of the findings and recommendations resulting from Battelle's static review, detailed interviews and onsite testing activity related to the ITS Standards deployed and currently in use for transportation management systems, specifically, traffic signal control, in Harris County, TX. The standards reviewed include the Advanced Transportation Controller Standard for the Type 2070 Controller, v02.03, dated March 12, 2004 and the ITS Cabinet Standard v01.02.17b, dated November 16, 2006.

The outcome of this effort, through a series of both subjective and objective evaluation criteria, is to determine the suitability, effectiveness and interoperability and interchangeability, of the standard, and to provide this feedback to the standards development organizations that are drafting the standards. This testing effort is not an evaluation of the site's conformance to the standard and should not be construed as such.

17. Key Words	18. Distribution Statement		
Intelligent Transportation Systems, ITS Standards, Harris County, ATC, 2070, ITS Cabinet, Advanced Transportation Controller	No restrictions. This document is available to the public.		
19. Security Classif. (of this report)	**20. Security Classif. (of this page)**	**21. No. of Pages**	**22. Price**
Unclassified	Unclassified	290	N/A

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1.0 Introduction

This report provides the results and findings of the ITS Standards Test Program as gathered from both the interview questionnaire and the field testing, and assessment and evaluation of the Advanced Transportation Controller Type 2070 (ATC 2070) and the Intelligent Transportation Systems (ITS) Roadside Cabinet as deployed by Harris County, Texas as part of the Greater Houston Transportation and Emergency Management Center (HCTX). This report fulfils the work product specified in Task 6.2 of Work Order BA34020. This material is based upon work supported by the Federal Highway Administration (FHWA) under contract number DTFH61-02-C-00134. Any opinions, findings, conclusions, or recommendations expressed in this publication are those of the author(s) and do not necessarily reflect the views of the Federal Highway Administration.

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2.0 Background

2.1 ITS Standards Testing Program

The U.S. Department of Transportation (USDOT) has created the Intelligent Transportation Systems (ITS) Standards Test Program, whose objective is to assess a standard's performance and evaluate the ability of the standard to accomplish interoperability and interchangeability in ITS deployments. The ITS Standards Test Team (ISTT) has been contracted by USDOT, in cooperation with the Standards Development Organizations (SDO) and USDOT, to evaluate the coverage and approach used by the site in deploying standards, and conduct both detailed static analysis and hands-on testing of the standard as used at the site.

2.2 Standards of Interest

This report contains the results from the evaluation and field testing of a specific subset of ITS standards applicable to traffic/transportation controllers in the form of the Advanced Transportation Controller and supporting hardware. The primary standards of interest for ITS standards testing in Harris County (HCTX) are the ATC 2070 and the ITS Cabinet. While these standards both continue to be refined, a specific version was chosen for this evaluation. These standards are enumerated in detail in Table 2.1.

Table 2.1. Standards of Interest

Identification	Title	Version	Date
ATC 2070	Advanced Transportation Controller (ATC) Standard for the Type 2070 Controller	02.03	March 12, 2004
ITS Cabinet Standard	Intelligent Transportation System (ITS) Standard Specification for Roadside Cabinets	01.02.17b	November 16, 2006

2.3 The Harris County Site

Harris County (HCTX), as part of the Greater Houston Transportation and Emergency Management Center, has deployed products based on both the Advanced Transportation Controller Type 2070 and the Intelligent Transportation System Cabinet standards. The ATC 2070 and ITS Cabinet provide the physical connection to intersection control signals and sensors, such as inductive loops and traffic signals, and provide command and control of hundreds of intersections in the Greater Houston area, with Ethernet connectivity and monitoring at Houston HCTX's offices, where data is collected and warehoused.

The site lead for this effort was Mr. Ron Johnson. Mr. Johnson is the Quality Control manager for the traffic division of Harris Co., where he is intimately involved in the County's procurement, installation, and maintenance of ATC-based intersections. In addition to this current role, Mr. Johnson was previously the Chief Engineer for one of the major 2070 controller

vendors. He has been involved in the standard process for nearly 20 years, starting with several of the early NEMA devices and continuing to this day as an active participant in the ATC 2070, ITS Cabinet, and ATC v5.2b standards.

Supporting HCTX as their software integrator, as well as a vendor of ATC and ITS Cabinet hardware, is ITS Siemens. Mr. Dave Miller represented Siemens, and, similar to Mr. Johnson, has numerous years in the standards development process.

Lastly, Mr. Herasmo Iniguez, who represented the ATC working groups, but is also a chief engineer with the California Department of Transportation, was a participant and witness to the activities. Mr. Iniguez, in addition to being an expert with the ATC 2070 application software and environment, is responsible for overseeing CalTrans testing and acceptance procedures for ATC-related products.

These three individuals collectively bring more than 50 years of experience to this standards development process and clearly could be considered subject matter experts in this area.

3.0 Standards Testing – Overview

3.1 Scope of the Test

These tests address the specific observable and testable features of the two ITS standards as they are embodied in the intersection control as deployed in Harris County. The test is not a system acceptance test or stress test, which seeks to compare behavior of the test items to functional or contractual requirements. Rather, this test seeks to compare the usage of the test items to their intended usage described in the standard and identify the reasons for any variations.

3.2 Testing Goals

The overall goal of the ITS Standards Testing Program is to assess and evaluate the suitability, effectiveness, interoperability and interchangeability of ITS standards. To best focus on the process to assess and evaluate ITS standards, the test team has identified these three key elements as essential in understanding whether or not a particular standard is ready for field use. These three high-level categorical elements for assessment and evaluation are defined and expanded in the following discussion.

3.2.1 Suitability

The dimension of suitability addresses those aspects of a standard that make it appropriate for a given purpose, easy to understand and use, or the contrary. This also includes issues and measurements relating to a standard's completeness and coverage when defining all aspects of the problem domain and providing access to, and control of, the appropriate technologies. The impact of an unsuitable standard tends to happen early in the system development life-cycle by needlessly complicating or subverting the choice from suitable alternative standards. The evaluation of suitability will be based on quantitative and qualitative analysis of the standards, structured questionnaire responses, and product capabilities, requirements, and design tradeoffs.

3.2.2 Effectiveness

The dimension of effectiveness addresses those aspects of a standard that make its use an appropriate means to achieve the intended or desired effect. This also includes issues relating to how well the features of the standard enable a reasonable and effective implementation in terms of performance requirements and other such operational and maintenance criteria. The impact of an ineffective standard will tend to happen during design and implementation of the system in terms of excessive resource requirements, negative effects on schedule, product performance, etc. The evaluation of effectiveness will be based on quantitative and qualitative analysis of the standards, structured questionnaire responses, operational use, and results from test trials.

3.2.3 Interoperability and Interchangeability

The dimension of interoperability addresses those aspects of a standard that support the ability of systems to provide services to and accept services from other systems and to use the services so exchanged to enable them to operate effectively together. This necessitates that interoperability goes beyond the mere exchange of data and requires that the data exchanged must be usable by

the other system. Further, interoperability is extended to interchangeability when characterized by standardized interfaces. The impact of standards that do not support interoperability and interchangeability will tend to occur during the integration with other systems. The evaluation of interoperability and interchangeability will be based on quantitative and qualitative analysis of the standards, logical characteristics of any external interfaces, and detailed examination of the syntactic and semantic content exchanged across those interfaces.

3.3 Testing Process Outline

This section presents an outline of the steps followed in the conduct of the ITS standards testing of the ATC 2070 and ITS Cabinet standards. The test process steps outlined in Table 3.1 describe the effort for determining what data and information would be identified and collected and where and how that collection would be accomplished.

Table 3.1. Test Process Steps

Step	Description	Expected Outcome
Establish and Verify Standards Baseline	• Examine implementation and project documentation. • Research and examine standards schemas, compile a list of specific versions, and identify standard and custom implementations.	This process step furnishes what can be termed a "static analysis", which provides an assessment of the content of the standard without regard to how the specific site may (or may not) be using it.
Interview Users, Vendors, and System Integrators	• Conduct structured, guided interviews using a prepared questionnaire developed from examination of the baseline standards content.	This process step provides direct evidence about how a site perceives its use of the standard, particularly in areas where the specifications allowed for flexibility.
Conduct On-Site Testing	• Conduct a controlled experiment using well-defined and documented test conditions. • Test all standard functions and features accessible through the implementation and all exception conditions.	This process step provides direct evidence of how a site (and the vendors to a site) actually used the standard, particularly with regard to deployed devices that ostensibly meet the standard.

3.3.1 Establish and Verify Standards Baseline

This step in the process supplements the baseline knowledge of the standards content. It is an essential step to quantify a site's use of the standard to support the decision to proceed with full test planning and conduct. The test team qualitatively and quantitatively verified the degree of the use and conformance with the standards of interest. This process includes static examination of standards and examination of technical documentation obtained from vendor/developers. This static analysis is the basis for the development of the detailed site interview questionnaire.

HCTX provided a complete package of documentation and specifications as they related to the procurement and implementation of the ATC 2070 and ITS Cabinet. As HCTX is in a somewhat

unique situation, serving as both a deployer of standards-based equipment and also as a major contributor to the standards process, the amount of documentation, other than the specifications themselves, are somewhat limited. As stated by the site, the standards reflect the procurement documentation used to satisfy their needs.

During the initial site survey conducted in February of 2007, physical identification of the equipment (ATC 2070 and the ITS Cabinet) was made at the HCTX site and functional operation in a laboratory environment was confirmed.

3.3.1.1 ATC 2070 Standard Coverage

The ATC 2070 standard allows for four basic permutations of controller configuration: 1) 2070V, 2) 2070L, 3) 2070LC, and 4) 2070 NEMA. Harris County utilizes the 2070L version of the ATC. This configuration allows for the following replaceable modules to also be examined:

Type 2070-1B Single Board CPU Module with Serial Hub
Type 2070-2B Field I/O Module
Type 2070-3B Front Panel Module, Display B
Type 2070-4A Power Supply Module, 10 Amps

3.3.1.2 ITS Cabinet Coverage

The ITS Cabinet specification consists of physical specifications to support mounting and wiring of external inputs and outputs, as well as identifies the necessary power and serial bus connections needed to interconnect devices. It is available in three different housing assemblies, identified as Type 1, Type 2, etc. In addition to these core housing assembly components, the cabinet standard specifies a series of interchangeable input and output assemblies as well as power and serial interface units.

Harris County deploys all three housing assembly sizes as well as most combinations of interchangeable assemblies.

3.3.2 Interview Users, Vendors, and System Integrators

This step includes structured technical interviews conducted at the vendor/contractor facilities and follow-up by phone. Interview questionnaires are prepared in advance and are derived from the static examination of the standards and system documentation. Although the questionnaires primarily consisted of questions related to the vendor's implementation of the standards, they also included questions directed to programmatic issues and agency needs. These interviews aid in the understanding of the vendor's implementation and address at least three potential categories of issues:

1) Issues related to exceptional conditions discovered by the developer.
2) Subjective and qualitative coverage and data collection for assessment of non-testable technical features.
3) Verification of standards content baseline prior to the commitment of resources to the more specific and extensive field testing.

The initial interview questionnaire for the ATC 2070 and ITS Cabinet standards testing was conducted in Houston, TX at the HCTX offices in August of 2007. Three (3) people were interviewed using the questionnaire developed for this process. These people, identified below, contributed information and opinions for this report. They represented three (3) different stakeholders in the process including public sector deployer, and in fact, also helped generate the standards under review. The text of the questionnaire, along with the responses from the various participants, is included in Appendix A of this document.

Upon completion of these interviews, the results were reviewed and a document of preliminary findings was generated. These findings have been further clarified over time via additional question and answer discussions with HCTX and on-site testing. These findings, both general and specific, are described in the findings section of this report.

3.3.3 Conduct On-Site Testing

This step includes structured, controlled experiment using well-defined and documented test conditions. The documentation is the standard itself, and the test conditions mimic those found as the devices under test are deployed. The intent is to test a representative sample of the types of standard functions and features accessible through the implementation and as many exception conditions as possible given timing of the site visit.

Table 3.2 shows the timeline of the events that were carried out in conducting the interview questionnaire and the device testing.

Table 3.2. Standards Testing Events

Event	Time and Place	Attendees
Questionnaire	Houston, TX August 1 – 2, 2007	Ron Johnson – HCTX Herasmo Iniguez – CalTrans Dave Miller – Siemens Tom Timcho – ISTT Wilt Alston – ISTT
Testing	Houston, TX December 3 – 6, 2007	Ron Johnson – HCTX Herasmo Iniguez – CalTrans Dave Miller – Siemens Tom Timcho – ISTT Wilt Alston – ISTT

3.4 On-Site Testing Approach

This section summarizes the specific approach used to conduct the on-site portion of the standards testing activity. A cursory assessment of the specifications found in Appendix B would show that only a fraction of the requirement clauses found in the documents has been tested. In order to determine how to test the standard, a multifaceted process was followed:

The entire document was broken down into separate clauses, each clause reflecting what could be called a requirement.

1. Each of these clauses was placed in a table similar to the tables shown in Appendix B.
2. Each of these clauses was evaluated as being quantifiable via performance testing, inspection, or analysis. These descriptions were intended to describe how each of the requirements could, under ideal conditions, be verified.
3. Each of these clauses was then evaluated in terms of what purpose it served in the standard (in other words, what requirement did it define) and how one might verify conformance with the clause. This "first pass," which classified each requirement as either "Design," "Performance," or "Procurement," was performed by the ITS Standards Test Team (ISTT) and was completed without insight from any of the key implementers who would be available during the subsequent interviews and testing exercises.
4. The ISTT then led HCTX site team, Johnson, Iniguez, and Miller, through the full standards requirement table, modifying the designations between "Design," "Procurement," and "Performance" with the goal to derive a list of items designated as "Performance" that were both indicative of the use of the standard by Harris County and able to actually be analyzed, demonstrated, inspected, or tested while on-site for the testing visit.
5. The items that remained on the list after this process are included in the table in Appendix B of this document. The methodology above resulted in seventy-three (73) verifiable requirements for the ATC 2070 and eighty-one (81) verifiable requirements for the ITS Cabinet. These requirements provided an excellent cross-section of the types of items specified in the standard.

3.5 On-Site Testing Results

The on-site testing was performed December 3-6, 2007 at the offices of HCTX using the test steps located in Appendix B and described in the previous section. The same key stakeholders from the interview phase were also involved in the testing process.

The results of the testing, along with pertinent comments, are included in Appendix B of this document.

3.6 On-Site Testing Analysis

Upon completion of the on-site testing, the results were compiled and the findings, both general and specific, and the recommendations of the ISTT were generated and documented. The summary of these findings are included in the next sections. The details are included in the Appendices of this Final Report.

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4.0 Observations and Findings

This section presents the general test findings derived and determined from examination, interpretation, and analysis of all test data and information. It is organized into general findings that relate to the standards and specific findings that relate to a specific section or paragraph of each document.

4.1 General Findings

As previous identified, the ISTT goal was to evaluate the standards in terms of their ability to satisfy the transportation community in terms of suitability, effectiveness, interoperability and interchangeability.

Taking the results shown in the following sections together and evaluating the overall performance of the standard, particularly with regard to its ability to accomplish interoperability and interchangeability given the approach used by the site in deploying standards, the following conclusions are apparent.

- The devices implemented as per the standard by various vendors were interoperable and interchangeable. The standard accomplishes its goals in this regard. It could therefore be said that the standards are complete, clear, effective, and suitable for the deployments visited.
- There were seven (7) specific instances (out of 73) in the verification of the ATC 2070 and seven (7) specific instances (out of 81) in the verification of the ITS Cabinet where the deployed devices did not reflect a strict adherence to the standard. Those instances did not negatively affect the deployment of the devices in terms of interoperability or interchangeability.
- The vendors delivering the various devices implemented as per the standard appear to be able to follow the directions, requirements, and specifications presented in the standard to provide devices that meet the needs of the users deploying those devices.
- There appears to be some amount of “legacy” or “historical” information included in the standard which is intended to support backward compatibility. Neither HCTX nor CalTrans made use of the legacy information, and as such, it could not be examined for suitability, effectiveness, or support of interoperability or interchangeability.
- There appears to be some amount of subjective description in the standard. Generally, these requirements are intended to address concerns such as “workmanship” or “good manufacturing processes” and therefore an objective specification is difficult to provide. The sites deploying the devices work around these issues by working closely with each vendor to provide additional understanding required to meet the standard, if needed.
- There are situations where a requirement stated in the text conflicts with a specification identified on the drawings. Either a statement that indicates the precedence should be included or this redundant specification should be removed.
- The Testing section should be reviewed for applicability to the devices described herein. It seems that this was adopted from another standard, but not fully tailored to the specific

needs of these devices. The intent is good, but compliance to it may be impossible to achieve, and if no vendors complies, the value is questionable.

- The inclusion of both design and procurement-related items in the standard is questionable. We recommend that they be moved to a companion volume, or at a minimum, clearly indicate that these are design or procurement items and should be treated as such.

4.2 Results – Static Evaluation

This section summarizes the findings resulting from a static evaluation of the standard, completed by ISTT staff before visiting the site to conduct the interview phase or the testing phase of the ITS standards testing for the ATC 2070 and ITS Cabinet standards. The "raw data" for these results may be found in Appendix B. These findings are listed as found in the Appendix with identifying section numbers as shown, with no additional grouping, except for the fact that the ATC 2070 and the ITS Cabinet are listed in separate tables.

4.2.1 ATC 2070

Item	11
Page	15
Paragraph	**3.1.9 Daughter Boards**
Clause	Components are allowed to be mounted under the daughter board.
Comment	
Recommendation	Drop from the standard.
Item	13
Page	15
Paragraph	**3.2.1 Components – General**
Clause	When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.
Comment	This appears to be a procurement standard and could be dropped from a design standard.
Recommendation	Drop from the standard.
Item	69
Page	19
Paragraph	**3.2.14.1 Wiring, Cabling, and Harnesses**
Clause	Conductors within an encased harness have no color requirements.
Comment	This could be covered via a blanket statement in the front of the standard.
Recommendation	Drop from the standard.
Item	70
Page	19
Paragraph	**3.2.14.1 Wiring, Cabling, and Harnesses**
Clause	Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.
Comment	What does "where possible" mean and how is it quantified?
Recommendation	Drop from the standard.

Item	122
Page	23
Paragraph	**3.3.5 Workmanship**
Clause	Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.
Comment	While it is unassailable that high quality is necessary, how is a vendor to determine that "the highest" quality has been met?
Recommendation	Drop from the standard.
Item	123
Page	23
Paragraph	**3.4.1 Human Engineering**
Clause	The equipment shall be engineered for simplicity, ease of operation and maintenance.
Comment	
Recommendation	Drop from the standard.
Item	129
Page	24
Paragraph	**3.4.2 Design Engineering**
Clause	The design shall take into consideration the protection of personnel from all dangerous voltages.
Comment	What does "take into consideration" mean and how is it verified?
Recommendation	Drop from the standard.
Item	159
Page	23
Paragraph	**3.5.4 Jumpers**
Clause	Jumpers are not allowed unless called out in the specifications or approved by the AGENCY.
Comment	As a requirement, this provides little guidance.
Recommendation	Drop from the standard or reword to state that jumpers are not allowed.
Item	206
Page	54
Paragraph	**4.2.3.5 Flash Memory**
Clause	The MCB shall be equipped with all necessary circuitry for writing to the FLASH Memory under program control.
Comment	Why would the MCB not be equipped to accomplish such a standard function?
Recommendation	Drop from the standard.
Item	271
Page	63
Paragraph	**4.2.7.2.5.1 CPU Module Software – Drivers and Descriptors**
Clause	The preferred method of accessing serial device drivers is through _os_setstat() and _os_getstat(). The _os_ss_size() and _os_gs_size() interface may not be required by future versions of this specification and is therefore not recommended for new development.
Comment	What is the value of stating the "preferred" method? The use of the term "may not be required" does not, on the surface, seem to fit with the recommendation against further new development.
Recommendation	Drop from the standard or reword.

Item	351
Page	73
Paragraph	**4.2.7.7.2 CPU Module Software – Drivers and Descriptors**
Clause	If the agency feels that knowledge of the source code and/or access to the source code is necessary for the purchase of Type 2070 ATCs, then they are referred to forthcoming guidance documents for provisions which should be included in a procurement specification to protect the interests of both the Manufacturer and the Agency.
Comment	Why is "agency" not in all caps, as per AGENCY in other places? This is very poorly worded. It is difficult to ascertain what this note refers to or accomplishes.
Recommendation	Drop from the standard or reword.
Item	369
Page	74
Paragraph	**4.3.5.2 Other Module Circuit Functions**
Clause	This feature is required to operate with the Type 210 Monitor Unit only.
Comment	Unclear as to why this is in the standard.
Recommendation	Drop from the standard or reword.
Item	566
Page	91
Paragraph	**4.4.5.10 Front Panel Assembly – FPA Controller**
Clause	Tab Stops shall be configurable at all columns.
Comment	Unclear as to why tab stops are being specified in a standard.
Recommendation	Drop from the standard.
Item	646
Page	99
Paragraph	N/A
Clause	Line drivers/receivers shall be socket mounted or surface mounted.
Comment	What other mounting options exist? If drivers can be mounted either way, why is it specified?
Recommendation	Drop from the standard.
Item	715
Page	106
Paragraph	**6.4.4 Module Power Supply**
Clause	The standard contains this language: "Specification 4.5.6 POWER SUPPLY REQUIREMENTS except Specification 4.5.3. In the previous section, the standard specifies that Specification 4.5.3 applies.
Comment	Confusingly worded.
Recommendation	Clarify.

4.2.2 ITS Cabinet

Item	14
Page	15
Paragraph	**3.1.9 Daughter Boards**
Clause	Components are allowed to be mounted under the daughter board.
Comment	
Recommendation	Drop from the standard.

Item	16
Page	15
Paragraph	**3.2.2 Components – General**
Clause	When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.
Comment	This appears to be a procurement standard and could be dropped from a design standard.
Recommendation	Drop from the standard.
Item	129
Page	23
Paragraph	**3.4.2 Design Engineering**
Clause	The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range.
Comment	What does this specification mean?
Recommendation	Drop from the standard.
Item	132
Page	24
Paragraph	**3.4.3 Generated Noise**
Clause	No item, component, or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.
Comment	At what noise level does interference occur?
Recommendation	Reword and clarify, providing an actual limit or requirement.
Item	124
Page	23
Paragraph	**3.4.1 Human Engineering**
Clause	The equipment shall be engineered for simplicity, ease of operation, and maintenance.
Comment	
Recommendation	Drop from the standard.
Item	130
Page	23
Paragraph	**3.4.2 Design Engineering**
Clause	The design shall take into consideration the protection of personnel from all dangerous voltages.
Comment	What does “take into consideration” actually mean and how is it assessed?
Recommendation	Drop from the standard or provide an actual requirement.
Item	160
Page	26
Paragraph	**3.5.4 Jumpers**
Clause	Jumpers are not allowed unless called out in the specifications or approved by the AGENCY.
Comment	As a requirement, this provides little guidance.
Recommendation	Drop from the standard or reword to state that jumpers are not allowed.
Item	804
Page	132
Paragraph	**5.4.1 General Requirements**
Clause	The method of isolation shall be based upon a design which shall provide reliable operation.
Comment	These words amount to suggestions that cannot be quantified in any way.
Recommendation	Drop from the standard or reword to provide a measurable requirement.

Item	815
Page	133
Paragraph	**5.5.1 General Requirements**
Clause	The method of isolation shall be based upon a design that provides reliable operation.
Comment	These words amount to suggestions that cannot be quantified in any way.
Recommendation	Drop from the standard or reword to provide a measurable requirement.

4.3 Results – Questionnaire

This section summarizes the findings resulting from the interview questionnaire phase of the ITS standards testing for the ATC 2070 and ITS Cabinet standards. The "raw data" for these results may be found in Appendix A. These findings are categorized into six (6) groups as they relate to:

- General Questions (ATC 2070 and ITS Cabinet): Completeness, Clarity, Effectiveness, Suitability, References, Terms and Definitions, Figures and Tables;
- General Questions (ATC 2070): Components, Mechanical, Quality Control, Electrical, Environment, and Testing;
- Controller-Specific Questions (ATC 2070): CPU Module, Field I/O Module, Drawings;
- General Questions (ITS Roadside Cabinet): All Areas;
- Cabinet-Specific Questions (ITS Roadside Cabinet): Transfer Relay Unit, Cabinet Monitor Unit, Serial Interface Unit, Drawings.

4.3.1 General Questions (ATC 2070 and ITS Cabinet): Completeness

Item	1.1.
Page	General Questions 1.2
Paragraph	N/A
Comment	The standard incorporates legacy requirements both in function and form factor, including, but not limited to, traffic control software programs and the types of components used in the cabinet system, e.g., switchbacks relays, etc. Furthermore, when these legacy items change in form factor, there may be a need to update the standard. Currently, some percentage of the legacy information is imbedded in the standard, although how much, is difficult to assess.
Recommendation	Remove legacy information from the standard if it serves no purpose going forward.
Item	1.2.
Page	General Question 1.3
Paragraph	N/A
Comment	There are few tasks that the implementers would like to accomplish that are not covered by the standard, although some exist. For example, HCTX is currently investigating the use of a series of less complex boxes, which might hang on poles. It is not clear how this new requirement would change the existing standard, given the need for different packaging and cabinet form factor.
Recommendation	Determine if compact form-factor of controller/cabinet is necessary for inclusion in this or other standard.

Item	1.3.
Page	General Question 1.7
Paragraph	N/A
Comment	The power supply functionality (as mentioned regarding the burgeoning use of LEDs) and the modem capability, since these implementers only use Ethernet capability, are examples of specified capability that is not needed now and might not be needed going forward.
Recommendation	Consider inclusion of LED-based signal heads in future versions of the standard.

4.3.2 General Questions (ATC 2070 and ITS Cabinet): Clarity

Item	2.1.
Page	General Question 2.1
Paragraph	N/A
Comment	Although the standards are complete, proper implementation does require the use of other standards. For example, specific guidelines for roads and traffic control, including how to lay out the lanes in an intersection and industry standards for electronics, AREMA, etc. are needed to properly implement the standards. **Aside**: Mr. Johnson (HCTX) mentioned that it was important for people to actually visit CalTrans to observe what they do, as a way to mitigate any misunderstanding from only reading the standard. The premise that the best way to avoid mistakes either in implementation or understanding and gain the requisite "informative knowledge" was to visit CalTrans, was mentioned several times.
Recommendation	Incorporate a recommendation that users of the standard seek guidance from "best of breed" implementers, such as Caltrans, possible through the USDOT Standards deployment support efforts.
Item	2.2.
Page	General Question 2.4
Paragraph	N/A
Comment	While no examples of any such areas were given, there may be areas of the standards that are not understandable. The implementers have been actively resolving these areas, via the same iterative process as the standard was developed using.
Recommendation	Continue the current process with regard to resolving these on-going issues.
Item	2.3.
Page	General Question 2.5
Paragraph	N/A
Comment	There had been messages or elements of the standards that were open ended or could be interpreted in more than one way, but the implementers closed the bulk of them over the iterative process that they've been on for so long. **Aside**: There appear to be items specified in the standard that have hidden or implied reasons. For example, if the material for the front latch is changed, the form factor of the latch will be different, and interoperability may be compromised. The standard says, "Use material XXX" without giving a specific reason. It is not clear how such information might be better communicated, if at all.
Recommendation	Incorporate explanatory or expansive text, specifically for providing context in situations such as the door handle, throughout the standard.

4.3.3 General Questions (ATC 2070 and ITS Cabinet): Effectiveness

Item	3.1.
Page	General Question 3.4
Paragraph	N/A
Comment	The standards provide a level of detail sufficient to procure the specified systems. However, there is still a quantity of "implied knowledge" required to use the standard properly. Both Mr. Johnson and Mr. Iniguez admitted that if one was in need of detail upon what to buy, he would need not only the standard, but also some other—as yet unspecified—understanding of what might be needed for a particular implementation.
Recommendation	Incorporate a recommendation that users of the standard seek guidance from "best of breed" implementers, such as Caltrans. See response for 2.1 above.

4.3.4 General Questions (ATC 2070 and ITS Cabinet): Suitability

Item	4.1.
Page	General Question 4.1
Paragraph	N/A
Comment	The use of the standards simplified the life cycle processes for requirements, design, build, evaluate and deploy.
Recommendation	None.

4.3.5 General Questions (ATC 2070 and ITS Cabinet): References

Item	5.1.
Page	General
Paragraph	N/A
Comment	The references to other external documents or material listed in the standards were complete and useable, likely due to the fact that the developers actually hired a professional editor.
Recommendation	None.
Item	5.2.
Page	General
Paragraph	N/A
Comment	There was no discussion of superfluous references, and it is believed that none exist.
Recommendation	None.
Item	5.3.
Page	General
Paragraph	N/A
Comment	In using the standard, the implementers admitted that they did consult some external references and that one has to be conversant with external references in order to make best use of the standard. There are issues buried in the standard that relate to experience the implementers have gained because this standard specifies a "legacy" item and reflects the lessons learned thereof. CalTrans noted that most of the external references are industry standards, and so one needs to understand those to properly use the standard. Nevertheless, it seems clear that as implementers who are also standard developers, the people interviewed for this testing process were not really equipped to generally address the concern of implied knowledge since they had such a long experience with both the standard and the implementation of it.
Recommendation	Clearly identify which standards are Informative versus Normative, and if possible, include specific statements as to the body of knowledge the specific referenced standard contributes to the understanding/implementation of this standard.

4.3.6 General Questions (ATC 2070 and ITS Cabinet): Terms and Definitions

Item	6.1
Page	General
Paragraph	N/A
Comment	Due to the iterative nature of the standard and the fact that the interviewees were both developers and implementers, it was deemed unnecessary to ask if the glossaries of terms, definitions, and acronyms met their needs in understanding and using the standards. However, during testing, it was discovered that some key 'measureable' characteristics of the standard were only embodied in the glossary.
Recommendation	Ensure that no requirements of the standard are found solely in the glossary.

4.3.7 General Questions (ATC 2070 and ITS Cabinet): Figures and Tables

Item	7.1
Page	General Question 7.2
Paragraph	N/A
Comment	There are not any figures or tables terms that need to be added or revised.
Recommendation	None. (Note that this question, as answered during the interview portion of the testing, was found to be incorrect during the actual testing portion where several illustrations were found to not match the text in the standard.)

4.3.8 General Questions (ATC 2070): Components

Item	8.1
Page	15
Paragraph	**3.2.2.1 Electronic Components**
Comment	The reference to socket mounts and the allowance of them is another legacy issue in the standard. The socket mounts were used historically, since the level of maintenance required it. This wording of the standard simply leaves a "door open" for an implementer to use socket mounts if needed.
Recommendation	Drop from standard.
Item	8.1.
Page	15
Paragraph	**3.2.2.4 Electronic Components**
Comment	The requirement that components be easily accessible, replaceable and identifiable for testing and maintenance is another legacy issue. Such a requirement was an issue with using daughter boards and non-surface mounted parts. Given that ICs now cannot typically be replaced, accessibility of the type provided by socket mounts is likely not that important.
Recommendation	Drop from standard.
Item	8.3
Page	18
Paragraph	**3.2.10 Fuses**
Comment	The fuse (there is only one) in the device can be described as easily accessible and removable without use of tools.
Recommendation	The reason for this requirement, the small amount of time available to service a device, might provide beneficial context to the standard.

Item	8.4
Page	18
Paragraph	**3.2.10 Fuses**
Comment	It was not clear upon what criterion (or criteria) anyone could be expected to base the characterization of "easily accessible" and it was clear that no obvious objective criteria was in place, either in the standard nor the minds of the implementers.
Recommendation	Provide an objective requirement, possibly in terms of force needed.

4.3.9 General Questions (ATC 2070): Mechanical

Item	9.1
Page	19
Paragraph	**3.2.14 Wiring, Cabling, and Harnesses**
Comment	The requirement that all the harnesses in the device be "neat, firm and properly bundled" is subjective, although the intent is to insure that there is no obstruction for serviceability. One of the goals of the standard is to insure that everything is of "the highest workmanship and quality" and poorly bundled cables do not reflect high workmanship. These statements are "boilerplate" requirements, intended to insure a high-quality device.
Recommendation	Provide an objective requirement, or drop from standard.
Item	9.2
Page	General
Paragraph	N/A
Comment	No objective criterion is currently used to communicate the cable requirement but the recurring theme of workmanship was deemed sufficient for these purposes, even though it is subjective.
Recommendation	Provide an objective requirement, or provide an example drawing, or drop from standard.
Item	9.3
Page	22
Paragraph	**3.3.1 Assemblies**
Comment	It is expected that the requirement that all assemblies in the device are modular, easily replaceable and incorporate plug-in capability for their associated devices or PCB will be met if the vendor follows the dimensions found in the standard. It is not clear that this expectation is not based upon implied knowledge resulting from so much time invested in developing and iterating the standard while implementing it.
Recommendation	Provide an objective requirement, or provide an example drawing, or drop from standard.
Item	9.4
Page	22
Paragraph	**3.3.1 Assemblies**
Comment	Such criteria as "easily replaceable" are part and parcel with developing a high-quality device.
Recommendation	Provide an objective requirement, or provide an example, or drop from standard.
Item	9.5
Page	23
Paragraph	**3.3.4.2 Model and Serial Numbers**
Comment	Characterizing the permanent label affixed to the inside near and center floor of the Type 2070 unit chassis as "easy to read" reflects quality workmanship and therefore requires no further explanation. Any subjectivity could be eliminated with the use of a picture.
Recommendation	Provide an objective requirement, or provide an example drawing, or drop from standard.

Item	9.6
Page	General
Paragraph	N/A
Comment	Such criteria as "easy to read" are part and parcel with developing a high-quality device.
Recommendation	Provide an objective requirement, or provide an example drawing, or drop from standard.
Item	9.7
Page	24
Paragraph	**3.4.1.3 Human Engineering**
Comment	In order to understand what the standard refers to when it says "the PCBs in the device slide smoothly in their guides while being inserted into or removed from the frame and fit snugly into the plug-in PCB connectors." Caltrans has developed requirements that are less subjective and may be of value to be considered. **Aside**: This requirement is intended to address "workmanship" as the overriding consideration. The implementers kept going back to "why" a particular requirement was placed in the standard—in effect defending the standard and justifying it—but the intent of the questions about how subjective criteria were measured was to understand the "what" of the standard, and how it could be quantified, communicated, and objectively known. This is the result of interviewing the developers of the standard about how they implement the standard.
Recommendation	Incorporate a recommendation that users of the standard seek guidance from "best of breed" implementers, such as Caltrans, or provide another reference that more objectively addresses the workmanship requirements implied in the standard.
Item	9.9
Page	General
Paragraph	N/A
Comment	A special tool is used to verify that the resistance between any two isolated, independent conductor paths is at least 100 MegOhms when a 500 VDC potential is applied. That tool is not mentioned in the standard, although this apparent oversight may simply reflect "common knowledge" for such an application.
Recommendation	Make a direct reference to the tool required to make this measurement.
Item	9.10
Page	25
Paragraph	**3.5.1.4.3 Design, Fabrication, and Mounting**
Comment	No active methodology for verifying the quality of all the solder joints on each PCB is used. Instead, overall performance, or field failures, trigger an investigation that generally find cold solder joints on the offending PCB. As ISO covers many of the GMP criteria implied in the standard, ISO could also be referenced, but it is currently not cited. The conflict with this approach—using ISO specifications—is that the devices are sometimes being manufactured by small companies for whom meeting the general requirements of ISO would be an undue burden. As a consequence, some ISO-type requirements are included and the implementers work with the vendor to understand how to meet them.
Recommendation	If the solder joints will not be verified in any event, but only the performance of the device will be assessed, having this requirement serves no purpose. Drop from the standard.

4.3.10 General Questions (ATC 2070): Quality Control

Item	10.1
Page	27
Paragraph	**3.6.1 Components**
Comment	Lot sampling all components is not routinely done. If failures occur, verification via lot sampling may occur as a result.
Recommendation	Either include requirement that vendor produce documentation that shows this is met, or drop requirement.
Item	10.5
Page	27
Paragraph	**3.6.2 Subassembly, Unit, or Module**
Comment	Electrical, environmental and timing compliance testing on each module, unit, printed circuit or subassembly is not generally required although the standard cites it. In some cases the failure rate of delivered modules is monitored to determine if the devices perform at higher than a 3% failure rate. If not, then the devices are sampled at an even higher rate. In other cases, where devices are not purchased in "lots" (contracted delivery of devices) ATC 2070 are installed directly in the field. Only in the event of failures are devices tested against the standard to determine if those devices are meeting the requirements.
Recommendation	Either include requirement that vendor produce documentation that shows this is met, or drop requirement.
Item	10.7
Page	27
Paragraph	**3.6.2 Subassembly, Unit, or Module**
Comment	Components are not tested as a complete controller assembly, although the standard requires it. This is another requirement that is specified in the standard but not followed until a problem is detected.
Recommendation	Either include requirement that vendor produce documentation that shows this is met, or drop requirement.
Item	10.9
Page	27
Paragraph	**3.6.2 Subassembly, Unit, or Module**
Comment	Housing, chassis, and connection terminals are not typically expected for mechanical sturdiness, at least not on a routine basis. Mr. Johnson mentioned that they probably would perform such an inspection during the approval process, but even then not on every single unit. **Aside**: Mr. Johnson noted that HCTX does not require the vendor to produce any reports of findings, contrary to what the standard seems to require. His point of view is that requiring the vendor to produce paperwork is of limited value, since the vendor could have simply created it out of thin air. If an item begins to fail, he can always go back and test it against the specification.
Recommendation	Either include requirement that vendor produce documentation that shows this is met, or drop requirement.
Item	10.14
Page	27
Paragraph	**3.6.2 Subassembly, Unit, or Module**
Comment	The equipment is visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies, as would be expected by GMP. In some cases a check-list and test-plan for this inspection, neither of which is required by the standard, is used.
Recommendation	Include a recommendation or example of a check-list for this inspection.

Item	10.17
Page	27
Paragraph	**3.6.3 Pre-delivery Repair**
Comment	The process for handling defects or deficiencies found by the inspection system involving mechanical structure or wiring include returning the items through the manufacturing process or special repair process for correction is defined as part of the warranty process.
Recommendation	Either include requirement that vendor produce documentation that shows this is met, or drop requirement.
Item	10.19
Page	27
Paragraph	**3.6.3 Pre-delivery Repair**
Comment	Although the standard specifies that PCB's should not be flow soldered a second time, it seems clear that the manufacturers do not have to provide any proof since the recipients of the devices wouldn't know how many times a board has been soldered anyway. It is not clear that this requirement should be in the standard.
Recommendation	Drop from the standard.
Item	10.20
Page	27
Paragraph	**3.6.3 Pre-delivery Repair**
Comment	Given that there is no way to tell how many times a board has been soldered, this requirement is simply a means by which to preclude errors before they happen. By setting this type of requirement, if the devices exhibit problems, those receiving the devices have a legitimate reason to question the vendor regarding this area.
Recommendation	Drop from the standard.

4.3.11 General Questions (ATC 2070): Electrical, Environment, and Testing

Item	11.1
Page	28
Paragraph	**3.7.3 Testing Certification**
Comment	HCTX does not follow the ATC 2070 standard with regard to requiring the generation of quality control/final testing reports, since they feel it would be of little value and not necessarily disclosing any information. Caltrans does require a report on the controller, but tests everything anyway. Given HCTX's impression (which is not necessarily inaccurate) and Caltrans' normal practice, it is not clear that requirements relating to reports add any value.
Recommendation	None at present, but it could be argued that this requirement is unnecessary, particularly since HCTX does not require it and since Caltrans tests everything regardless of the submission of a report.
Item	11.3
Page	28
Paragraph	**3.7.3 Testing Certification**
Comment	For Siemens, all test reports delivered generally include Design Acceptance testing of all supplied components. For the other implementers, the answer was as noted above.
Recommendation	None.
Item	11.5
Page	28
Paragraph	**3.7.3 Testing Certification**
Comment	Some implementers do not require reports, so the requirement that those reports include physical and functional testing of all modules and items is moot for them.
Recommendation	None.

Item	11.7
Page	28
Paragraph	**3.7.3 Testing Certification**
Comment	Some implementers do not require reports, so the requirement that those reports include environmental testing report(s) for all equipment is moot for them.
Recommendation	None.
Item	11.9
Page	30
Paragraph	**3.7.5.2.2 Low-Repetition High-Energy Transients**
Comment	Some implementers follow the ATC 2070 standard with regard to high-energy and high repetition transients, completing all tests that are non-destructive. Some implementers do not require reports, so the requirement that those reports include high-energy and high repetition transients is moot for them.
Recommendation	None.
Item	11.11
Page	30
Paragraph	**3.7.5.2.2 Low-Repetition High-Energy Transients**
Comment	Given the maturity of the standard and the involvement the interviewees had in its development, the question regarding transients and power service is irrelevant. It is unknown if the answer would be similar for users who did not also play such a substantial role in its development.
Recommendation	None.
Item	11.13
Page	31
Paragraph	**3.7.5.5 Temperature and Humidity**
Comment	Given the maturity of the standard and the involvement the interviewees had in its development, the question regarding temperature and humidity testing is irrelevant. It is unknown if the answers be similar for users of the standard who did not also play such a substantial role in its development.
Recommendation	None.
Item	11.15
Page	32
Paragraph	**3.7.6 Test Facilities**
Comment	None of the implementers follows the standard with regard to performing environmental testing themselves, but all expect that the vendors who deliver devices will meet the standard in this regard.
Recommendation	Include criteria for acceptance of the product against these requirements.
Item	11.17 – 11.22
Page	32
Paragraph	**3.7.6 Test Facilities**
Comment	While none of the implementers actually run environmental tests, some of them receive a report from the vendor for each of the environmental tests that is more of a check-list of all the tests run. One of the implementers noted that even if several devices failed for apparent environmental reasons, he still would not follow the standard and require a report of the environmental tests. It remains unclear why these test reports are listed as required in the standard when they are not "required" be these implementers.
Recommendation	Reword this section to provide guidance to the vendor for the design and build of the devices, but not to require the presentation of a report.

Item	11.23 – 11.26
Page	38
Paragraph	**3.7.8 Vibration Test**
Comment	Given the maturity of the standard and the involvement the interviewees had in its development, questions regarding vibration testing procedures are irrelevant. It is unknown if the answers be similar for users who did not also play such a substantial role in its development.
Recommendation	None.
Item	11.27 – 11.30
Page	40
Paragraph	**3.7.9 Shock (Impact) Test**
Comment	Given the maturity of the standard and the involvement the interviewees had in its development, questions regarding shock testing are irrelevant. It is unknown if the answers be similar for users who did not also play such a substantial role in its development.
Recommendation	None.
Item	11.31 – 11.34
Page	43
Paragraph	**3.7.11 Cabinet Assembly Tests**
Comment	Given the maturity of the standard and the involvement the interviewees had in its development, questions regarding cabinet assembly testing are irrelevant. It is unknown if the answers would be similar for users who did not also play such a substantial role in its development. **Aside**: Caltrans is the only authority who has created an "acceptance test" for verifying the operation of the overall unit. It is not clear how HCTX verifies the overall operation of a unit, outside the Caltrans "DAT" test, which HCTX does not routinely use. Mr. Johnson suggested that Caltrans become a *de facto* certifying body for the industry. It is not clear that the standard provides real value with regard to all the testing requirements which are included in it.
Recommendation	Consider dropping this section from the standard.
Item	11.35
Page	45
Paragraph	**3.7.13 Cabinet Monitor Unit Tests**
Comment	A number of the specific areas of testing outlined in the ATC 2070 standard reflect that they are "under consideration." HCTX noted two things about these sections. One, they perform discrete tests for individual components, and therefore there are no guidelines for this area. Two, these sections should be deleted since much of the information in them is carry-over from a prior version of the standard.
Recommendation	Drop from the standard.

4.3.12 Controller-Specific Questions (ATC 2070): CPU Module

Item	12.1
Page	51
Paragraph	**4.2 Type 2070-1 CPU Module**
Comment	None of the interviewees prepared a separate software design specification, in addition to the software design specifications listed in the ATC 2070 standard. Again, the use of the DAT, developed by Caltrans, was mentioned during the discussions. The DAT is actually called out in Section 4.2.7.5.1. There was disagreement between Mr. Johnson and Mr. Iniguez as to if the DAT is always "required" versus never left in a 2070 controller. One of the users, in fact, one of the key users at HCTX, had never used the DAT. It appears that now HCTX will begin, as a result of this discussion and interview, to use the DAT. Either way, the wording in the standard needs to be modified to reflect the state-of-the-art, including the use of a DAT, from where it comes, and how it is used. Although Caltrans has supervised the development of the DAT, it is apparently a product derived from a number of manufacturers.
Recommendation	Recommend inclusion of DAT in delivered software.

4.3.13 Controller-Specific Questions (ATC 2070): Field I/O Module

Item	13.1
Page	74
Paragraph	**4.3.4.3 Parallel I/O Ports**
Comment	The use of the terminology "glitch" with regard to the performance of a Parallel I/O Ports output circuit has been cleaned up. Apparently, v02.03, which the ISTT had been given to evaluate, was not the latest internal version, which is v02.06. This later version reflects some improvements, of which this is one.
Recommendation	Ensure 'glitch' is defined.
Item	13.9
Page	89
Paragraph	**4.4.4 Display**
Comment	HCTX created their own system design specification relative to the types of items specified in the Display Section, 4.4.4, portion of the standard, despite the fact that the standard included a simple design specification.
Recommendation	Recommend that HCTX-specific items be considered for inclusion in future standard.

4.3.14 Controller-Specific Questions (ATC 2070): Drawings

Item	14.1
Page	97 and Beyond
Paragraph	**4.7 Chapter Details (Drawings)**
Comment	All interviewees felt the drawings were clear and provided the appropriate amount of information. They mentioned that the current drawing structure reflects the fact that the current standard reflects the end of a long iteration process. **Aside**: It is clear that interviewing the developer(s) of the standard is not suitable for addressing many of these questions in an objective way. The amount of "implied knowledge" inherent in the standard cannot be ascertained via these interviews.
Recommendation	A detailed review of all drawings by a manufacturing engineer could benefit deficiency identification and eliminate the legacy knowledge issues.

Item	14.2
Page	97 and Beyond
Paragraph	**4.7 Chapter Details (Drawings)**
Comment	Mr. Iniguez noted that all manufacturers normally submit drawings additional to the drawings shown in the standard, drawings that the implementer will use to verify that what the vendor is going to produce will meet the standard. Mr. Johnson noted that a manufacturer must place all the items on the front, and exactly where need not be specified by the standard. Given the number of items, they can only end up in certain places. **Aside**: This represented the first time in the interview process where the need for implied knowledge, knowledge not provided by the standard would be needed by a manufacturer, and that a manufacture would have to produce information not specifically cited by the standard. Mr. Iniguez noted that the vendor should submit s theory of operation, but this requirement is not described in the standard. It was not clear, even in follow-up questioning, how a manufacturer could be expected know to submit such an item.
Recommendation	None. (While it is outside the scope of this review, it is worth noting that the V5.2 ATC standard includes a theory of operation section.)

4.3.15 General Questions (ITS Roadside Cabinet): All Areas

Item	17
Page	General
Paragraph	N/A
Comment	All questions in this section were deemed unnecessary as they had been answered in previous sections. Furthermore, given the fact that the standard being tested is the result of many, many iterations—resulting in what could only be termed a "legacy" product—and is being employed by the developers, such questions as these will provide little, if any, additional insight into the standard's effectiveness.
Recommendation	None.

4.3.16 Cabinet-Specific Questions (ITS Roadside): Transfer Relay Unit

Item	21.1
Page	41
Paragraph	**4.3.1.6 Model 204 Flasher Unit**
Comment	Regarding the question on experimentally verifying that the flasher unit circuitry would operate in an open-circuit condition without load for 10 years minimum, several findings were apparent. Mr. Johnson mentioned that they install a 2 microfarad capacitor in the circuit because it was impractical to operate without load. This section should be updated to reflect that the capacitor is needed in some cases. This requirement is currently being met due to the existence of cabinets that have been running in the field for over 10 years. That does not address the standard and how one would meet this requirement *a priori*.
Recommendation	Update this section to include a reference to the 2 microfarad capacitor mentioned above by Mr. Johnson.
Item	21.2
Page	41
Paragraph	**4.3.1.6 Model 204 Flasher Unit**
Comment	In explaining how they approach the 10 year requirement, Mr. Miller mentioned that his organization brought in a guy to do a MTBF to predict these requirements.
Recommendation	This requirement and others like it should be reflected in the "boilerplate" of the standard, using an MTBF premise.

Item	21.4
Page	42
Paragraph	**4.3.2 Model 205 Flash Transfer Relay Unit**
Comment	None of the interviewees had actually experimentally verified that the switch would perform a minimum of 100,000 operations while switching a tungsten load of 1000 Watts at 70 degrees C. Mr. Johnson noted that the intent of this requirement should be to determine if the flasher could work all day flashing continuously. What is needed is a "reasonable expectation" for the timing. Despite this understanding, it remains unclear how an implementer with less experience with the standard would use this requirement.
Recommendation	Construct the requirement to identify the operational needs that must be met and not specific, 'arbitrary' value.
Item	21.7
Page	42
Paragraph	**4.3.2 Model 205 Flash Transfer Relay Unit**
Comment	The requirement, to experimentally verify that the DPDT contact points were capable of switching 20 Amperes or one Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitations, was called a "design criteria" by Mr. Johnson, but he was unaware if his organization actually determined if the devices met the criteria. Mr. Iniguez noted that this requirement represents the "expected rating" of the device, as opposed to the output of a test. The standard currently specifies that this requirement be experimentally verified.
Recommendation	Modify the standard to illustrate that this is a design standard and not an experimental requirement.

4.3.17 Cabinet-Specific Questions (ITS Roadside): Cabinet Monitor Unit

Item	22.1
Page	42
Paragraph	**4.4 Model 212 ITS Cabinet Monitor Unit (CMU)**
Comment	None of the interviewees prepared an input message design specification in addition to the one listed in section 4.4 of the ITS Cabinet Monitor Unit standard. Mr. Miller noted that the detail in this section was a result of a previous decision to make sure it was possible to "mix and match" between CMU's and AMU's from different vendors, which was verified experimentally. **Aside**: There appears to be a need for a "white paper" that provides some insight about what HCTX has found in trying to reconfigure the ITS Cabinets for operation in specific cases.
Recommendation	None. It is possible that the white paper noted above would be useful, but it is not required at this time.

4.3.18 Cabinet-Specific Questions (ITS Roadside): Serial Memory Key, etc.

Item	23.1
Page	55 and Beyond
Paragraph	**4.4.14 Monitor Unit Serial Memory Key**
Comment	The interviewees implemented the monitor unit serial memory key as specified in section 4.4.14 of the ITS Cabinet Monitor Unit standard.
Recommendation	None.

Item	24.1
Page	General
Paragraph	**4.4.15 CMU Connector**
Comment	The interviewees implemented the pin-outs on the CMU Connector as specified in this section of the standard.
Recommendation	None.
Item	25.1
Page	General
Paragraph	**4.4.16 Serial Bus #1 Frames**
Comment	The interviewees implemented the byte format for the Serial Bus #1 Frames as specified in this section of the standard.
Recommendation	None.

4.3.19 Cabinet-Specific Questions (ITS Roadside): Serial Interface Unit

Item	26.1
Page	104
Paragraph	**4.7.15.9.4 Tracking Functions Overview**
Comment	Mr. Johnson noted that although the Tracking Functions and Complex Output Functions are implemented in his organization's devices as specified in the standard, he is not happy with the current behavior because the two features can generate output without a direct command from the controller. Mr. Miller felt this was not a valid fear since the programmer can choose to use this functionality or not. There are applications in the SIU that can influence the outputs regardless of what the controller says. The purpose of this functionality is to off-load work from the controller, which is beneficial, even though the use of this functionality could result in some loss of closed-loop control. It is not clear how this will be resolved going forward.
Recommendation	None, although it is worth noting that two key stake-holders differ in point of view about this portion of the standard.

4.3.20 Cabinet-Specific Questions (ITS Roadside): Detectors

Item	28.1
Page	127
Paragraph	**5.2.1 General Requirements**
Comment	The requirements in this section posited in terms of a "vehicle" passing over or remaining over loop wires embedded in the roadway, were verified via techniques developed as a result of the legacy nature of this specification. It is not clear how a new vendor would understand how this requirement should be verified.
Recommendation	None.

4.4 Results – On-Site Testing

This section summarizes the findings resulting from the testing phase of the ITS standards testing for the ATC 2070 and ITS Cabinet standards. The "raw data" for these results may be found in Appendix B. These findings are categorized into groups corresponding to the devices tested, across both devices, as they relate to:

- ATC Type 2070 General Requirements
- ATC Type 2070 Controller Requirements
- ATC Type 2070 CPU Requirements
- ATC Type 2070 Field I/O Module Requirements
- ATC Type 2070 Front Panel Assembly Requirements
- ATC Type 2070 Power Supply Module Requirements
- ATC Type 2070 VME Cage Assembly Requirements (No testable requirements.)
- ATC Type 2070 Peripheral Equipment Requirements (No testable requirements.)
- ATC Type 2070-2N NEMA Field I/O Module Requirements (No testable requirements.)
- ATC Type 2070-4N NEMA Power Supply Module Requirements (No testable requirements.)
- ATC Type 2070-8 NEMA Field I/O Module Requirements (No testable requirements.)
- ITS Cabinet General Requirements
- ITS Cabinet PC Board Requirements (No testable requirements.)
- ITS Cabinet Models 200 and 204 Requirements
- ITS Cabinet Model 200 Switch Pack Unit Requirements
- ITS Cabinet Model 204 Flasher Unit and Model 205 Flash Transfer Unit Requirements
- ITS Cabinet Model 212 Monitor Unit (CMU) Requirements
- ITS Cabinet Model 214 Auxiliary Monitor Unit (AMU) Requirements
- ITS Cabinet Model 216-12 & 216-24 Power Supply Unit Requirements
- ITS Cabinet Type 218 – Serial Interface Unit (SIU) Requirements
- ITS Cabinet Loop Detector General Requirements
- ITS Cabinet Housing Requirements
- ITS Cabinet Rack Cage Requirements (No testable requirements)
- ITS Cabinet Assembly Requirements

4.4.1 ATC Type 2070 General Requirements

Item	50
Page	18
Paragraph	**3.2.9.1 Load Circuit Breaker Auxiliary Internal Switches**
Comment	ATC 2070 Requirement 50 (auxiliary switches) is apparently not applicable to the ATC 2070 and actually referred to the ITS Cabinet.
Recommendation	Delete this clause from the standard.

Item	79
Page	20
Paragraph	**3.2.14.6 Wiring, Cabling, and Harnesses**
Comment	ATC 2070 Requirement 79 (conductor color-coding) was not met by all examined products. The standard specifies the use of the US color convention, but the device we examined appeared to be using both the US standard as well as the European standard.
Recommendation	Update the standard to reflect the European standard, or delete this clause entirely.
Item	81
Page	20
Paragraph	**3.2.15.2 Indicators**
Comment	ATC 2070 Requirement 81 (viewing angle) was not met. This requirement might actually be too strenuous, but is clearly not being met by the devices currently implemented.
Recommendation	Modify the standard to reflect the actual needs of the implementation.

4.4.2 ATC Type 2070 Controller Requirements

All tested ATC 2070 requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.3 ATC Type 2070 CPU Requirements

Item	189
Page	52
Paragraph	**4.2.2.3 Type 2070 – 1B Configuration**
Comment	ATC 2070 Requirement 189 (LED labeling) was not met. The actual modules reflected the drawing, but not the text of this requirement. In other words, the drawing and the text in the standard do not match.
Recommendation	Correct the standard.
Item	227
Page	55
Paragraph	**4.2.6 Datakey**
Comment	ATC 2070 Requirement 227 (2 megabyte Datakey) was not met. HCTX doesn't use this size of key and never requested them from the manufacturer as a result.
Recommendation	None.
Item	304
Page	68
Paragraph	**4.2.7.2.9 Network Requirements**
Comment	ATC 2070 Requirement 304 (boot image) was not met. It is not clear if the text at Section 4.2.7.2.9 and the text at section 4.2.7.2.10.4, which refer to the same file, are consistent.
Recommendation	Correct the standard.
Item	307
Page	68
Paragraph	**4.2.7.2.10.1 Standard OS-9 File System Configuration**
Comment	ATC 2070 Requirement 307 (CD contents) was not met. Mr. Johnson didn't have a CD and had never used one in this manner.
Recommendation	This is again a procurement item, and should be handled accordingly. Correct the standard to reflect that this is a recommendation dependent upon the needs of the client and not a requirement.

Item	313
Page	68
Paragraph	**4.2.7.2.10.3 Standard OS-9 File System Configuration**
Comment	ATC 2070 Requirement 313 (utilities found in /CMDS directory) was not met. The utility *tsmon* was not in the /CMDS directory and was instead found in the boot image.
Recommendation	Correct the standard.
Item	315
Page	69
Paragraph	**4.2.7.2.10.4 Standard OS-9 File System Configuration**
Comment	ATC 2070 Requirement 315 (network utilities in the /CMDS directory) was not met. The utilities *tftpd* and *dtfpdc* were missing, due to an error between versions in Mr. Iniguez's CPU module drivers. (This is likely not a result of the standard, but simply an oversight within the case being examined.)
Recommendation	None.
Item	350
Page	72
Paragraph	**4.2.7.7.1 Deliverables**
Comment	ATC 2070 Requirement 350 (CD contents) was not met, for reasons previously noted: Mr. Johnson neither normally received a CD nor understood that he should.
Recommendation	Correct the standard to reflect that this is a recommendation dependent upon the needs of the client and not a requirement.

4.4.4 ATC Type 2070 Field I/O Module Requirements

Item	464
Page	82
Paragraph	**4.3.9.2.4 Request Module Status**
Comment	ATC 2070 Requirement 464 (performance with Datakey) was deemed not applicable and appears to be a legacy requirement, included in the standard only so software may continue to be written for older Field I/O modules, but still work in newer ones.
Recommendation	Add note to standard that Field I/O modules with Datakey are legacy and that this clause is only applicable in the case of their use.
Item	465
Page	82
Paragraph	**4.3.9.2.4 Request Module Status**
Comment	ATC 2070 Requirement 465 (performance with Datakey) was not tested for the same reason as given above.
Recommendation	None.
Item	466
Page	82
Paragraph	**4.3.9.2.4 Request Module Status**
Comment	ATC 2070 Requirement 466 (performance with Datakey) was not tested for the same reason as given above.
Recommendation	None.

4.4.5 ATC Type 2070 Front Panel Assembly Requirements

All tested ATC 2070 requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.6 ATC Type 2070 Power Supply Module Requirements

All tested ATC 2070 requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.7 ATC Type 2070 VME Cage Assembly Requirements

This module/device presented no testable ATC 2070 requirements as the versions of the 2070 controller available for testing in HCTX did not utilize the VME Cage.

4.4.8 ATC Type 2070 Peripheral Equipment Requirements

This module/device presented no testable ATC 2070 requirements as the versions of the 2070 controller available for testing in HCTX did not require the use of the 2070 Peripheral Equipment.

4.4.9 ATC Type 2070-2N NEMA Field I/O Module Requirements

HCTX does not use the NEMA version of the controller, and as such, there were no testable ATC 2070 requirements.

4.4.10 ATC Type 2070-4N NEMA Power Supply Module Requirements

HCTX does not use the NEMA version of the controller, and as such, there were no testable ATC 2070 requirements.

4.4.11 ATC Type 2070-8 NEMA Field I/O Module Requirements

HCTX does not use the NEMA version of the controller, and as such, there were no testable ATC 2070 requirements.

4.4.12 ITS Cabinet General Requirements

Item	88
Page	20
Paragraph	**3.2.15.1 Indicators**
Comment	ITS Cabinet Requirement 88 (LED color and design) was not met on at least a few older modules present in the Harris County lab, but these modules were not in use in the field. The operational need for this requirement was verified via demonstration with an older EDI Switch Pack that was found in the lab.
Recommendation	Add non-reflective to the text of the standard as the purpose is to ensure proper viewing even in direct sunlight.
Item	92
Page	20
Paragraph	**3.2.16.1 Connectors – General**
Comment	ITS Cabinet Requirement 92 (mating connector keying) was not met for DB25, but plugging this board into the wrong slot will not cause any type of hazard or equipment damage. Generally, all situations where damage or hazard could occur were covered by and met this requirement, but it isn't obvious without analyzing the design.
Recommendation	Identify clearly those connectors in which this requirement is applicable.

4.4.13 ITS Cabinet PC Board Requirements

This module/device presented no testable ITS Cabinet requirements.

4.4.14 ITS Cabinet Models 200 and 204 Requirements

Item	164
Page	39
Paragraph	**4.1.1.2 Models 200 and 204 General**
Comment	ITS Cabinet Requirement 164 (screw head types) was not met. It is clear that the operational need—avoiding a serviceperson having to go back to his vehicle to obtain another type of screwdriver—was appropriate, but given that communication ports only come in slotted type screws, it is unlikely that this requirement can be or will be met.
Recommendation	Delete this clause from the standard or at a minimum, specifically identify the allowable screw head types, i.e., slotted, Phillips, or phil/slot and the expected size range, i.e., #0-#2.

4.4.15 ITS Cabinet Model 200 Switch Pack Unit Requirements

Item	181
Page	40
Paragraph	**4.2.1.5 Models 200 Switch Pack Unit General**
Comment	ITS Cabinet Requirement 181 (switch indication LED placement) was not met on any device found in the lab at Harris County. Furthermore, it was not met on any of the newer devices found in the lab, devices that had been "approved for use" by Caltrans. The typical placement of the LEDs for all devices examined was ¾ inch apart, versus the 1 inch stated in the standard.
Recommendation	Correct the standard to reflect the dimensions being used.

4.4.16 ITS Cabinet Model 204 Flasher Unit and Model 205 Flash Transfer Unit Requirements

All tested ITS Cabinet requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.17 ITS Cabinet Model 212 Monitor Unit (CMU) Requirements

All tested ITS Cabinet requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.18 ITS Cabinet Model 214 Auxiliary Monitor Unit (AMU) Requirements

All tested ITS Cabinet requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.19 ITS Cabinet Model 216-12 & 216-24 Power Supply Unit Requirements

All tested ITS Cabinet requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.20 ITS Cabinet Type 218 – Serial Interface Unit (SIU) Requirements

Item	552
Page	92
Paragraph	**4.7.14.7 Serial Ports**
Comment	ITS Cabinet Requirement 552 (port labeling) was not met. The standard appears to be discrepant, since the ports are neither identified nor labeled as specified in the text as shown on the drawings in the standard.
Recommendation	Correct the standard so that the drawings and the text match the currently-implemented devices.
Item	553
Page	92
Paragraph	**4.7.14.7 Serial Ports**
Comment	ITS Cabinet Requirement 553 (port labeling) was not met. The standard appears to be discrepant, since the ports are neither identified nor labeled as specified in the text as shown on the drawings in the standard.
Recommendation	Correct the standard so that the drawings and the text match the currently-implemented devices.

4.4.21 ITS Cabinet Loop Detector General Requirements

All tested ITS Cabinet requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.22 ITS Cabinet Housing Requirements

All tested ITS Cabinet requirements in this section of the standard were met and no findings were attributed to this portion of the standard.

4.4.23 ITS Cabinet Rack Cage Requirements

This module/device presented no testable requirements.

4.4.24 ITS Cabinet Assembly Requirements

Item	950
Page	154
Paragraph	**6.4.1.6 Connector Sockets**
Comment	ITS Cabinet Requirement 950 (socket mounting dimension) was not met. The dimension was correct, but the wording was inverted. The verbiage should say, "7.50 from the back panel to the front panel of the unit" versus what is shown in the standard.
Recommendation	Correct the standard.

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5.0 Conclusion

As stated in the Section 3.0 of this final report, the overall goal of the ITS Standards Testing Program is to assess and evaluate the suitability, effectiveness, interoperability and interchangeability of standards. The measure of these three key elements is essential in understanding whether or not a particular standard is ready for field use. The conclusion is therefore stated in terms of these measures.

5.1 Suitability

In terms of suitability, while the standard doesn't explicitly define user requirements, which we have identified as a finding, through the interview and testing process, the ISTT was satisfied that the products produced as a result of the standards do indeed meet the needs of the deploying agency. The test site, Harris Co., TX, represents a major consumer of devices built to these standards. As noted in the Introduction, the individuals cited for these conclusions – Mr. Johnson, representing HCTX, and Mr. Iniguez, representing both CalTrans and the working group – have numerous years of experience in this area and would both be considered experts in this subject matter. As such, their acceptances of the standard support the conclusion of suitability.

5.2 Effectiveness

In terms of effectiveness, the standards fully meet the measure of effectiveness in that they are an effective solution to satisfy the needs of the user; however, there is some concern in the ability of newcomers to this community to easily grasp and adhere to these standards. These standards represent an evolutionary process that has involved many stakeholders over many years and has its origins in similar, but more site-specific standards. Thru years of refinement, these standards have come to represent the best practices and capabilities of a consortium of stakeholders. These are all positive contributions to the standard.

What has not been fully determined is the ability of a newcomer to, without ambiguity, design, and build devices that conform to the standard, and provide for the end-user agency needs. While it is was not within the scope of this specific effort, it might be of interest to USDOT and the working groups to interview a vendor and/or agency who does not have the lengthy background in order to uncover any findings along this path.

5.3 Interoperability and Interchangeability

In terms of interoperability and interchangeability, over the course of evaluation and testing, we had the opportunity to witness first hand, product from multiple vendors configured into systems that performed their intended function. Furthermore, we were able to witness hot-swapping of components from multiple vendors, again, with no exceptions to their intended purpose. This capability was quite impressive and ultimately, was the major driver for the creation of these standards, and proof positive as to the benefits standardization can bring.

5.4 Other Key Observations

As a next step, in order to assure conformance to the standard can be met, and for the benefit of the newcomer to the standards community, and to correct the deficiencies in the standard, we offer the following thoughts:

- Use of the Systems Engineering Process to produce user needs is of value and should be employed throughout the system life cycle. The standard could benefit from the inclusion of a tailored requirements verification matrix, which would aid the agency and vendors in determining the type and method for how to satisfy each of the requirements embodied within the standard. The ISTT, thru its analysis process, has generated a first pass of this type of matrix, as shown in Appendix B. While it is by no means 100% accurate, we attempted to both identify the requirement type, but also the method (analysis, demonstration, inspection, and test) to verify conformance to the requirements.
- A thorough review of all drawings should be conducted to ensure that they are consistent with the text and that duplicate, sometime conflicting requirements are corrected.
- Subjective statements should be examined and removed, or at a minimum, qualified as such.
- Separating design and procurement items from actual performance requirements should be considered.
- The Test Section Area (Section 3.0) should be corrected to truly represent the needs and requirements for the device, or should be removed.

The bottom line, based on the limited testing, but strong historical evidence and thorough interviews, is that the ATC 2070 and ITS Cabinet Standards do indeed meet the goals of the ITS Standards program and should be considered a success for satisfying the stakeholder needs. The majority of the findings contained herein are minor, and have more to do with documentation errors and inconsistencies than they actually have to do with substantive implementations or errors in design against the features of the standard.

Appendix A: ATC 2070 / ITS Cabinet Interview Questionnaire

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General Questions

Question	Response	Remarks / Analysis / Action Items
1. Completeness		
1.1. Were there other standards used?	HCTX: Such as NETC, there are specific guidelines for roads and traffic control, including how to lay out the lanes in an intersection. CalTrans: There are also industry standards for electronics, AREMA, etc.	This question, while asked, was not on the printed copies of the questionnaire.
1.2. Are their any legacy requirements, over and above what is included in the standard that should be included in a standard?	HCTX: Two kinds of things, traffic control software programs and components used in the cabinet system, e.g., switchbacks relays, etc. When these legacy items change in form factor, we may have to actually update the standard.	The legacy standards are currently imbedded in the standard, sort of an unspoken portion of the standard?
1.3. Are there any tasks that you'd like to accomplish that are not covered by the standard?	HCTX: We are currently looking at a series of less complex boxes, which might hang on poles. How do we handle that, since we'd need different packaging?	The form factor for the ITS cabinet would not work in this case.
1.4. Are there other customizations that you have to implement to get the items covered by the standard to fit?	HCTX: Yes. The impact of going to LED signals, for example, effects the form factor in the cabinet, due to things like amperage, etc.	Equipment designed to run at 10 amps simply doesn't run well at 1 amp or less. This is more of a cabinet issue versus a controller issue.
1.5. Is there capability in the 2070 that you choose not to use?	HCTX: Not really.	

Question	Response	Remarks / Analysis / Action Items
1.6. What configurations of 2070 have you deployed?	HCTX: We're using LN, versus NEMA cabinets. We're basically using a 2070 with a field I/O module, but we don't use the modem stuff, since we're mostly Ethernet. CalTrans: We only use the L version.	The Ethernet capability and the use of serial versus parallel interface seem pretty important.
1.7. Are there any things in the standard that you cannot envision ever using?	HCTX: The answer is, most of the power supply stuff (as mentioned regarding the burgeoning use of LEDs) and the modem capability, since we only use Ethernet capability, might be examples.	
2. Clarity		
2.1. Are the standards clear?	HCTX: How can we say different? I can show you a volume with many, many pages of comments during the early iterations of the standard. This leads to the current clarity. CalTrans: Because this is a specific standard for a specific industry, that makes this usage better. In fact, one of our goals was the clarity of standard. Siemens: There was a lot of interaction between vendors and standards creators to aid the clarity.	HCTX mentioned that it is important for people to actually visit CalTrans to "see" what they do.
2.2. Are the standards unambiguous?	HCTX: No. Because of the process of iterative refinement, as noted above.	
2.3. Are there any messages/frames/elements that are confusing or inappropriate in the standards?	HCTX: If anything, there might be too much detail in places.	

Question	Response	Remarks / Analysis / Action Items
2.4. Were there any areas of the standards that were not understandable? (their purpose or implementation)	HCTX: Yes, but we're working on clearing them up, as mentioned above.	
2.5. Were there any messages or elements of the standards that were open ended or could be interpreted in more than one way?	Siemens: Yes, there "were" but we closed a lot of them over the iterative process that we've been on for so long.	How do we convey the concept that one needs to "view" the process at a seasoned vendor like CalTrans, before they attempt to implement the standard. A recurring theme raised by Johnson, is that there is "informative knowledge" that a group planning to implement the standard would gain by, for example, visiting CalTrans and watching. There appear to be certain items specified in the standard that have hidden reasons. For example, HCTX related that if the material for the front latch is changed, the form factor of the latch is different, and interoperability is compromised. However, in the standard, it simply says, "use material XXX" without any mention of such a reason. How should such information be communicated, if at all?
2.6. Were there any areas of the standards where you needed or sought guidance or clarification? • what's the data purpose/meaning • how it is encoded • units of measure • etc.	No.	
3. Effectiveness		
3.1. Are the standards effective in the exchange of information of a traffic management system to other centers or information service providers?	HCTX: Yes. CalTrans: Yes.	Mr. Johnson was not exactly sure what the question was intended to address. The ISTT pressed with "were there parts of the standard that led to over-design?" The answer was still no.

Question	Response	Remarks / Analysis / Action Items
3.2. What area could messages/frames/elements be added or changed to improve the effectiveness of the standards in providing traffic management information?	HCTX: No. (When we selected Motorola processors chips there were some shortcomings, but that choice led us down an architecture path that we've followed, for better or worse.) Siemens: All I could think of might be that as we go along, we keep adding new drivers and support for additional serial speeds, etc.	
3.3. Did the use of the ITS standards simplify the procurement specification process?	HCTX: Yes. (Harris County recently completed documentation for cataloging all our procurements. We used the standard for developing that document.)	
3.4. To what level of detail were the ITS standards specified in procuring your system? • specific standards / versions • specific messages / data elements • etc.	HCTX: We actually look at the standard to determine what one might need, e.g., a 2070 with certain components, but you have to be more specific than saying "just give me a 2070." But it might be a weakness of the standard that a user is required to have some knowledge of what he needs, knowledge that is not necessarily in the standard itself. CalTrans: Everything we might need is specified in the standard, but we also refer to a particular version of the 2070, say an L version, which is also specified in standard.	The "L" version is specified on page 48-49 of the standard. It appears that if one was in need of detail upon what to buy, they would need to not only have the standard, but also some other, apparently unspecified understanding of what might be needed for their particular implementation. It appears that the customer might need to have understanding that cannot be acquired from reading the standard only! One also needs to determine where "user options" end and information suitable for a standard begins.
3.5. Did the use of the ITS standards simplify your life cycle process for requirements, design, build, evaluate and deploy?	HCTX: Yes.	

Question	Response	Remarks / Analysis / Action Items
4. Suitability		
4.1. Are the messages/frames/elements suitable for implementation of the traffic management system?	Yes. HCTX: In some cases, this process cost more.	The issue was more due to the costs of developing the specification itself.
4.2. Are there any areas of the standard that seem either deficient or out of scope of its purpose?		Skipped.
4.3. Are there any messages/frames/elements that could be added or changed that would improve the suitability of the standard in providing traffic management information?		Skipped
4.4. Do you feel that there were any programmatic, technical or operational impacts on you (positive or negative) because of the use of the ITS standards?		Skipped
4.5. Did you adapt your operational needs to the standards? Were adaptation recognized as having a positive or negative effect?		Skipped
5. References		
5.1. Were the references to other external documents or material listed in the standards, if any, complete and useable?	Siemens: We tried to make sure that we had only normative references to specifications. In fact we hired an editor.	
5.2. Were there any superfluous references?		Skipped

Question	Response	Remarks / Analysis / Action Items
5.3. Did you or members of your team consult any of the external references and, if so, did they contribute positively to your understanding of the standards?	HCTX: To some extent one has to be conversant with the external references. There are issues buried in the standard that relate to experiences we've gained due to the fact this standard specifies a "legacy" item and reflects the "learnings" thereof. CalTrans: Most of the external references are industry standards, and so one needs to understand those to properly use the standard.	Additional question from the ISTT: I didn't see a "timing diagram" or anything like that. How is that type of information specified? Additional embellishment from the ISTT: It seemed that you were very specific in the standard, displaying some implicit context that is not always provided in the standard. How is this conveyed? It seems clear that as implementers who are also standard developers, the guys that we interviewed are not really equipped to generally address this concern.
6. Terms and Definitions		
6.1. Did the glossaries of terms, definitions and acronyms meet your needs in understanding and using the standards?		Skipped.
6.2. Are there any definitions, terms or acronyms that need to be added or revised?		Skipped.
6.3. Were there any superfluous definitions, terms or acronyms?		Skipped.
7. Figures and Tables		
7.1. Did the figures and tables in the standards aid in your understanding of the standard and its intended use?	HCTX: In the cabinet area specifically, no. We've been careful to include all that is needed, including pictures if needed. Deployment forced the addition of some of the pictures we now have.	A recurring theme throughout this process was the fact that the current standard reflects a lot of iteration.
7.2. Are there any figures or table, terms that need to be added or revised?	HCTX: Not really.	

ATC Type 2070 General Requirements Questions

Question	Response	Remarks / Analysis / Action Items
8. Components		
8.1. Do you use socket mounts for any devices?	CalTrans: The socket mounts were used at one time, since the level of maintenance level required it. HCTX: In the 170 world, the program was put on a memory chip that required a socket. In today's world a socket is not needed, really. Additionally, the early drivers were "current hogs" so sockets were required.	Another legacy issue! This part of the standard simply leaves a "door open" for an implementer to use sockets if needed.
8.2. If not, why not?		Skipped.
8.3. Would you characterize your components as easily accessible, replaceable and identifiable for testing and maintenance?	HCTX: This was an issue with using daughter boards and non-surface mounted parts. Given that ICs cannot really be replaced any more, accessibility is likely not that important anymore. CalTrans: It might be that these types of specs are not as applicable.	"With the advent of surface-mount technology this requirement is easier / harder to judge?"
8.4. Upon what criterion (or criteria) do you base this characterization?		Skipped.
8.5. Would you describe all the fuses in the device as easily accessible and removable without use of tools?	CalTrans: This issue relates to the fact that the amount of time required to service a device is small, or has to be.	The user requirement is that things be serviceable in a relatively fast timeframe.
8.6. Upon what criterion (or criteria) do you base this characterization?	CalTrans: We don't have fuses on individual components, but the requirement is about the speed of being able to service the device. There is only one fuse in the 2070 anyway.	There appears to be implied knowledge at work here. There were not any obvious objective criteria at work here.

Question	Response	Remarks / Analysis / Action Items
9. Mechanical (1:16:30)		
9.1. Would you characterize all the harnesses in the device as neat, firm and properly bundled?	HCTX: That one is subjective. The problem is that if one doesn't bundle stuff properly there is obstruction for serviceability. What I've seen in some places is the use of pictures to illustrate what "properly bundled" looks like. CalTrans: The other part of this requirement is that we state in other places that everything is to be of "the highest workmanship and quality" and clearly poorly bundled cables do not reflect high workmanship.	Many of these are "boilerplate" statements, intended to create a high-quality device.
9.2. Upon what criterion (or criteria) do you base this characterization?		The interviewees offered no way to put this in objective terms, but felt pretty strongly that the recurring theme of workmanship was sufficient for these purposes, even though it might appear to be subjective.
9.3. Would you say that all assemblies in the device are modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs?	HCTX: We spec the location of devices. If you follow those dimensions, the assemblies will be easily replaceable.	
9.4. Upon what criterion (or criteria) do you base this characterization?	Same as above.	
9.5. Would you characterize the permanent label affixed to the inside near and center floor of the Type 2070 unit chassis as "easy to read"?	CalTrans: The issue goes back, and this applies even to the previous one, to QPL, i.e., quality workmanship. HCTX: You could get around this by using a picture.	
9.6. Upon what criterion (or criteria) do you base this characterization?	Same as above.	

Question	Response	Remarks / Analysis / Action Items
9.7. Would you say that the PCBs in the device slide smoothly in their guides while being inserted into or removed from the frame and fit snugly into the plug-in PCB connectors?	HCTX: We're depending upon a relatively tight fit to keep these modules from slipping out. This is also another reason why a person would benefit from attending the CalTrans "course." If the dimensions are right, one shouldn't have a problem anyway. CalTrans: And if someone refers to this and calls us on it, we will likely fall back on the issue of "workmanship" and leave it at that.	The interviewees kept going back to "why" and justifying it, but these questions are trying to understand the "what" and how it is measured, quantified, communicated, and objectively known.
9.8. Upon what criterion (or criteria) do you base this characterization?		
9.9. How do you verify that the resistance between any two isolated, independent conductor paths is at least 100 Megohms when a 500 VDC potential is applied?	HCTX: There is a special tool used for measuring this.	
9.10. Do you verify the quality of all the solder joints on each PCB?	HCTX: Most times, we notice that when modules start to fail, one can find cold solder joints on it. Again, if one examines the ISO requirements he can find a definition that is pertinent for this specification.	If ISO covers a bunch of these types of GMP, then maybe ISO should be referenced, but it is currently not cited. The conflict with this approach, is that the devices are being manufactured by small companies for whom meeting the requirements of ISO would be an undue burden. As a consequence, some of the ISO-type requirements are included and the implementers simply work with the vendor to understand how to meet it.
9.11. If not, why not?		
10. Quality Control		
10.1. Did you lot sample all components?	HCTX: We don't require this, but we expect devices to work and if they don't we may require some verification here.	

Question	Response	Remarks / Analysis / Action Items
10.2. If not, why not?		
10.3. Did you sample at a rate higher than on a lot-by-lot basis?		
10.4. If so, why?		
10.5. Did you complete electrical, environmental and timing compliance testing on each module, unit, printed circuit or subassembly?	CalTrans: We monitor the failure rate to determine if the devices perform at higher than a 3% failure rate. If they do not, we sample higher. HCTX: We don't buy devices in "lots" since we use a contractor. We send devices directly to the field and expect them to work. We do bring every controller in to see if it works, although we don't test them as explained. However, if devices begin to fail, we need to the specification to determine if they are meeting the requirements.	
10.6. If not, why not?		
10.7. Did you test components as a complete controller assembly?	HCTX: No.	
10.8. If not, why not?		
10.9. Did you inspect housing, chassis, and connection terminals for mechanical sturdiness?	HCTX: We probably will during the approval process, but not every single one. We do not require the vendor to produce any report of his findings.	Mr. Johnson's point of view is that requiring the vendor to produce paperwork is of limited value, since the vendor could have simply created it out of thin air. However, if an item begins to fail, he can always test it against the specification.
10.10. If not, why not?		
10.11. Did you electrically test harnessing to sockets for proper wiring sequence?	HCTX: Yes.	

Question	Response	Remarks / Analysis / Action Items
10.12. If so, on what periodicity did you conduct these tests, and how did you arrive at it?	HCTX: 100% Siemens: If you didn't test at this level, you would have a failure and not know where to start.	There is a lot of detail in the specification for the purpose of helping vendors be able to produce good product.
10.13. If not, why not?		
10.14. Did you visually and physically inspect the equipment shall to assure proper placement, mounting, and compatibility of subassemblies?	HCTX: Yes. This also a part of GMP.	CalTrans has a check-list and test-plan for this that is not included in the standard. Harris County uses CalTrans as a de facto qualifying body.
10.15. If so, on what periodicity did you conduct this inspection, and how did you arrive at it?		
10.16. If not, why not?		
10.17. Does your process for handling defects or deficiencies found by the inspection system involving mechanical structure or wiring include returning the items through the manufacturing process or special repair process for correction?	HCTX: Yes.	This is defined as part of the warranty issues. If the device is out of warranty, I am at a loss.
10.18. If not, why not?		
10.19. Under what conditions do you allow PCB flow soldering a second time?	HCTX: We don't address this since we wouldn't know how many times a board has been soldered anyway!	It is not clear if this should be in the standard or not, and interviewing the clients did not make this issue any clearer.
10.20. Are there any conditions under which you allow a PCB to be flow soldered more than twice?	HCTX: We have no way to tell how many times a board has been soldered, but we are trying to preclude errors before they happen by setting criteria like this. However, if I get into problems, I have a legitimate reason to question this area.	
10.21. If not, why not?		
10.22. If so, why?		

Question	Response	Remarks / Analysis / Action Items
11. Electrical, Environment, and Testing (3:53:25)		
11.1. Did you follow the ATC 2070 standard with regard to generating quality control / final testing reports?	HCTX: I don't require a report. I think we need to do more in this area. CalTrans requires a report on the controller. CalTrans: Yes.	There is a perception by HCTX that no one would ever submit a test report reflecting any failures anyway. As such, he doesn't feel that receiving a set of test reports adds any value. **Why is this requirement and requirements like it, in the standard?** Since CalTrans tests everything anyway, it could be argued that the standard's requirement for testing reports seems superfluous. However, California is unique in this regard.
11.2. If not, why not?		
11.3. Specifically, did your reports include: Design Acceptance testing of all supplied components?	Siemens: Yes. HCTX: Same as above.	
11.4. If not, why not?		
11.5. Specifically, did your reports include: Physical and functional testing of all modules and items?	Siemens: Same as above. HCTX: Same as above.	
11.6. If not, why not?		
11.7. Specifically, did your reports include: Environmental testing report(s) for all equipment?	Siemens: Same as above. HCTX: Same as above.	
11.8. If not, why not?		

Question	Response	Remarks / Analysis / Action Items
11.9. Did you follow the ATC 2070 standard with regard to high-energy and high repetition transients?	Siemens: We do all the tests that are non-destructive. HCTX: Same as above. CalTrans: Same as above.	It is clear that this standard is very mature, so many of these questions are irrelevant.
11.10. If not, why not?		
11.11. Do you believe that the ATC 2070 standard fully covered the important factors with regard to transients and power service?	Same as above.	
11.12. If not, why not?		
11.13. Did you follow the ATC 2070 standard with regard to temperature and humidity testing?	Same as above.	
11.14. If not, why not?		
11.15. Do you believe that the ATC 2070 standard fully covered the relevant and/or correct factors with regard to temperature and humidity testing?	Same as above.	
11.16. If not, why not?		
11.17. In selecting your instrumentation for conducting the environmental tests, what criteria did you follow?	HCTX: You need a pretty sophisticated chamber to even accomplish these tests. And given the fact that we require a time cycle and other things, you really need a high quality chamber.	
11.18. Did you follow the procedures outlined in the ATC 2070 standard fully for your environmental testing, or did you modify them?	Same as above.	
11.19. Why or why not?		
11.20. If so, what specific changes, or types of changes did you make?	Same as above.	

Question	Response	Remarks / Analysis / Action Items
11.21. Can you provide a full report for each of the environmental tests you ran and relate it to the relevant portions of the ATC 2070 standard?	Same as above. Siemens: For manufacturing, it doesn't look like a formal report, but more a check-list of all the tests run.	Follow-Up Question: Let's say you noticed that several of the controllers you've installed from a given vendor fail on a particularly cold day. How do you respond? HCTX: Well, it's a warranty item. If it fails I call the manufacturer to fix it and I expect him to fix it. I still likely wouldn't ask for a test report. (Again, if test reports aren't required why are they "required"?)
11.22. Of what value, if any, were the environmental procedures listed in the ATC 2070 standard?	Same as above.	
11.23. Did you follow the procedures outlined in the ATC 2070 standard fully for your vibration testing, or did you modify them?	Same as above.	
11.24. Why or why not?		
11.25. Can you provide a full report for each of the vibration tests you ran and relate it to the relevant portions of the ATC 2070 standard?	Same as above.	
11.26. Of what value, if any, were the vibration testing procedures listed in the ATC 2070 standard?	Same as above.	
11.27. Did you follow the procedures outlined in the ATC 2070 standard fully for your shock testing, or did you modify them?	Same as above.	
11.28. Why or why not?		
11.29. Can you provide a full report for each of the shock tests you ran and relate it to the relevant portions of the ATC 2070 standard?	Same as above.	

Question	Response	Remarks / Analysis / Action Items
11.30. Of what value, if any, were the shock testing procedures listed in the ATC 2070 standard?	Same as above.	
11.31. Did you follow the procedures outlined in the ATC 2070 standard fully for your cabinet assembly testing, or did you modify them?	Same as above.	
11.32. Why or why not?		
11.33. Can you provide a full report for each of the cabinet assembly tests you ran and relate it to the relevant portions of the ATC 2070 standard?	Same as above.	Side issue for all testing: CalTrans is the only authority who has created an "acceptance test" for verifying the operation of the overall unit. It is not clear how HCTX verifies the overall operation of a unit, outside this CalTrans "DAT" test. HCTX seemed to feel that it makes sense for CalTrans to become a "certification laboratory" for the industry. Otherwise it is not clear that the standard provides real value with regard to all these testing requirements.
11.34. Of what value, if any, were the cabinet assembly testing procedures listed in the ATC 2070 standard?	Same as above.	
11.35. A number of the specific areas of testing outlined in the ATC 2070 standard reflect that they are "under consideration." How did you approach meeting these portions of the ATC 2070 standard?	HCTX: We perform discrete tests for individual components, and therefore there are no guidelines for this area. These sections need to go away. Much of this is simply a carry-over from a prior version.	

ATC Type 2070 Controller-Specific Requirements Questions

Question	Response	Remarks / Analysis / Action Items
12. Type 2070-1 CPU Module (5:11:54)		
12.1. Did you prepare a separate software design specification, in addition to the software design specifications listed in the ATC 2070 standard?	Siemens: No. HCTX: No.	Again, the use of the DAT, developed by CalTrans, was mentioned during the discussions. The DAT is actually called out in Section 4.2.7.5.1. There was disagreement between Mr. Johnson (HCTX) and Mr. Iniguez as to if the DAT is always "required" versus never left in a 2070 controller. One of the users, in fact, one of the key users at HCTX had never used the DAT. It appears that now HCTX will begin, as a result of this discussion and interview, to use the DAT. Either way, the wording in the standard needs to be reworded to reflect the state-of-the-art, including the use of a DAT, from where it comes, and how it is used. Although CalTrans has supervised the development of the DAT, it is a product derived from a number of manufacturers.
12.2. Why or why not?		
12.3. Did you find that the software design specifications listed in the ATC 2070 standard were adequate to design and build the device in question?	HCTX: Yes.	
12.4. Why or why not?		
12.5. Does the first executable file in the boot image of the default directory, designated as "Sysgo", operate as specified in the ATC 2070 standard?	HCTX: Yes, with the caveat that we currently do not use the DAT, as per the previous discussions.	
12.6. Why or why not?		

Question	Response	Remarks / Analysis / Action Items
13. Type 2070-2 Field I/O Module (FI/O)		
13.1. What definition did you use for the terminology "glitch" with regard to the performance of a Parallel I/O Ports output circuit?	HCTX: Section cleaned up already.	Apparently, v02.03, which the ISTT had been given to evaluate, was not the latest "internal" version, which is v02.06. This later version reflects some improvements, of which this is one.
13.2. Why did you use this definition?		
13.3. Did you follow the standard's recommendation with regard to the creation and supply of options with additional features, defined as: **Option 3A** – FPA controller, two keyboards, AUX switch, alarm bell and Display A **Option 3B** – FPA controller, two keyboards, AUX switch, alarm bell and Display B **Option 3C** – System Serial Port 6 Lines, isolated and vectored to Connector C60S.	HCTX: For reasons of standardizing, we do not want deviation from the things we list.	
13.4. If not, why not?		
13.5. If so, are you clear about the purpose of this specification? (What is it?)	HCTX: Same as above.	
13.6. How did you meet, or verify that you met, this keyboard specification? "Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 milliseconds following contact closure."	HCTX: Yes.	
13.7. Did you follow the ATC 2070 standard with regard to all the details in the Display Section 4.4.4?	HCTX: Yes.	

Question	Response	Remarks / Analysis / Action Items
13.8. Was the section Display Section 4.4.4 of the ATC 2070 standard helpful to you in your development?	HCTX: Yes.	In the view of HCTX, much of this stuff is important because this "is a functional display" so changes will effect usage.
13.9. Did you also create your own system design specification relative to the types of items specified in the Display Section, 4.4.4, portion of the ATC 2070 standard?	HCTX: Yes.	
13.10. Why or why not?		
13.11. Did you follow the ATC 2070 standard with regard to all the details in the Power Supply section?	Siemens: Yes.	One of the underlying premises used in developing the standard was the belief that it is better to put as much detail in the standard itself, and avoid the user having to look in some other document to find answers he might need. The key user from HCTX noted that "as long as I knew what I was doing" I could follow the specification and get what I was after. It is not clear what "know what I was doing" means in a more general sense.
13.12. Was the Power Supply section of the ATC 2070 standard helpful to you in your development?		
13.13. Did you also create your own system design specification relative to the types of items specified in the Power Supply section of the ATC 2070 standard?		
13.14. Why or why not?		

Question	Response	Remarks / Analysis / Action Items
14. Chapter Details – Drawings – (Type 2070 Controller)		
14.1. Exactly what use did you make of the drawings listed in this section?	HCTX: When we use three decimal places, we are specifying a more important specification, but that is not actually spelled out in the standard. CalTrans: We don't normally specify the "off-the-shelf" parts, such as the keyboard too closely.	Again, the current drawing structure reflects the fact that the current standard reflects the end of a long iteration process. It is also pretty clear that interviewing the developer of the standard is not suitable for addressing many of these questions in an objective way. It is also pretty clear that because of this challenge, the amount of "implied knowledge" inherent in the standard cannot be ascertained via these interviews!
14.2. Did you generate your own drawings similar to these?	CalTrans: All manufacturers normally submit lots of drawings that we can use to verify that what they are going to produce will meet our needs. HCTX: The basic thought process is that a manufacturer must place all the items on the front, and exactly where is not specified by the standard but given the number of items, they can only end up in certain places.	This represents the first time in the entire interview process where it was admitted that the standard did not provide all information needed or produced by a manufacturer and that a manufacture would have to produce additional information.
14.3. Why or why not?	CalTrans: For example, they should submit s theory of operation, but such is not described in the standard. (Follow up question: Then how does a manufacturer know to submit one?)	It seems pretty clear that items like a theory of operation are required by the client, but not specified in the standard.
15. Chapter Details – Drawings – (Type 2070-6 A & B)		
15.1. Exactly what use did you make of the drawings listed in this section?		Skipped due to mature nature of standard.
15.2. Did you generate your own drawings similar to these?		Skipped due to mature nature of standard.
15.3. Why or why not?		

Question	Response	Remarks / Analysis / Action Items
16. Chapter Details – Drawings – (NEMA Module)		
16.1. Exactly what use did you make of the drawings listed in this section?		Skipped due to mature nature of standard.
16.2. Did you generate your own drawings similar to these?		Skipped due to mature nature of standard.
16.3. Why or why not?		

ITS Roadside Cabinet General Requirements Questions

Question	Response	Remarks / Analysis / Action Items
17. Components		
17.1. Do you use socket mounts for any devices?		These questions were deemed unnecessary as they have been answered in previous sections. Furthermore, given the fact that the standard being tested is the result of many, many iterations – resulting in what could only be termed a "legacy" product – and is being employed by the developers anyway, such questions as these will provide little, if any, feedback on the standard's appropriateness.
17.2. If not, why not?		
17.3. Would you characterize your components as easily accessible, replaceable and identifiable for testing and maintenance?	Same as above.	
17.4. Upon what criterion (or criteria) do you base this characterization?	Same as above.	
17.5. Would you describe all the fuses in the device as easily accessible and removable without use of tools?	Same as above.	

Question	Response	Remarks / Analysis / Action Items
17.6. Upon what criterion (or criteria) do you base this characterization?	Same as above.	
17.7. Did you experimentally verify that the life of all components, operating continuously (24 hours per-day, 365 days per-year) in their circuit application, was ten years or longer?	Same as above.	
17.8. If so, how did you verify this?	Same as above.	
17.9. If not, why not?		
18. Mechanical		
18.1. Would you characterize all the harnesses in the device as neat, firm and properly bundled?	Same as above.	
18.2. Upon what criterion (or criteria) do you base this characterization?	Same as above.	
18.3. Would you say that all assemblies in the device are modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs?	Same as above.	
18.4. Upon what criterion (or criteria) do you base this characterization?	Same as above.	
18.5. Would you characterize the permanent label affixed to the inside near and center floor of the Type 2070 unit chassis as “easy to read”?	Same as above.	
18.6. Upon what criterion (or criteria) do you base this characterization?	Same as above.	

Question	Response	Remarks / Analysis / Action Items
18.7. Would you say that the PCBs in the device slide smoothly in their guides while being inserted into or removed from the frame and fit snugly into the plug-in PCB connectors?	Same as above.	
18.8. Upon what criterion (or criteria) do you base this characterization?	Same as above.	
18.9. How do you verify that the resistance between any two isolated, independent conductor paths is at least 100 Megohms when a 500 VDC potential is applied?	Same as above.	
18.10. Do you verify the quality of all the solder joints on each PCB?	Same as above.	
18.11. If not, why not?		
19. Quality Control		
19.1. Did you lot sample all components?	Same as above.	
19.2. If not, why not?		
19.3. Did you sample at a rate higher than on a lot-by-lot basis?	Same as above.	
19.4. If so, why?		
19.5. Did you complete electrical, environmental and timing compliance testing on each module, unit, printed circuit or subassembly?	Same as above.	
19.6. If not, why not?		
19.7. Did you test components as a complete controller assembly?	Same as above.	
19.8. If not, why not?		

Question	Response	Remarks / Analysis / Action Items
19.9. Did you inspect housing, chassis, and connection terminals for mechanical sturdiness?	Same as above.	
19.10. If not, why not?		
19.11. Did you electrically test harnessing to sockets for proper wiring sequence?	Same as above.	
19.12. If so, on what periodicity did you conduct these tests, and how did you arrive at it?	Same as above.	
19.13. If not, why not?		
19.14. Did you visually and physically inspect the equipment shall to assure proper placement, mounting, and compatibility of subassemblies?	Same as above.	
19.15. If so, on what periodicity did you conduct this inspection, and how did you arrive at it?		
19.16. If not, why not?		
19.17. Does your process for handling defects or deficiencies found by the inspection system involving mechanical structure or wiring include returning the items through the manufacturing process or special repair process for correction?	Same as above.	
19.18. If not, why not?		
19.19. Under what conditions do you allow PCB flow soldering a second time?	Same as above.	
19.20. Are there any conditions under which you allow a PCB to be flow soldered more than twice?	Same as above.	
19.21. If not, why not?		
19.22. If so, why?		

Question	Response	Remarks / Analysis / Action Items
20. Electrical, Environment, and Testing		
20.1. Did you follow the ITS Roadside Cabinet standard with regard to generating quality control / final testing reports?	Same as above.	
20.2. If not, why not?		
20.3. Specifically, did your reports include: Design Acceptance testing of all supplied components?	Same as above.	
20.4. If not, why not?		
20.5. Specifically, did your reports include: Physical and functional testing of all modules and items?	Same as above.	
20.6. If not, why not?		
20.7. Specifically, did your reports include: Environmental testing report(s) for all equipment?	Same as above.	
20.8. If not, why not?		
20.9. Did you follow the ITS Roadside Cabinet standard with regard to high-energy and high repetition transients?	Same as above.	
20.10. If not, why not?		
20.11. Do you believe that the ITS Roadside Cabinet standard fully covered the important factors with regard to transients and power service?	Same as above.	
20.12. If not, why not?		
20.13. Did you follow the ITS Roadside Cabinet standard with regard to temperature and humidity testing?	Same as above.	
20.14. If not, why not?		

Question	Response	Remarks / Analysis / Action Items
20.15. Do you believe that the ITS Roadside Cabinet standard fully covered the relevant and/or correct factors with regard to temperature and humidity testing?	Same as above.	
20.16. If not, why not?		
20.17. In selecting your instrumentation for conducting the environmental tests, what criteria did you follow?	Same as above.	
20.18. Did you follow the procedures outlined in the ITS Roadside Cabinet standard fully for your environmental testing, or did you modify them?	Same as above.	
20.19. Why or why not?		
20.20. If so, what specific changes, or types of changes did you make?	Same as above.	
20.21. Can you provide a full report for each of the environmental tests you ran and relate it to the relevant portions of the ITS Roadside Cabinet standard?	Same as above.	
20.22. Of what value, if any, were the environmental procedures listed in the ITS Roadside Cabinet standard?	Same as above.	
20.23. Did you follow the procedures outlined in the ITS Roadside Cabinet standard fully for your cabinet assembly testing, or did you modify them?	Same as above.	
20.24. Why or why not?		
20.25. Can you provide a full report for each of the cabinet assembly tests you ran and relate it to the relevant portions of the ITS Roadside Cabinet standard?	Same as above.	

Question	Response	Remarks / Analysis / Action Items
20.26. Of what value, if any, were the cabinet assembly testing procedures listed in the ITS Roadside Cabinet standard?	Same as above.	

ITS Roadside Cabinet Auxiliary Cabinet-Specific Requirements Questions

Question	Response	Remarks / Analysis / Action Items
21. Model 204 Flasher Unit and Model 205 Flash Transfer Relay Unit		
21.1. Did you experimentally verify that the flasher unit circuitry would operate in an open-circuit condition without load for 10 years minimum?	HCTX: We actually installed a 2 microfarad capacitor because it was impractical to operate without load. We really don't do this, but we might.	This section apparently should be updated to reflect that the capacitor is needed, but it was not clear from our discussions. It also seems pretty clear that this requirement is simply being met because there exist cabinets that have been running for over 10 years.
21.2. If so, how did you verify this?	Siemens: We brought in a guy to do a MTBF to predict these requirements. So when the initial ones came out we did actually need an MTBF specification.	This requirement and others like it should be reflected in the "boilerplate" of the standard, using an MTBF premise.
21.3. If not, why not?		
21.4. Did you experimentally verify that the switch would perform a minimum of 100,000 operations while switching a tungsten load of 1000 Watts at 70 degrees C?	HCTX: This seems like a good test to run, but these parameters, in terms of the number of operations.	The intent of this requirement should be to determine if the flasher could work all day flashing continuously. What is needed is a "reasonable expectation" for the timing.
21.5. If so, how did you verify this?		
21.6. If not, why not?		

Question	Response	Remarks / Analysis / Action Items
21.7. Did you experimentally verify that the DPDT contact points were capable of switching 20 Amperes or one Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitations?	HCTX: This is an actual design criterion. I'll have to determine if we resolved this, because I'm not sure. CalTrans: This is the "expected rating" of the device, as opposed to the output of a test.	It's not clear what the result of this discussion was, but it was clear that that the standard needs some work in this area.
21.8. If so, how did you verify this?		
21.9. If not, why not?		
22. Model 212 ITS Cabinet Monitor Unit (CMU)		
22.1. Did you prepare an input message design specification, in addition to the one listed in section 4.4 of the ITS Cabinet Monitor Unit standard?	Siemens: The detail in this unit is a result of a previous decision to make sure we could "mix and match" between CMU's and AMU's from different vendors. (If the same vendor always delivered the two units, we wouldn't need to be so detailed about the protocol.) We actually had a person build a CMU using the standard and it worked as expected, which verifies that the information is as needed.	There appears to be a need for a "white paper" that provides some insight about what HCTX has found in trying to reconfigure the ITS Cabinets to get them to work in certain situations.
22.2. Why or why not?		
22.3. Did you find that the message format specifications listed in section 4.4 of the ITS Cabinet Monitor Unit standard were adequate to design and build the device in question?	Same as above. Siemens: We originally did not have all this detail in the standard, but actually added it because the number of things we needed the CMU to do increased.	CMU also stand for "conflict monitor" and actually monitors the controller for conflicts. This leads to the intersection being put into "flash" without a person being able to tell why via the monitor. It is not clear how this should be addressed.
22.4. Why or why not?		

Question	Response	Remarks / Analysis / Action Items
23. Monitor Unit Serial Memory Key		
23.1. Did you implement the monitor unit serial memory key as specified in section 4.4.14 of the ITS Cabinet Monitor Unit standard?	HCTX: Yes. CalTrans: Yes.	
23.2. Why or why not?		
24. CMU Connector		
24.1. Did you use the pin-outs as specified in this section of the standard?	Same as above.	
24.2. Why or why not?		
25. Serial Bus #1 Frames		
25.1. Did you use the byte format as specified in this section of the standard?	Same as above.	
25.2. Why or why not?		
26. Type 218 – Serial Interface Unit (SIU)		
26.1. Did you design and implement Tracking Functions and Complex Output Functions as specified in the standard?	HCTX: These two features can be implemented without direct output from the controller. This is a behavior of the field output that I'm not very happy with. I've been arguing for years that I don't want these two features. Siemens: The programmer can choose to use this functionality or not. As such this is not a valid fear.	There are applications in the SIU that can influence the outputs regardless of what the controller says. The purpose of this functionality is to off-load work from the controller. This could result in some loss of closed-loop control.
26.2. Why or why not?		

Question	Response	Remarks / Analysis / Action Items
26.3. For example, in the case of a Tracking Function, does the implementation you used for the transmission of a definition follow this requirement:	Skipped.	
26.4. For example, in the case of a Tracking Function, does the implementation you used for the transmission of a definition follow this requirement:	Skipped.	
26.5. Did you exactly follow the block diagrams shown in Section 4.7.20 of the standard?	Skipped.	
26.6. If not, why not?		
27. Cabinet Details – Drawings		
27.1. Exactly what use did you make of the drawings listed in this document?	Previously answered.	
27.2. Did you generate your own drawings similar to those listed?	Previously answered.	
27.3. Why or why not?		

ITS Roadside Cabinet Detector Sensor Units, Elements & Isolators Requirements Questions

Question	Response	Remarks / Analysis / Action Items
28. Model 222 & 224 Loop Detector Sensor Unit		
28.1. Requirements in this section are posited in terms of a "vehicle" passing over or remaining over loop wires embedded in the roadway. How did you verify these requirements?	HCTX: We know how to do this because, again, it's a legacy issue.	
28.2. If you did not use an actual vehicle, how are you sure you met the requirements?	Skipped.	

Question	Response	Remarks / Analysis / Action Items
28.3. What does the terminology, "AGENCY licensed motor vehicles" refer to?	Skipped.	
29. Magnetic Detector		
29.1. Exactly how did you verify that the sensing element used in this device was "moisture proof"?	Skipped.	
29.2. Exactly how did you verify that the sensing element would detect a car traveling at all speeds between three and 80 miles per hour?	HCTX: We actually use a car.	

ITS Roadside Cabinet System Requirements Questions

Question	Response	Remarks / Analysis / Action Items
30. Cabinet Cage Configuration Drawings		
30.1. Exactly what use did you make of the drawings listed in this section?	Previously answered.	
30.2. Did you generate your own drawings similar to these?	Previously answered.	
30.3. Why or why not?		
31. Cabinet Details Drawings		
31.1. Exactly what use did you make of the drawings listed in this section?	Previously answered.	
31.2. Did you generate your own drawings similar to these?	Previously answered.	
31.3. Why or why not?		

Question	Response	Remarks / Analysis / Action Items
32. Cabinet Housing Construction		
32.1. Did you exactly follow the standard with regard to the construction of cabinet system housings?	Previously answered.	
32.2. Why or why not?		
32.3. If you deviated from the standard, what specific changes did you make?	Previously answered.	

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Appendix B: ATC 2070 / ITS Cabinet Tested Requirements

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B.1 ATC Type 2070 General Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
1	All sharp edges and corners shall be rounded and free of any burrs.	**3.1.6 Metals**			Inspection	**Design**
7	Within the circuit of any device, module, or Printed Circuit Board (PCB), electrical isolation shall be provided between DC logic ground, equipment ground and the AC conductor.	**3.1.6 Metals**			Performance Test	**Design**
8	They [the DC logic ground and AC conductor] shall be electrically isolated from each other by 500 megohms, minimum, when tested at the input terminals with 500 VDC.	**3.1.6 Metals**			Analysis	**Design**
9	Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards shall be mechanically secured with a minimum of four spacers/metal screws.	**3.1.6 Metals**		It is sufficient to specify that the daughter boards are mechanically secured. Specifying the number of screws is not necessary and creates a useless requirement.	Inspection	**Design**
10	Connectors shall be either Flat Cable or PCB Headers.	**3.1.6 Metals**			Inspection	**Design**
11	Components are allowed to be mounted under the daughter board.	**3.1.9 Daughter Boards**		This requirement provides no value.	**Drop from the standard.**	**Design**
14	The electronic circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.	**3.2.1 Components – General**			Inspection	**Design**
15	No device shall be socket mounted unless specifically called out.	**3.2.2 Components - Electronic**			Inspection	**Design**
16	No component shall be operated above 80% of its maximum rated voltage, current or power ratings.	**3.2.2 Components – Electronic**		~~This is a procurement requirement and has nothing to do with the design of the cabinet~~.	Analysis	**Design**
17	Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.	**3.2.2 Components – Electronic**			Analysis	**Design**
19	The design life of all components, operating for twenty-four hours a day and operating in their circuit application, shall be ten years or longer.	**3.2.2 Components – Electronic**			Analysis	**Design**
20	Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance.	**3.2.2 Components – Electronic**		Poorly worded standard. Easily replaceable means what exactly?	Inspection	**Design**
21	Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.	**3.2.2 Components – Electronic**		How is the possibility for damage by shock or vibration quantified?	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
24	The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150%. Capacitor encasements shall be resistant to cracking, peeling and discoloration.	**3.2.3 Capacitors**			Analysis	**Design**
25	All capacitors shall be insulated and shall be marked with their capacitance values and working voltages.	**3.2.3 Capacitors**			Inspection	**Design**
26	Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.	**3.2.3 Capacitors**			Inspection	**Design**
28	Under 1 Watt potentiometers shall be used only for trimmer type function.	**3.2.4 Potentiometers**			Inspection	**Design**
29	The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.	**3.2.4 Potentiometers**			Analysis	**Design**
31	All resistors shall be insulated and shall be marked with their resistance values.	**3.2.5 Resistors**			Inspection	**Design**
32	Resistance values shall be indicated by the EIA color codes, or stamped value.	**3.2.5 Resistors**			Inspection	**Design**
34	Special ventilation or heat sinking shall be provided for all 2-watt or greater resistors.	**3.2.5 Resistors**			Inspection	**Design**
35	They [all resistors] shall be insulated from the PCB.	**3.2.5 Resistors**			Inspection	**Design**
37	All metal oxide semiconductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.	**3.2.6 Semiconductor Devices**			Inspection	**Design**
38	Device pin "1" locations shall be properly marked on the PCB adjacent to the pin.	**3.2.6 Semiconductor Devices**			Inspection	**Design**
41	Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with thermal conductive compound or material, in addition to being mechanically secured.	**3.2.8 Triacs**			Inspection	**Design**
44	Contacts shall be silver alloy and enclosed in an arc quenching chamber.	**3.2.9 Circuit Breakers**			Inspection	**Design**
45	Overload tripping shall not be influenced by an ambient air temperature range of from -18 degrees C to 50 degrees C.	**3.2.9 Circuit Breakers**		It appears that this requirement “sneaked in” from the re-use of cabinet boilerplate. There are no circuit breakers in the ATC 2070.	Performance Test	**Design**
46	The minimum Interrupting Capacity shall be 5,000 amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity.	**3.2.9 Circuit Breakers**			Performance Test	**Design**
47	For circuit breakers 80 amperes and above, the minimum interrupting capacity shall be 10,000 amperes, RMS.	**3.2.9 Circuit Breakers**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
49	The Load Circuit Breakers used to power Switch Packs shall have auxiliary switches.	**3.2.9 Circuit Breakers**			Inspection	**Design**
51	All Fuses that are resident in a bayonet style fuse holder shall have the fuse size rating labeled on the holder or on the panel adjacent to the holder.	**3.2.10 Fuses**			Inspection	**Design**
54	The switch contact resistance shall be 100 milliohms maximum at 2 milliamperes, 30 VDC.	**3.2.11 Switches**			Analysis	**Design**
63	Screw size [for the terminal blocks] is called out under the associated file, panel or assembly.	**3.2.12 Terminal Blocks**			Inspection	**Design**
64	Provided the connectors mate, screw lug cam driven devices or crimp pin connectors shall be allowable if the interface is part of a harness.	**3.2.13 Screw Lug and Cam Driven Connectors**		Is specifying an exact gauge of wire appropriate? Maybe 22-gauge wire is a minimum size.	Inspection	**Design**
66	Harnesses shall be neat, firm and properly bundled with external protection.	**3.2.14 Wiring, Cabling, and Harnesses**		Words like “neat” are subjective in a standard and are both un-testable and undefined.	Inspection	**Design**
67	They [wiring harnesses] shall be tie-wrapped and routed to minimize crosstalk and electrical interference.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
68	Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
69	Conductors within an encased harness have no color requirements.	**3.2.14 Wiring, Cabling, and Harnesses**		Does this specification add any value?	**Drop from the standard.**	**Design**
70	Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.	**3.2.14 Wiring, Cabling, and Harnesses**		What does “where possible” mean and how is it quantified?	**Drop from the standard.**	**Design**
72	Wiring shall be routed to prevent conductors from being in contact with metal edges.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
73	Wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
74	All conductors, except those that can be readily traced, shall be labeled.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
75	Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
77	The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
80	All indicators and character displays shall be readily visible at a radius of up to 4 feet within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 footcandles) of white light with the light source at 45 degrees (+/-2 degrees) to the front panel.	**3.2.15 Indicators and Character Displays**			Performance Test	**Design**
82	All indicators shall be self-luminous.	**3.2.15 Indicators and Character Displays**			Inspection	**Design**
85	Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance shall be provided.	**3.2.15 Indicators and Character Displays**		How much clearance? Is the amount of clearance important?	Inspection	**Design**
86	Liquid Crystal Displays (LCD) shall be readable at temperatures of -20 degrees C to +70 degrees C.	**3.2.15 Indicators and Character Displays**			Performance Test	**Design**
87	All controller unit functions are required to operate at temperatures of –37 degrees C to +74 degrees C.	**3.2.15 Indicators and Character Displays**			Performance Test	**Design**
89	The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).	**3.2.16 Connectors**			Inspection	**Design**
91	The terminal block shall be a barrier type with 6-32, 0.25 inches or longer, nickel plated brass binder head screws.	**3.2.16 Connectors**			Inspection	**Design**
92	Each terminal shall be permanently identified as to its function.	**3.2.16 Connectors**			Inspection	**Design**
93	Pin and socket contacts for connectors shall be beryllium copper construction subplated with 1.27 microns nickel and plated with 0.76 microns gold.	**3.2.16 Connectors**			Inspection	**Design**
94	Pin diameter shall be 0.0618 inches.	**3.2.16 Connectors**			Inspection	**Design**
99	The PCB 22/44 Connector shall have 22 independent contacts per side; dual sided with 0.156 inch contact centers.	**3.2.16 Connectors**			Inspection	**Design**
101	All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.	**3.2.16 Connectors**		Manufacturing specification. (There is no way to ascertain if this requirement was met after-the-fact.)	Inspection	**Design**
102	Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 0.00015 inches of gold over 0.00005 inches of nickel; and shall have a current rating of 1 Ampere minimum and an insulation resistance of 5 Megohms minimum.	**3.2.16 Connectors**			Inspection Performance Test	**Design**
103	Each PCB header post shall be 0.025 inches square by 0.3425 inches high from the plane of the PCB to the end of the pin; shall be mounted on 0.10 inch centers; and shall be tempered hard brass plated with 0.00015 inches of gold over 0.00005 inches of nickel.	**3.2.16 Connectors**			Inspection	**Design**
104	Each PCB header socket block shall be nylon or diallyl phthalate.	**3.2.16 Connectors**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
105	Each PCB header socket contact shall be removable, but crimp-connected to its conductor.	**3.2.16 Connectors**			Inspection	**Design**
107	Each PCB header socket contact shall be brass or phosphor bronze plated with 0.0015 inches of gold over 0.00005 inches of nickel.	**3.2.16 Connectors**			Inspection	**Design**
109	All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs.	**3.3.1 Assemblies**		Words like, “easily replaceable” are subjective and untestable.	Inspection	**Design**
110	Assemblies shall be provided with two guides for each plug-in PCB or associated device (except relays).	**3.3.1 Assemblies**			Inspection	**Design**
111	The guides shall extend to within 0.75 inches from the face of either the socket or connector and front edge of the assembly.	**3.3.1 Assemblies**			Inspection	**Design**
112	If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.	**3.3.1 Assemblies**			Inspection	**Design**
113	All screw type fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.	**3.3.2 Locking Devices**			Inspection	**Design**
114	No components, traces, brackets or obstructions shall be within 0.125 inches of the board edge (guide edges).	**3.3.3 PCB Design and Connectors**			Inspection	**Design**
115	The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs.	**3.3.3 PCB Design and Connectors**			Inspection	**Design**
116	The manufacturer's model number and circuit issue or revision number shall appear on the rear panel of all equipment supplied (where such panel exists).	**3.3.4 Model and Serial Numbers**			Inspection	**Design**
117	In addition to any assignment of model numbers by the manufacturer, the TYPE number shall be displayed on the front panel in bold type, at least 0.25 inches high.	**3.3.4 Model and Serial Numbers**			Inspection	**Design**
121	Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.	**3.3.5 Workmanship**			**Drop from the standard.**	**Design**
122	The following tolerances shall apply, except as specifically shown on the plans or in these specifications: *TYPE DIMENSIONAL TOLERANCE* Sheet Metal +/-0.0525 inch PCB +0 inch, - 0.010 inch Edge Guides +/-0.015 inch *Note: These dimensional tolerances do not apply to material gauge or thickness.	**3.3.6 Tolerances**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
123	The equipment shall be engineered for simplicity, ease of operation and maintenance.	**3.4.1 Human Engineering**			**Drop from the standard.**	**Design**
125	PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors.	**3.4.1 Human Engineering**			Inspection	**Design**
126	PCBs shall require a force no less than 5 pounds-force or greater than 50 pounds-force for insertion or removal.	**3.4.1 Human Engineering**			Analysis	**Design**
127	The design shall be inherently temperature compensated to prevent abnormal operation.	**3.4.2 Design Engineering**		What does "inherently temperature compensated" mean? I think their try to refer to using natural convection for cooling rather than using a fan since a fan is not fail-safe. The standard should say that more clearly.	Analysis	**Design**
128	The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range.	**3.4.2 Design Engineering**			Analysis	**Design**
129	The design shall take into consideration the protection of personnel from all dangerous voltages.	**3.4.2 Design Engineering**		What does "take into consideration" mean and how is it verified?	**Drop from the standard.**	**Design**
131	No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.	**3.4.3 Generated Noise**		What noise level is "sufficient to interfere…" exactly? No pass/fail criteria anyway.	Performance Test	**Design**
133	PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.	**3.5.1 Design, Fabrication, and Mounting**			Performance Test	**Design**
136	Inter-component wiring shall be by laminated copper clad track having a minimum weight of 0.2 ounces per square foot with adequate cross section for current to be carried.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Design**
137	All copper tracks shall be plated or soldered to provide complete coverage of all exposed copper tracks.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Design**
138	Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.	**3.5.1 Design, Fabrication, and Mounting**		"As short as possible" is a nebulous requirement.	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
144	Semiconductor devices that dissipate more than 250 milliwatts or cause a temperature rise of 10 degrees C or more shall be mounted with spacers, transipads or heat sinks to prevent contact with the PCB.	**3.5.1 Design, Fabrication, and Mounting**			Analysis	**Design**
145	When completed, all residual flux shall be removed from the PCB.	**3.5.1 Design, Fabrication, and Mounting**		This is okay, but should be worded differently. This reads like a manufacturing step. Maybe it should just say that the PCB shall be free of all residual flux.	Inspection	**Design**
146	The resistance between any two isolated, independent conductor paths shall be at least 100 Megohms when a 500 VDC potential is applied.	**3.5.1 Design, Fabrication, and Mounting**		Wouldn't the 100 Mohms would be 100 Mohms regardless of the VDC applied. What is the point of specifying 500 VDC? Should the VDC specification be removed? It makes testing a lot more difficult and possibly destructive.	Performance Test	**Design**
148	Where less than 0.25 inches lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.0625 inches (+/-0.0005 inches) Thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Design**
149	Each PCB connector edge shall be chamfered at 30 degrees from board side planes.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Design**
150	The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Design**
151	The key slots shall be 0.045 inches (+/- 0.005 inches) for 0.1 inches spacing and 0.055 inches (+/- 0.005 inches) for 0.156 inches spacing.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Design**
152	Hand soldering shall comply with Military Specification MIL-STD-2000.	**3.5.2 Soldering**		Need to dig up this specification.	Inspection	**Design**
156	Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.	**3.5.2 Soldering**		This requirement cannot be verified after-the-fact.	Inspection	**Design**
157	If exposure to the temperature bath is of such a time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.	**3.5.2 Soldering**		This is a manufacturing process requirement rather than a design requirement.	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
158	Definitions for the purpose of this section on PCBs shall be taken from MIL-P-55110D Section 3.3 and any current addendum.	**3.5.3 Definitions**		Need to dig up this specification.	Inspection	**Design**
50	The auxiliary switches shall "open" when the load breaker has tripped and the system will transfer the power from the Main Contactor to the Flash or Blank condition.	**3.2.9 Circuit Breakers**	n/a	This is a cabinet specification and should not be in this standard.	Performance Test	**Performance**
52	Fuses shall be easily accessible and removable without use of tools.	**3.2.10 Fuses**	P	Words such as, "easily accessible" are not of value in a standard, since they can neither be defined nor measured.	Inspection	**Performance**
65	For field termination, screw lug and cam driven assemblies are interchangeable for field wiring termination, provided they both accommodate 22-gauge wire on the inputs and 22-gauge wire on the outputs.	**3.2.13 Screw Lug and Cam Driven Connectors**	n/a	Can the 22-gauge specification be expressed in terms of performance? Note: It is not clear that this clause is applicable.	Inspection	**Performance**
71	Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.	**3.2.14 Wiring, Cabling, and Harnesses**	P		Inspection	**Performance**
79	Conductor color identification shall be as follows: AC- circuits - white Equip. Ground – solid green or continuous green color with 1 or more yellow stripes. DC logic ground – continuous white with a red stripe. AC+ circuits – continuous black or black with colored stripe. DC logic ungrounded or signal – any color not specified.	**3.2.14 Wiring, Cabling, and Harnesses**	P/F	The standard is apparently using a US convention, but the AC power cord on the Eagle 2070L that we examined did not exhibit US standard and seems to meet European color coding schemes.	Inspection	**Performance**
81	All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted.	**3.2.15 Indicators and Character Displays**	F	The Eagle 2070 we examined did not meet this requirement. It is likely that this specification is too strenuous anyway. It might be that this requirement should be split for indicators and displays.	Performance Test	**Performance**
84	Each LED indicator shall be white or clear when off.	**3.2.15 Indicators and Character Displays**	P		Inspection	**Performance**
88	Connectors shall be keyed to prevent improper insertion of the wrong connector where equipment damage or operator injury may result.	**3.2.16 Connectors**	P	On the Eagle 2070, nothing is keyed, but you can't break anything or get hurt, so it meets the standard.	Inspection	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
118	A permanent label shall be affixed to the inside near and center floor of the Type 2070 unit chassis when viewed from the front.	**3.3.4 Model and Serial Numbers**	P	Might this requirement be better communicated by including a font size?	Inspection	**Performance**
119	The label shall display the unit's serial number.	**3.3.4 Model and Serial Numbers**			Inspection	**Performance**
120	The number shall be permanent and easy to read.	**3.3.4 Model and Serial Numbers**	P	Words like "easy to read" are undefined and as such, un-testable.	Inspection	**Performance**
124	Knobs shall be a minimum of 0.5 inches in diameter and a minimum separation of 0.5 inches edge to edge.	**3.4.1 Human Engineering**	P		Inspection	**Performance**
130	No item, component or subassembly shall emit an audible noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted.	**3.4.3 Generated Noise**	P	Tested with a sound meter obtained from Siemens.	Performance Test	**Performance**
2	Sheet shall be 63 gauge American Standard (0.060-inch) minimum thick Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.	**3.1.6 Metals**		This appears to be a manufacturing or manufacturer specification. What specific, measurable, performance standard is met by using a particular thickness or type of material?	Inspection	**Procurement**
3	Sheet shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.	**3.1.6 Metals**			Inspection?	**Procurement**
4	Sheet, Rod, Bar and Extruded shall be Type 1018/1020.	**3.1.6 Metals**		What performance requirement is addressed by this standard?	Inspection?	**Procurement**
5	All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class l or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.	**3.1.6 Metals**		Need to dig up this specification.	Inspection	**Procurement**
6	All bolts, nuts, washers, screws, hinges and hinge pins shall be stainless steel unless otherwise specified.	**3.1.6 Metals**			Inspection	**Procurement**
12	All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:	**3.2.1 Components – General**		Manufacturing and/or supply chain specification. What performance requirement is addressed by this standard?	Inspection	**Procurement**
13	When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.	**3.2.1 Components – General**		This is a procurement requirement and has nothing to do with a design standard.	**Drop from the standard.**	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
18	No component shall be provided where the manufactured date is three years older than the contract award date.	**3.2.2 Components – Electronic**			Analysis	**Procurement**
22	The Manufacturer shall submit detailed engineering technical data on all components at the request of the AGENCY.	**3.2.2 Components – Electronic**		This specifies a documentation task for the manufacturer that has no affect on the cabinet design.	Analysis	**Procurement**
23	The Manufacturer shall certify that the component application meets the requirements of this standard.	**3.2.2 Components – Electronic**		Procurement requirement.	Analysis	**Procurement**
27	Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements.	**3.2.4 Potentiometers**		Need to dig up this specification.	Analysis	**Procurement**
30	Fixed carbon film, deposited carbon, or composition insulated resistors shall conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684.	**3.2.5 Resistors**		Need to dig up this specification.	Inspection	**Procurement**
33	The value of the resistors shall not vary by more than 5% between -37 degrees C and 74 degrees C.	**3.2.5 Resistors**			Analysis	**Procurement**
36	All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable.	**3.2.6 Semiconductor Devices**		Need to dig up this specification.	Inspection	**Procurement**
39	All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination.	**3.2.7 Transformers and Inductors**			Inspection	**Procurement**
40	All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.	**3.2.7 Transformers and Inductors**		Need to dig up this specification.	Inspection	**Procurement**
42	Circuit breakers shall be listed by UL or ETL.	**3.2.9 Circuit Breakers**			Inspection	**Procurement**
43	The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the ampere rating shall be visible from the front of the breaker.	**3.2.9 Circuit Breakers**			Inspection	**Procurement**
48	Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carlingswitch Time Delay Curve #24 or equal).	**3.2.9 Circuit Breakers**		Need to dig up this specification.	Analysis	**Procurement**
53	Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 milliamperes, 30 VDC.	**3.2.11 Switches**			Inspection	**Procurement**
55	The contacts shall be gold over brass.	**3.2.11 Switches**			Inspection	**Procurement**
56	The switch contacts shall be rated for a minimum of 1 ampere resistive load at 120 VAC and shall be silver over brass (or equal).	**3.2.11 Switches**			Inspection	**Procurement**
57	The switch shall be rated for a minimum of 40,000 operations.	**3.2.11 Switches**			Inspection	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
58	The switch contacts shall be rated for a minimum of 5 amperes resistive load at 120 VAC or 28 VDC and shall be silver over brass (or equal).	**3.2.11 Switches**			Inspection	**Procurement**
59	The switch shall be rated for a minimum of 40,000 operations.	**3.2.11 Switches**			Inspection	**Procurement**
60	Ratings shall be the same as CONTROL, except the contact rating shall be a minimum of 10 amperes at 125 VAC.	**3.2.11 Switches**			Inspection	**Procurement**
61	The terminal blocks shall be barrier type, rated at 20 amperes and 600 VAC RMS minimum.	**3.2.12 Terminal Blocks**			Inspection	**Procurement**
62	The terminal screws shall be 0.3125 inches minimum length nickel plated brass binder head type with screw inserts of the same material.	**3.2.12 Terminal Blocks**			Inspection	**Procurement**
76	All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper.	**3.2.14 Wiring, Cabling, and Harnesses**		Need to dig up these specifications.	Inspection	**Procurement**
78	Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.	**3.2.14 Wiring, Cabling, and Harnesses**		Why is insulation less than 15 mils allowed?	Inspection	**Procurement**
83	All indicators shall have a rated life of 100,000 hours minimum.	**3.2.15 Indicators and Character Displays**			Inspection	**Procurement**
90	Type T connector shall be a single row, 10 position, feed through terminal block.	**3.2.16 Connectors**			Inspection	**Procurement**
95	All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.	**3.2.16 Connectors**		Are they actually specifying a particular tool to be used for assembly? This is an assembly procedure not a design requirement. Why is a specific tool specified?	Inspection	**Procurement**
96	Edge connectors shall have bifurcated gold-plated contacts.	**3.2.16 Connectors**			Inspection	**Procurement**
97	The PCB receptacle connector shall meet or exceed the following: Operating Voltage: 600 VAC (RMS) Current Rating: 5.0 Amperes Insulation Material: Diallyl Phthalate or Thermoplastic Insulation Resistance: 5,000 Megohms Contact Material: Copper alloy plated with 0.00005 inches of nickel and 0.000015 inches of gold Contact Resistance: 0.006 Ohm maximum	**3.2.16 Connectors**			Performance Test	**Procurement**
98	The two-piece PCB connector shall meet or exceed the DIN 41612.	**3.2.16 Connectors**		Need to dig up this specification.	Inspection	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
100	Each wire terminal shall be solderless with PVC insulation and a heavy duty short - locking spade type connector.	**3.2.16 Connectors**		~~The type of crimping tool is an assembly procedure, not a design requirement~~. The crimping tool is specified due to the likelihood that improper crimps will result in poor connections. It could possibly be specified in a more direct manner.	Inspection	**Procurement**
106	The Manufacturer shall list the part number of the extraction tool recommended by its manufacturer.	**3.2.16 Connectors**			Inspection	**Procurement**
108	The surge suppression device shall comply with ANSI/IEEE C62.41 (100 Kilohertz Ring Wave, the 1.2/50 microseconds – 8/20 Combination Wave and the EFT Burst) at voltages and currents specified at "Location Category B2" and at "Test Severity" level III (i.e. up to 4.0 Kilovolts, open-circuit).	**3.2.17 Surge Protection Device**		Need to dig up this specification.	Inspection	**Procurement**
132	All contacts on PCBs shall be plated with a minimum thickness of 0.00003 inches gold over a minimum thickness of 0.000075 inches nickel.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Procurement**
134	Fabrication of PCBs shall be in compliance with Military Specification MIL-P-13949, except as follows:	**3.5.1 Design, Fabrication, and Mounting**		Need to dig up this specification.	Inspection	**Procurement**
135	NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0625 inches minimum thickness shall be used.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Procurement**
139	All PCBs shall conform to Section 3.3 of Military Specification MIL-P-13949G. Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better.	**3.5.1 Design, Fabrication, and Mounting**		Need to dig up this specification.	Inspection	**Procurement**
140	The class of permissible bow or twist shall be Class C (Table V) or better.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Procurement**
141	The class of permissible warp or twist shall be Class A (Table II) or better.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
142	Sections 4.2 through 6.6 of Military Specification MIL-P-13949G (inclusive) shall be omitted except as referenced in previous sections of this specification.	**3.5.1 Design, Fabrication, and Mounting**		Need to dig up this specification.	Inspection	**Procurement**
143	The mounting of parts and assemblies on the PCB shall conform to Military Specification MIL-STD-275E, except as follows:	**3.5.1 Design, Fabrication, and Mounting**		Need to dig up this specification. Something missing?	Inspection	**Procurement**
147	All PCBs shall be coated with a moisture resistant coating.	**3.5.1 Design, Fabrication, and Mounting**			Inspection	**Procurement**
153	Automatic flow soldering shall be a constant speed conveyor system with the conveyor speed set at optimum to minimize solder peaks or points.	**3.5.2 Soldering**		This is a manufacturing process requirement rather than a design requirement. The soldering process is specified due to the likelihood that poor solder points will result in poor connections. It could possibly be specified in a more direct manner. The quality of the solder points is not directly testable. As such, determining if this standard has been met becomes an exercise in verifying the performance of the board supplier. Is the quality of the vendor an item for a standard?	Inspection	**Procurement**
154	Temperature [during soldering] shall be controlled to within +/- 8 degrees C of the optimum temperature.	**3.5.2 Soldering**		This requirement cannot be verified after-the-fact.	Inspection	**Procurement**
155	The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process.	**3.5.2 Soldering**			Inspection	**Procurement**
159	Jumpers are not allowed unless called out in the specifications or approved by the AGENCY.	**3.5.4 Jumpers**			**Drop from the standard.**	**Procurement**

B.2 ATC Type 2070 Controller Requirements

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th>Pass
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>162</td><td>It is noted that the Power Failure Power Restoration operations of this unit are specific to the requirements of the user. All associated modules shall comply to said operations.</td><td>4.1.4 Power Fail and Power Restoration Operation</td><td></td><td>Aside from being poorly-worded, the value of this specification is suspect. Was it found that most developers of type 2070 controllers were supplying units that had power failure restoration operation that was different than the user required? If not, why specify this?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>163</td><td>2070 UNIT module / assembly power limitations shall be as follows:
<table>
<tr><th>Types</th><th>+5VDC</th><th>+12VDC ISO</th><th>+12VDC ser</th><th>-12 VDC ser</th></tr>
<tr><td>MCB</td><td>750 milliamperes</td><td>-----</td><td>-----</td><td>-----</td></tr>
<tr><td>TRANS BD</td><td>750 milliamperes</td><td>-----</td><td>-----</td><td>-----</td></tr>
<tr><td>2070-2A FI/O</td><td>250 milliamperes</td><td>750 milliamperes</td><td>-----</td><td>-----</td></tr>
<tr><td>2070-2B FI/O</td><td>250 milliamperes</td><td>500 milliamperes</td><td>-----</td><td>-----</td></tr>
<tr><td>2070-3A&B FPA</td><td>500 milliamperes</td><td>-----</td><td>50 milliamperes</td><td>50 milliamperes</td></tr>
<tr><td>2070-3C FPA</td><td>100 milliamperes</td><td>-----</td><td>50 milliamperes</td><td>50 milliamperes</td></tr>
<tr><td>2070-5 VME Cage</td><td>5.0 amperes</td><td>-----</td><td>200 milliamperes</td><td>200 milliamperes</td></tr>
<tr><td>2070-6 All Comm</td><td>500 milliamperes</td><td>-----</td><td>100 milliamperes</td><td>100 milliamperes</td></tr>
<tr><td>2070-7 All Comm</td><td>250 milliamperes</td><td>-----</td><td>50 milliamperes</td><td>50 milliamperes</td></tr>
</table></td><td>4.1.5 Power Limitations</td><td></td><td>Given the rigor of these requirements, it would be expected that each device noted could be measured for adherence to the specification. However, how is one to test a limitation in a non-destructive manner?</td><td>Inspection</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
164	All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 megabits per second. Isolation circuitry shall be by opto- or capacitive-coupled isolation technologies.	**4.1.6 EIA-485 Communications Circuitry**			Inspection Performance Test	**Design**
165	Through-hole EIA-485 Line Drivers/Receivers, when used, shall be socket mounted.	**4.1.7 EIA-485 Line Drivers/Receiver**			Inspection	**Design**
166	Surface mounted drivers/receiver shall be acceptable.	**4.1.7 EIA-485 Line Drivers/Receiver**		If surface mounted drivers are acceptable, why are socket mounted drivers specified? Worthless requirement, as currently worded.	Inspection	**Design**
168	A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input.	**4.1.7 EIA-485 Line Drivers/Receiver**			Inspection	**Design**
173	Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.	**4.1.8 Sockets**		Manufacturing specification.	Inspection	**Design**
174	SP5and SP3 SDLC frame address assignments (Command/Response) are as follows: SP5 SP3 CPU 2070-1 = "19" "19" FI/O 2070-2A & 8 = "20" "Not Applicable" CPU Broadcast to all = "255" "255" All other addresses are reserved by this standard. The SDLC response frame address shall be the same address as the Command frame it receives.	**4.1.9 SDLC**			Performance Test	**Design**
167	EIA-485 Line Drivers/Receivers shall not draw more than 35 milliamperes in active state and 20 milliamperes in inactive state per channel.	**4.1.7 EIA-485 Line Drivers/Receiver**			Analysis	**Design**
169	The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-).	**4.1.7 EIA-485 Line Drivers/Receiver**			Performance Test	**Design**
170	A control signal is inactive when its positive terminal voltage is higher than its negative terminal.	**4.1.7 EIA-485 Line Drivers/Receiver**	P		Performance Test	**Performance**
171	Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-).	**4.1.7 EIA-485 Line Drivers/Receiver**	P		Performance Test	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
172	A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).	**4.1.7 EIA-485 Line Drivers/Receiver**	P		Performance Test	**Performance**
160	The composition weight shall not exceed 25 pounds.	**4.1.2 General – Unit Configurations**		This requirement could refer to road-side constraints, but it still seems odd.	Inspection	**Procurement**
161	The CHASSIS Top and Bottom, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Power Supply Enclosure, and Front Panel shall be made of 63 gauge minimum aluminum sheet. The CHASSIS Side panels shall be 80 gauge minimum sheet.	**4.1.3 Metalwork**		This appears to be a manufacturing or manufacturer specification. What specific, measurable, performance standard is met by using a particular thickness or type of material?	Inspection	**Procurement**

B.3 ATC Type 2070 CPU Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
177	The module shall meet all the requirements listed under this section and Chapter Details 4.7 except for the following:	**4.2.1 Type 2070 – 1B Configuration**		From the wording of the sections following, this is very confusing. The words, "except as specified below" are much clearer.	Inspection	**Design**
178	The VME software and hardware bus requirements shall not apply nor do the MCB and Board Interface Harness physical requirements.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
179	A Dual SCC Device (asynch/synch) and associated circuitry shall be furnished to provide two additional system serial ports.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
180	The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
181	The Dual SCC2 shall be assigned as System Serial Port SP8.	**4.2.1 Type 2070 – 1B Configuration**			Analysis	**Design**
182	The SP8 and associated circuitry shall interface with the MC68360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
183	The SP8 shall meet all SP2 Port requirements including EIA 485 Drivers / receivers and synchronous data rate of 614.4 kilobits per second.	**4.2.1 Type 2070 – 1B Configuration**			Inspection Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
184	The 68360 SCC1 shall be reassigned to ETHERNET (ENET) Network meeting ETHERNET 10 MBPS IEEE 802.3 (TP) 10 BASE T Standard Requirements, both hardware and software.	**4.2.1 Type 2070 – 1B Configuration**			Analysis	**Design**
185	The four network lines shall be used to route ETHERNET across the MOTHERBOARD to the "A" Connectors.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
186	DC Grounding plane around the network connectors and lines shall be provided.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
187	Network Lines shall be assigned as: Network 1 = ENET TX+, Network 2 = ENET TX-, Network 3= ENET RX+, and Network 4 = ENET RX-.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
188	The conditioned ETHERNET shall be brought out on RJ 45 C14S Connector mounted on the CPU-1B Front Panel.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Design**
191	The MCB shall be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master & Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester, a system clock driver, and BTO (64).	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
192	The CONTROLLER Device shall be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
193	The Fast IRQ Service System is reserved for AGENCY use only.	**4.2.3 Main Controller Board (MCB)**			**Cannot be verified.**	**Design**
194	The Interrupts shall be configured as follows: Level 7 –VMEbus IRQ7 Level 6 –VMEbus IRQ6 ACFAIL Level 5 – VMEbus IRQ5 CPU Module Counters / Time vectored), Serial Interface Interrupts Level 4 –VMEbus IRQ4 Level 3 –VMEbus IRQ3 Level 2 –VMEbus IRQ2 Level 1 –VMEbus IRQ1	**4.2.3 Main Controller Board (MCB)**			Analysis	**Design**
195	The Memory Address Organization shall be configured as follows: 8000 0000 – 80FF FFFF STANDARD 9000 0000 – 9000 FFFF SHORT	**4.2.3 Main Controller Board (MCB)**			Analysis	**Design**
196	16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary.	**4.2.3 Main Controller Board (MCB)**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
197	The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's File Manager, or approved equivalent.	**4.2.3 Main Controller Board (MCB)**			Analysis	**Design**
198	The address of each memory block shall be specified by the manufacturer and provided with the documentation.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
199	When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state; and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
200	[After the switch to Standby Power] An on-board circuit shall sense the +5 VDC Standby Power and shift to an On-board CPU Power Source.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
201	When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.	**4.2.3 Main Controller Board (MCB)**		What is meant by "the appropriate MCB Circuitry"? No one in the room knew what "appropriate" referred to.	Performance Test	**Design**
202	A minimum of 8 megabytes of DRAM Memory, organized in 32-bit words, shall be provided.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
203	A minimum of 1 megabyte of SRAM is required, of which 512 KiloBytes minimum shall be available for Agency use as a RAM drive (R0).	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
204	The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 nanoseconds and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.	**4.2.3 Main Controller Board (MCB)**			Inspection Performance Test	**Design**
205	A minimum of 8 megabytes of FLASH Memory, organized in 16- or 32-bit words, shall be provided.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
206	The MCB shall be equipped with all necessary circuitry for writing to the FLASH Memory under program control.	**4.2.3 Main Controller Board (MCB)**		Why would the MCB not be equipped to accomplish such a standard function?	**Drop from the standard.**	**Design**
207	No more than 1 megabyte of FLASH Memory shall be used for Boot Image (List) and a minimum of 7 megabytes shall be available for AGENCY use.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
208	Flash Memory shall have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
209	A software settable hardware Time-of-Day (TOD) clock shall be provided.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
210	It [the software settable clock] shall, under on-board standby power, maintain an accuracy of +/-1 minute per 30 days at 25 degrees C (77 degrees F).	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
211	The clock shall be aligned to a minimum fractional second resolution of 10 milliseconds and shall track seconds, minutes, hours, day of month, month, and year.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
212	A software-driven CPU RESET signal (Active LOW) shall be provided to reset other controller systems.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
213	The signal output shall be driver capable of sinking 30 milliamperes at 30 VDC.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
214	Execution of the program module "CPURESET" in the boot image shall assert the CPU RESET signal once.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
215	An open-collector output, capable of sinking 30 milliamperes at 30 VDC, shall be provided to drive the Front Panel Assembly CPU Activity LED INDICATOR.	**4.2.3 Main Controller Board (MCB)**			Inspection	**Design**
216	The OS-9 Operating System TICK Timer shall be derived from each transition of LINESYNC with a tick rate of 120 ticks per second.	**4.2.3 Main Controller Board (MCB)**			Analysis Performance Test	**Design**
217	The SRAM and TOD Clock Circuitry, under Standby mode, shall draw no more than 8 microamperes at 2.5 VDC and 35 degrees C.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
218	An On-board Capacitor supply shall hold up SRAM and TOD or a minimum of 7 days.	**4.2.3 Main Controller Board (MCB)**			Performance Test	**Design**
219	The Transition Board shall provide a 1 KiloOhm pull-up resistor for the A2 & A3 installed lines.	**4.2.4 Transition Board**			Inspection	**Design**
220	If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).	**4.2.4 Transition Board**			Performance Test	**Design**
221	A SHIELDED INTERFACE HARNESS shall be provided. It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors.	**4.2.5 Shielded Interface Harness**			Inspection	**Design**
222	A minimum of 25 mm of slack shall be provided.	**4.2.5 Shielded Interface Harness**			Inspection	**Design**
223	No power shall be routed through the harness.	**4.2.5 Shielded Interface Harness**			Inspection	**Design**
224	The harness shall be 100% covered by an aluminum mylar foil and an extruded black 0.8 mm PVC jacket or equal.	**4.2.5 Shielded Interface Harness**			Inspection	**Design**
226	Power shall not be applied to the receptacle if the key is not present.	**4.2.6 Datakey**			Performance Test	**Design**
228	The Datakey shall be temperature rated for –40 to +80 degrees C operation.	**4.2.6 Datakey**			Inspection	**Design**
229	The Datakey shall be black in color.	**4.2.6 Datakey**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
230	The Datakey shall be initialized to the format and default values defined below.	**4.2.6 Datakey**			Inspection	**Design**
233	The data format in the CPU Datakey header for the Latitude and Longitude fields shall comply with IEEE/ANSI 754-1985 STD.	**4.2.6 Datakey**			Inspection	**Design**
234	All the other fields shall follow a Big Endian Format as implemented by Motorola CPUs.	**4.2.6 Datakey**			Inspection	**Design**
238	Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis Inspection	**Design**
239	Device drivers which require extensions to the standard OS-9 libraries shall use the _os_getstat() and _os_setstat() functions.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis Inspection	**Design**
240	When PB2070.param2.pointer is used, PB2070.param1 should be loaded with the size of what PB2070.param2.pointer is referencing.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis Inspection	**Design**
241	When calling _os_getstat() or _os_setstat(), all reserved or unused parameters and fields in PB2070 should be loaded with 0 (zero).	**4.2.7 CPU Module Software – Drivers and Descriptors**		What purpose does the sample code in the standard serve?	Analysis	**Design**
244	Access to the MC68360 internal timers shall be provided through the following device descriptors: Descriptor names for each timer: timer1 = access to MC68360's internal timer #1 timer2 = access to MC68360's internal timer #2 timer3 = access to MC68360's internal timer #3 timer4 = access to MC68360's internal timer #4 timer12 = access to MC68360's internal timer #1 & #2 (cascaded) timer34 = access to MC68360's internal timer #3 & #4 (cascaded)	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
246	Timer Standard OS-9 Function Calls: error_code _os_open (char *timer_desc_name, path_id *path); error_code _os_read (path_id path, void *timer_value, u_int32 *size); **Note**: Prior to calling _os_read(), size must be loaded with the value 4 and timer value must be pointed to a u_int32. _os_read() shall read the current timer value and load it into timer_value as µS x 100. error_code _os_close (path_id path).	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
247	Timer Extension to Standard OS-9 Function Calls: error_code _os_setstat(path_id path, SS_2070, PB2070 *pb)	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
248	The timer drivers shall support the following modes using the SS_2070 _os_setstat() option code and a custom parameter block structure:	**4.2.7 CPU Module Software – Drivers and Descriptors**				**Design**
249	a) Send signal after specified time interval. Sets timer to zero and schedules individual one-shot signal. Pb→code = SS2070_Timer_Sig (0x1000); /* request for one-shot signal */ pb.param1 = signal; /* signal code to send (0 = do not send a signal and cancel any pending signals) */" pb→param2.param = period; /* timer period in microseconds x 100 */	**4.2.7 CPU Module Software – Drivers and Descriptors**		This appears to be a code sample. Why is this in a standard?	Analysis	**Design**
250	b) Send recurring periodic signal. Sets timer to zero and schedules repeating periodic signal. Pb→code = SS2070_Timer_Cyc (0x1001); /* request for periodic signal */ pb.param1 = signal; /* signal code to send (0 = do not send a signal and cancel any pending signals) */" pb→param2.param = period; /* timer period in microseconds x 100 */	**4.2.7 CPU Module Software – Drivers and Descriptors**		This appears to be a code sample. Why is this in a standard?	Analysis	**Design**
251	c) Start timer. Start the timer if stopped. Timer will free run in a periodic mode, starting at the current timer value as its initial value and timer's maximum allowable time as its timer period (6.5535 seconds for timers 1-4 and 429496.7295 seconds for timers 12 and 34). Timer will not send a signal and any pending signals will be cancelled. Timer mode will be SS2070_Timer_Start. Pb.code = SS2070_Timer_Start (0x1002); /* start timer if stopped */"	**4.2.7 CPU Module Software – Drivers and Descriptors**		This appears to be a code sample. Why is this in a standard?	Analysis	**Design**
252	d) Stop timer. Leaves current value in timer. Cancels any pending signals. Pb→code = SS2070_Timer_Stop (0x1003); /* stop timer if running */	**4.2.7 CPU Module Software – Drivers and Descriptors**		This appears to be a code sample. Why is this in a standard?	Analysis	**Design**
253	e) Reset timer. Stops timer if running, resets timer value to zero, and cancels any pending signals. Pb→code = SS2070_Timer_Reset (0x1004); /* reset timer (stop and zero) */	**4.2.7 CPU Module Software – Drivers and Descriptors**		This appears to be a code sample. Why is this in a standard?	Analysis	**Design**
254	Timer Extension to Standard OS-9 Function Calls: error_code _os_getstat(path_id path, SS_2070, PB2070 *pb)	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
255	The timer driver will support the following function using the SS_2070 _os_getstat() option code and custom parameter block structure:	**4.2.7 CPU Module Software – Drivers and Descriptors**				**Design**
256	15. Retrieve current timer configuration. Typedef struct { u_int32 value; u_int32 mode; u_int32 signal; u_int32 period; } Timer_status; pb→code = GS2070_Status (0x1C) /* Request timer status data */ pb→param1 = sizeof(Timer_status) pb→param2.pointer = Timer_status* Status data shall be returned in the structure pointed to by pb→param2.pointer as follows: pb→param2.pointer→value /* current timer value in µS x 100 */ pb→param2.pointer→mode /* SS2070_Timer_Sig if one-shot signal pending, SS2070_Timer_Cyc if periodic signal pending, SS2070_Timer_Start if free running, SS2070_Timer_Stop if not active */ pb→param2.pointer→signal /* signal code pending if SS2070_Timer_Sig or SS2070_Timer_Cyc, 0 otherwise */ pb→param2.pointer→period /* timer period in microseconds x 100 if SS2070_Timer_Sig or SS2070_Timer_Cyc, 0 otherwise */	**4.2.7 CPU Module Software – Drivers and Descriptors**		This appears to be a code sample, as well as some specific coding techniques. Why is this in a standard?	Analysis	**Design**
257	All timer periods are specified in units of hundreds of microseconds, i.e. a timer period of 7 = 700 microseconds.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
258	The minimum allowed timer period shall be 500 microseconds.	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does this have to do with a standard? Why is this specified?	Analysis	**Design**
259	The maximum timer period for timers 1-4 shall be 6.5535 seconds (0xFFFF).	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
260	The maximum timer period for timer12 and timer34 shall be 429496.7295 seconds (0xFFFFFFFF).	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does this have to do with a standard? Why is this specified?	Analysis	**Design**
261	The driver shall return error E$Param from _os_setstat() if the requested timer period is outside the allowable range.	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does this have to do with a standard? Why is this specified?	Performance Test Analysis	**Design**
262	Access and control to the CPU Datakey shall be provided through the following descriptor name: *Descriptor Name* datakey = access to the CPU Datakey	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does this have to do with a standard? Why is this specified?	Inspection	**Design**
264	Access and control to the CPU Datakey shall be provided through the following functions:	**4.2.7 CPU Module Software – Drivers and Descriptors**				**Design**
265	*Function Calls* error_code _os_open (char *datakey_desc_name, path_id *path); error_code _os_close (path_id path); error_code _os_read (path_id path, void *data_buffer, u_int32 *data_size); error_code _os_write (path_id path, void *control, u_int32 *data_size); error_code _os_seek(path_id path,u_int32 position); sets read / write offset error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase); /*erases sector(s) if pointer is on a block boundary, returns E$PARAM error if not on a boundary */" error_code = _os_gs_pos(path_id path,u_int32 *position); /* gets current file pointer position */ error_code = _os_gs_size(path_id path, u_int32 *size); /* gets current datakey size */"	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does this have to do with a standard? Why is this specified?	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
266	*Error Codes Returned by Function Calls* E$NotRdy if datakey is not inserted E$Seek if Offset plus *data_size is beyond end of CPU Datakey. E$EOF if upon read or write, the last byte of CPU Datakey has previously been processed."	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does this have to do with a standard? Why is this specified?	Inspection	**Design**
267	Use of SCF to implement the Datakey driver is not allowed.	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does this have to do with a standard? Why is this specified?	Inspection	**Design**
268	The asynchronous serial communications device drivers shall support the six flow control modes (FCM#) described below: 0) No Flow Control Mode 1) Manual Flow Control Mode 2) Auto-CTS Flow Control Mode 3) Auto-RTS Flow Control Mode 4) Fully Automatic Flow Control Mode 5) Dynamic Flow Control Mode	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does CTS stand for? As with other portions of this section of the standard, this seems rather specific for a standard.	Analysis	**Design**
269	The serial device driver shall be able to set user options via _os_setstat() and return status via _os_getstat().	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**

270	To support legacy application programs, the device driver shall also be
	able to set user options via _os_ss_size() and to return status via _os_gs_size():
	error_code_os_setstat(path_id path, SS_2070, void *pb);
	error_code_os_getstat(path_id path, SS_2070, void *pb);
	error_code_os_ss_size(path_id path, u_int32 size);
	error_code_os_gs_size(path_id path, u_int32 *size)
		4.2.7 CPU Module Software – Drivers and Descriptors			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>271</td><td>The preferred method of accessing serial device drivers is through _os_setstat() and _os_getstat(). The _os_ss_size() and _os_gs_size() interface may not be required by future versions of this specification and is therefore not recommended for new development.</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td>What is the value of stating the “preferred” method?
The use of the term “may not be required” does not, on the surface, seem to fit with the recommendation against further new development.</td><td>Drop from the standard.</td><td>Design</td></tr>
<tr><td>272</td><td>The option subcodes to be passed in pb→code and the data to be contained in pb→param1 are defined as follows. Pb→param2 is unused here and should be set to 0 (zero). For _os_ss_size() and _os_gs_size(), the size argument is the same format as pb→param1.</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td>What does this have to do with a standard? Why is this specified?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>273</td><td>The supported _os_setstat() / _os_ss_size() options shall be as follows:</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td></td><td>Design</td></tr>
<tr><td>274</td><td>a) Subcode passed in pb→code is SS2070_OFC (0x23).
Data passed in pb→param1 is defined as follows:
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31-24</td><td>Auto RTS turn-off extension in number of characters (range: 0-255, 0=default).</td></tr>
<tr><td>23-14</td><td>Reserved for future use.</td></tr>
<tr><td>13</td><td>Inhibit return of error E$Write from _os_write() when transmit buffer full in FCM# 2, 4, 5 (default=0, 0=error, 1=block)</td></tr>
<tr><td>12</td><td>Inhibit variable SCC MRBLR (default =0; 0=NO; 1=inhibit).</td></tr>
<tr><td>11</td><td>Inhibit SCC TODR (default=0; 0=NO; 1=inhibit).</td></tr>
<tr><td>10-8</td><td>Flow Control Mode Number (FCM#) (range:0-5).</td></tr>
<tr><td>7-0</td><td>Subcode SS2070_OFC (0x23).</td></tr>
</table></td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th>Pass
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>275</td><td>a) continued.
Variable MRBLR (68360 SCC)
To reduce the IRQ handler overhead, the 68360 SCC driver shall use variable MRBLR as follows. If SS2070_OFC bit 12 is set to 1, the MRBLR shall be fixed at 16 for all baud rates. Variable MRBLR is not required for SP1 or SP8 on the 2070-1B CPU Module.
Baud Rate — MRBLR Setting
1200 — 1
2400 — 2
4800 — 4
9600 — 8
19200 & Higher — 16</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>276</td><td>a) continued.
TODR (68360 SCC only)
TODR requests processing a new TX buffer immediately. To reduce impact on other serial channel operations, SS2070_OFC bit 11 may be set to 1 to prevent assertion of TODR. TODR is not required for SP1 or SP8 on the 2070-1B CPU Module.</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>277</td><td>b) Subcode passed in pb→code is SS2070_IFC (0x22).
Data passed in pb→param1 is defined as follows:
Bits — Description
31-11 — Reserved for Future Use.
10 — DCD must be asserted to receive data (default=0; 0=NO; 1=YES).
9-8 — Reserved for Future Use.
7-0 — Subcode = SS2070_IFC (0x22).</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>278</td><td>c) Subcode passed in pb→code is SS2070_Ssig (0x1A).
1. If CTS is currently negated and bits 16 – 31 are not all 0:
Setting the SS2070_Ssig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal as soon as CTS is asserted.
Setting the SS2070_Ssig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot signal immediately.</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>279</td><td>c) continued.
2. If CTS is currently asserted and bits 16 – 31 are not all 0:</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>280</td><td>c) continued.
3. If both bits 11 and 12 of the SS2070_Ssig parameter block are set, and bits 16 – 31 are not all 0:
The controller will send a one-shot signal upon the next change of CTS state.
Data passed in pb→param1 is defined as follows:
<table><tr><th>Bits</th><th>Description</th></tr><tr><td>31-16</td><td>A signal number to be sent to calling process when the state of an input changes.</td></tr><tr><td>15-13</td><td>Reserved for Future Use.</td></tr><tr><td>12</td><td>Send signal when CTS is de-asserted.</td></tr><tr><td>11</td><td>Send signal when CTS is asserted.</td></tr><tr><td>10-8</td><td>Reserved for Future Use.</td></tr><tr><td>7-0</td><td>Subcode = SS2070_Ssig (0x1A).</td></tr></table></td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>281</td><td>The supported _os_getstat()_ / _os_gs_size() options shall be as follows:</td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td></td><td>Design</td></tr>
<tr><td>282</td><td>a) Subcode passed in pb→code is GS2070_Status (0x1C).
Data returned in pb→param1 is defined as follows:
<table><tr><th>Bits</th><th>Description</th></tr><tr><td>31-16</td><td>Current unfilled transmit buffer character count of the serial device driver.</td></tr><tr><td>15-11</td><td>Reserved for Future Use.</td></tr><tr><td>10-8</td><td>Current Flow Control Mode Number (FCM#).</td></tr><tr><td>7</td><td>Reserved for Future Use.</td></tr><tr><td>6</td><td>Overrun error – 0=no error; 1=error has occur since last GS2070_Status call.</td></tr><tr><td>5</td><td>Frame error – 0=no error; 1=error has occur since last GS2070_Status call.</td></tr><tr><td>4</td><td>Parity error – 0=no error; 1=error has occur since last GS2070_Status call.</td></tr><tr><td>3-2</td><td>Reserved for Future Use.</td></tr><tr><td>1</td><td>DCD state – 0=de-asserted; 1=asserted.</td></tr><tr><td>0</td><td>CTS state – 0=de-asserted; 1=asserted.</td></tr></table></td><td>4.2.7 CPU Module Software – Drivers and Descriptors</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
283	Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
284	The descriptor names shall be as follows: led = access to CPU Activity LED Indicator dstclock = access to Daylight Savings Time Clock correction	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**

285	The standard OS-9 SCFMAN library calls and their functions are as follows:
	error_code _os_open (char *desc_name, path_id *path); //open descriptor for command
	error_code _os_close (path_id path); //close descriptor
	error_code _os_write (path_id path, void *value, u_int32 *data_size); //set value of function
	*value = 1, turn on LED or enable DST correction (default)
	*value = 0, turn off LED or disable DST correction
	set u_int32*data_size to 1
	error_code _os_read (path_id path, void *value, u_int32 *data_size); //get current state
	set u_int32*data_size to 1
		4.2.7 CPU Module Software – Drivers and Descriptors			Analysis	**Design**

286	Leap Year and Daylight Savings Time (DST) Adjustments – The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
289	Setting Hardware Clock from OS-9 System Clock – Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 milliseconds resolution.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
290	Setting Hardware Clock from OS-9 System Clock – The driver shall compensate for any time elapsed during the process of updating the hardware clock.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
291	Setting OS-9 System Clock from Hardware Clock – At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
292	Setting OS-9 System Clock from Hardware Clock – The clocks shall be synchronized to a minimum of 10 milliseconds resolution.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
293	The current sector of FLASH being written shall first be backed up in SRAM.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
294	The backup sector copy shall be invalidated when FLASH write operation is completed.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
295	In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
296	A user write operation shall restore the valid backup sector copy first.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
297	Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
298	"FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
299	The default delay factor is 30 seconds. No more that 150 KB of SRAM shall be dedicated to this purpose.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
300	Power loss or other interruption while writing to the FLASH drive may cause FLASH drive file and/or disk corruption. It is therefore strongly recommended that the FLASH drive be used to hold controller applications only.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
301	MODEL 2070-1A and 2070-1B CPU modules shall include the following set of standard OS-9 networking modules in the operating system boot image, sufficient to support network configuration, startup, and ftp and telnet servers: spip, ip0, sptcp, tcp0 spudp, udp0, spraw, raw0, spenet, enet, netdb (dns version), ipstart, ifconfig, route, ndbmod, ftpd, ftpdc, telnetd, telnetdc, pkman, pkdrvr, pk, pks, ping, dhcp.	**4.2.7 CPU Module Software – Drivers and Descriptors**		This seems rather specific for a standard. Why is it included?	Inspection	**Design**
309	Execute permission shall be included in the attributes of all files in the /CMDS directory.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
310	/SYS shall contain a default “password” file following the standard OS-9 password file format.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
311	A username “super” with password “user” shall be defined in the password file.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
318	The modules shall be configured with the network default values as defined in Section 4.2.6 (Datakey).	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
320	The netcfg utility shall also provide command line options to allow the user to write and display the network parameters in the Datakey header, write and display the Startup Override byte in the Datakey header, and copy a script or executable file from disk to the Datakey following the header.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
322	The netcfg utility shall reside in /CMDS.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
323	The PPP and SLIP descriptors shall have baud rates and ports set as follows and shall reside in the /CMDS/BOOTOBJS directory: hdlc0 and spsl0 configured to use /sp1 and 38400 bits per second hdlc1 and spsl1 configured to use /sp2 and 115200 bits per second hdlc2 and spsl2 configured to use /sp3 and 115200 bits per second hdlc3 and spsl3 configured to use /sp4 and 38400 bits per second	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
324	A set of example configuration files consistent with the above networking modules shall be provided in the /ETC directory.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
325	The /ETC directory shall contain the following text files: hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf, routes.conf. makefile, nfs.map, nfsd.map	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
326	The provided software shall boot OS-9 from SYSRESET.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
327	The entire program shall be resident in FLASH Memory.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
328	The asynchronous serial port descriptors shall be configured with the following defaults: 8-bit word, 1 stop bit, no parity, no pause, Xon and Xoff both OFF. Port SP4 shall have echo enabled, all other ports shall have no echo.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
329	Default speeds for the asynchronous serial port shall be as defined in Figure 4-7-7.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
330	Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 2.0 seconds.	**4.2.7 CPU Module Software – Drivers and Descriptors**		This requirement seems arbitrary, and unlikely to be verified.	Performance Test	**Design**
331	The boot image init module shall be configured with the default directory name as /f0wp and sysgo as the first executable module.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
332	In the executable module, sysgo, the backspace command applies to the current line, regardless of auto-wrap or autoscroll.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
333	ACFAIL/POWER DOWN transitions shall generate an interrupt.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Performance Test	**Design**
334	The interrupt generated during ACFAIL/POWER DOWN transitions shall update an OS-9 event named “ACFAIL”.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
335	The “ACFAIL” event shall set a value 1 indicating an ACFAIL condition occurred for the DOWN transition and set 0 indicating non-ACFAIL condition for the HIGH transition.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
336	The IRQ7 and auto-vector 31(7) shall not be used to update the “ACFAIL” event.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
337	In addition, the ACFAIL condition shall generate the OS-9 auto-vector 30(6) interrupt service.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
338	Each interrupt service installed shall exit with the "Carry Bit" set allow OS9 to propagate the ACFAIL interrupt.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
339	The Manufacturer shall supply an interrupt handler at priority 255 that acknowledges and clears the interrupt.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
340	Priority 1 shall be reserved for the OS-9 system.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
341	A Long Out is defined as ACFAIL transition to LOW follow[ed] by a SYSRESET going LOW.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
342	The SYSRESET going HIGH shall be followed by an operating system reboot.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis Performance Test	**Design**
343	A Manufacturer may include an error handling routine to save troubleshooting data regarding initialization, power-up test abnormalities and other error conditions.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis Inspection	**Design**
344	If used, the error report shall be stored in the file /r0/ErrorReport and shall not exceed 11 kilobytes in size.	**4.2.7 CPU Module Software – Drivers and Descriptors**		Does this mean that the error report is optional?	Analysis	**Design**
345	When required, a DAT Program shall be provided resident in the Type 2070 ATC Unit as the application program.	**4.2.7 CPU Module Software – Drivers and Descriptors**		What does "when required" mean in the context of a standard? Why would an optional item be specified in a standard?	Analysis	**Design**
346	A Utility Program shall be provided that would allow the user to upgrade (re-flash) the Boot Image as defined in section 4.2.7.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
347	This utility shall provide the capabilities for upgrading the Operating System and drivers when available by the manufacturer.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
348	The Utility Program shall provide the capability for the user to dynamically upgrade the Boot Image via the command prompt.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Analysis	**Design**
349	The Manufacturer shall also provide a copy in CD Memory of all files originally stored in the flash drive /f0 so that they can be reloaded as needed.	**4.2.7 CPU Module Software – Drivers and Descriptors**				**Design**
351	If the agency feels that knowledge of the source code and/or access to the source code is necessary for the purchase of Type 2070 ATC's, then they are referred to forthcoming guidance documents for provisions which should be included in a procurement specification to protect the interests of both the Manufacturer and the Agency.	**4.2.7 CPU Module Software – Drivers and Descriptors**		Why is "agency" not in all caps, as per AGENCY in other places? This is very poorly worded. It is difficult to ascertain what this note refers to or accomplishes.	**Drop from the standard.**	**Design**
352	OS-9 compliant header files shall be provided with all driver modules.	**4.2.7 CPU Module Software – Drivers and Descriptors**			Inspection	**Design**
175	The TYPE 2070-1B CPU shall be a single board module meeting the 2X WIDE board requirements.	**4.2.1 Type 2070 – 1B Configuration**	P	This is a standard VME specification, but is shown on the drawing 4-7-6.	Inspection	**Performance**
189	Four LEDs labeled "TX, RX, TX Collision and TX Status" shall be mounted on the front panel signifying ETHERNET operational conditions.	**4.2.1 Type 2070 – 1B Configuration**	F	The actual modules reflected the drawing, but not the text of this requirement.	Inspection Performance Test	**Performance**
190	The 2070-1B CPU shall not draw more than 1.00 Amperes of +5VDC and 500 milliamperes of ISO+12 VDC.	**4.2.1 Type 2070 – 1B Configuration**		Might the word "module" be better used here?	Performance Test	**Performance**
225	A DATAKEY Receptacle (KC4210, KC4210PCB or equal) shall be provided and mounted on the CPU module front panel (or the Transition Board of Type 1A).	**4.2.6 Datakey**	P		Inspection	**Performance**
227	The Manufacturer shall supply a 2 megabyte Memory Size Datakey (SFK2Mb or equal) with each MODEL 1A TB (Transition Board) or 1B CPU module unless specified otherwise.	**4.2.6 Datakey**	F	HCTX doesn't use this size of key and never receives them from the manufacturer.	Inspection	**Performance**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>231</td><td>When programmed, the memory on the key of header version 1 shall be organized as follows:
<table>
<tr><th>Bytes</th><th>Description</th><th>Default Values</th></tr>
<tr><td>1-2</td><td>16 bit Frame Check Sequence (FCS) calculated as defined in clause 4.6.2 of ISO/IEC 3309. This FCS is calculated across bytes 3-64</td><td></td></tr>
<tr><td>3</td><td>Key Type</td><td>See table below</td></tr>
<tr><td>4</td><td>Header Version</td><td>1</td></tr>
<tr><td>5-8</td><td>Latitude</td><td>0.0</td></tr>
<tr><td>9-12</td><td>Longitude</td><td>0.0</td></tr>
<tr><td>13-14</td><td>Controller ID</td><td>0xFFFF</td></tr>
<tr><td>15-16</td><td>Communication drop number</td><td>0xFFFF</td></tr>
<tr><td>17-20</td><td>IP Address</td><td>10.20.70.51</td></tr>
<tr><td>21-24</td><td>Subnet Mask</td><td>255.255.255.0</td></tr>
<tr><td>25-28</td><td>Default Gateway</td><td>10.20.70.254</td></tr>
<tr><td>29</td><td>Startup Override</td><td>0xFF</td></tr>
<tr><td>30-64</td><td>Reserved for Agency use</td><td>All bytes set to 0xFF</td></tr>
<tr><td>65 to End</td><td>User Data</td><td>All bytes set to 0xFF</td></tr>
</table></td><td>4.2.6 Datakey</td><td>P</td><td>The Key Type did not come back as specified when we read a Datakey installed on a 2070 at the CalTrans' site.</td><td>Inspection</td><td>Performance</td></tr>
<tr><td>232</td><td>When programmed, Byte 3 of the header shall contain the Key Type value as defined in the following table:
<table>
<tr><th>Key Type</th><th>Model No.</th><th>Memory Size</th><th>Sector Size</th></tr>
<tr><td>1</td><td>DK1000</td><td>1 Kilobyte</td><td>1 Byte</td></tr>
<tr><td>2</td><td>LCK16000</td><td>16 Kilobytes</td><td>1 Byte</td></tr>
<tr><td>3</td><td>SFK2Mb</td><td>2 megabytes</td><td>64 Kilobytes</td></tr>
<tr><td>4</td><td>TBD</td><td>4 megabytes</td><td>64 Kilobytes</td></tr>
<tr><td>5</td><td>TBD</td><td>8 megabytes</td><td>64 Kilobytes</td></tr>
</table></td><td>4.2.6 Datakey</td><td>P</td><td></td><td>Inspection</td><td>Performance</td></tr>
<tr><td>235</td><td>The CPU Module shall be supplied with Radisys/Microware OS-9 Version 3.2, or later, with kernel edition #372 or later.</td><td>4.2.7 CPU Module Software – Operating System</td><td>P</td><td>Verified via Mr. Iniguez's PC over the Internet.</td><td>Inspection</td><td>Performance</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
236	The following modules shall be included in the OS: 1. Embedded OS-9 Real Time Kernel 2. Sequential Character File Manager (SCF) 3. Stacked Protocol File Manager (SPF) 4. Pipe File Manager (PIPEMAN) 5. Random Block File Manager (RBF) 6. C Shared Library (CSL)	**4.2.7 CPU Module Software – Operating System**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**
237	Boot Image shall include the following utility modules: Break, Date, Deiniz, Devs, Free, Copy Dir, Tmode, Edt, List, Load, Deldir Dump, Del, Ident, Iniz, Irqs, Events Echo, Format, Dcheck, Login, Link, Kermit Tsmon, Mdir, Mfree, Pd, Makdir, Save Attr, Rename, Procs, Unlink, Sleep, Xmode Shell, Build, Setime, Merge	**4.2.7 CPU Module Software – Operating System**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**
242	Drivers shall be provided to access the FLASH, SRAM, and DRAM memories. The following descriptors shall apply: /f0 FLASH drive non-volatile, writeable /dd FLASH drive OS-9 default device for /f0 /f0wp FLASH Drive as /f0 but, write protection /f0fmt FLASH Drive as /f0 except format enabled /r0 SRAM Drive non-volatile ramdisk /r0fmt SRAM Drive as /r0 but format enabled /r2 DRAM Drive volatile 1 MB ramdisk, not automatically initialized	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Analysis	**Performance**
243	A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Analysis	**Performance**
287	Setting Hardware Clock from OS-9 System Clock – A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
288	Setting Hardware Clock from OS-9 System Clock – The descriptor name shall be "ClockUpdate."	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**
302	The boot image shall include a default inetdb module with a module revision of zero. It shall contain the following entries only: Hosts localhost 127.0.0.1 me Protocols ip 0 IP icmp 1 ICMP igmp 2 IGMP tcp 6 TCP udp 17 UDP Services ndp 13312/tcp ndpd npp 13568/tcp nppd echo 7/tcp echo 7/udp ftp-data 20/tcp ftp-data 20/udp ftp 21/tcp ftp 21/udp telnet 23/tcp telnet 23/udp nameserver 42/tcp nameserver 42/udp tftp 69/tcp tftp 69/udp	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet. The image shown on the controller he Telenet'd into had several other entries than are listed here.	Inspection	**Performance**
303	The boot image shall include a default inetdb2 module with a module revision of zero.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
304	It [the boot image of inetdb2 module] shall contain the following entry only: Interfaces enet0 binding /spqe0/enet (no address, netmask, or broadcast)	**4.2.7 CPU Module Software – Drivers and Descriptors**	F	Verified via Mr. Iniguez's PC over the Internet. There is an apparent conflict between this entry and 4.2.7.2.10.4.	Inspection	**Performance**
305	On the MODEL 2070-1B CPU module, an OS-9 SPF Ethernet hardware driver and descriptor for the 68360 (SCC1) shall be provided in the operating system Boot Image. The descriptor shall be named spqe0.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**
306	A setup utility or script shall be provided to copy the directories and files from the CD to the /f0 flash drive on a controller.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	The utility in this question is "Kermit" and we verified that it is present.	Inspection	**Performance**
307	The following set of files shall be provided on a PC-readable CD to allow a 2070 to be configured with a typical OS-9 development system file configuration: /CMDS, /CMDS/BOOTOBJS, /ETC and /SYS.	**4.2.7 CPU Module Software – Drivers and Descriptors**	F	We could not verify this requirement due to the fact that Mr. Johnson didn't have a CD and had apparently also never used one in this way.	Inspection	**Performance**
308	/CMDS, /CMDS/BOOTOBJS, /ETC and /SYS directories shall be used to organize the files.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**
312	/SYS shall also contain the following four standard OS-9 network configuration shell script files: startspf, startnfs, loadspf and loadnfs.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P		Inspection	**Performance**
313	The utilities tar, make, fixmod, login, tsmon, and mshell shall be included in the /CMDS directory.	**4.2.7 CPU Module Software – Drivers and Descriptors**	F	The utility tsmon could not be found in the /CMDS directory, but was located, instead, in the boot image.	Inspection	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
314	The following OS-9 modules should be included in the /CMDS/BOOTOBJS directory to allow for standard TCP/IP network communications using Ethernet Protocol over Ethernet hardware and/or Serial Line Internet Protocol (SLIP) or Point-to-Point Protocol over serial links: 1. Drivers and Descriptors for PPP: spipcp, ipcp0, splcp, lpc0, sphdlc, hdlc0, hdlc1, hdlc2, hdlc3. 2. Drivers and Descriptors for SLIP: spslip, spsl0, spsl1, spsl2, spsl3. 3. LAN Comm Pak modules: spenet, enet, spip, ip0, sptcp, tcp0, spudp, udp0, spraw, raw0, sproute, route0. 4. Telnet support modules: pkman, pkdvr, pk, pks. 5. Network Trap Handler: netdb_local, netdb_dns. 6. NFS Modules: nfs, nfsnul and nfs_devices.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet.	Inspection	**Performance**
315	The following Network utilities shall be included in the /CMDS directory: arp, dhcp, ftp, ftpd, ftpdc, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, telnet, telnetd, tftpd, tftpdc, telnetdc, hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, pppd, chat, pppauth, nfsd, mountd, and showmount.	**4.2.7 CPU Module Software – Drivers and Descriptors**	F	Utilities tftpd and dtfpdc are both missing, due to a mistake between versions.	Inspection	**Performance**
316	Default inetdb, inetdb2 and rpcdb modules shall be generated by the make utility via the use of a makefile and the network configuration files residing the /ETC directory.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	Verified via Mr. Iniguez's PC over the Internet, where we actually ran the utility.	Inspection	**Performance**
317	The generated inetdb, inetdb2 and rpcdb modules should be located in the /CMDS/BOOTOBJS directory.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P		Inspection	**Performance**
319	A Utility Program named netcfg shall be provided. If the Datakey is present and valid, netcfg shall set the IP Address, Subnet Mask and Default Gateway of the enet0 interface when executed by a user at the command line.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	We ran this utility from the command line, but Mr. Iniguez's controller apparently didn't have a key installed.	Inspection	**Performance**
321	If the Datakey is not present or invalid, netcfg shall display an error and exit without altering any configuration.	**4.2.7 CPU Module Software – Drivers and Descriptors**	P	As per above.	Performance Test	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
350	The following items will be provided to the purchasing AGENCY on a CD disk readable by a PC compatible computer. 1. Specific hardware memory addresses, including FLASH, SRAM, and DRAM starting addresses, shall be specified and provided. Written documentation of addresses shall be in PDF form and will have the file name of "Memory Map.pdf" 2. Copy of all provided written manuals in PDF form. 3. RE-FLASH Utility and the procedures for its use in PDF form. The PDF documentation of the procedures shall have the file name of "Reflash Utility Procedures.pdf."	**4.2.7 CPU Module Software – Drivers and Descriptors**	n/a	Manufacturing specification. For reasons already noted, no CD was available.	Inspection	**Performance**
176	The module shall be furnished normally resident in MOTHERBOARD Slot A5.	**4.2.1 Type 2070 – 1B Configuration**			Inspection	**Procurement**

B.4 ATC Type 2070 Field I/O Module Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
353	The I/O Ports shall provide 64 bits of input using ground-true logic.	**4.3.4 Parallel I/O Ports**			Analysis	**Design**
354	Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 microamperes or the input voltage exceeds 8.5 VDC.	**4.3.4 Parallel I/O Ports**			Performance Test	**Design**
355	Each input shall have an internal pull-up to the Isolated +12 VDC and shall not deliver greater than 20 milliamperes to a short circuit to ground.	**4.3.4 Parallel I/O Ports**			Performance Test	**Design**
356	The I/O Ports shall provide 64 bits of output.	**4.3.4 Parallel I/O Ports**		Is "ground-true" logic important here? Why or why not? What is ground-true logic? It sounds like a brand name.	Analysis	**Design**
357	Inputs shall have the following characteristics: 1. A voltage between 0 and 4 volts shall be considered the **Low** (True/Operate) state. 2. A voltage greater than 8 volts shall be considered the **High** (False) state. 3. The transition from the **Low** state to **High** state (and vice versa) shall occur between 4 and 8 volts.	**4.3.4 Parallel I/O Ports**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
358	Outputs shall have the following characteristics: 1. The **Low** (True/Operate) voltage shall be between 0 and 3 volts. 2. Current sinking capability in the **Low** state shall be at least 100 milliamperes. 3. With an external impedance of 100 kiloOhms or greater, the transition from 4 to 16 volts (and vice versa) shall be accomplished within 0.1 millisecond. 4. The **High** state impedance shall exceed 1 Megohms to 12 volts DC.	**4.3.4 Parallel I/O Ports**			Analysis	**Design**
359	Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal.	**4.3.4 Parallel I/O Ports**			Performance Test	**Design**
360	Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing.	**4.3.4 Parallel I/O Ports**			Performance Test	**Design**
361	The state of all output circuits at the time of Power Up or in Power Down state shall be open (logic 0).	**4.3.4 Parallel I/O Ports**			Performance Test	**Design**
362	It shall be possible to simultaneously assert all outputs within 100 microseconds of each other.	**4.3.4 Parallel I/O Ports**			Performance Test Analysis	**Design**
363	An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.	**4.3.4 Parallel I/O Ports**		What exactly is the definition of "glitch"? Either this word should be changed or the specification should be dropped from the standard. (Depending upon how the user of the standard verified this specification.)	Performance Test	**Design**
364	A maximum capacitive load of 100 picofarads shall be presented to the LINESYNC input signal.	**4.3.5 Other Module Circuit Functions**			Analysis	**Design**
365	The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.	**4.3.5 Other Module Circuit Functions**		It is unclear what this specification means.	Analysis	**Design**
366	An External WDT "Muzzle" Jumper shall be provided on the board.	**4.3.5 Other Module Circuit Functions**			Inspection	**Design**
368	When the jumper is missing (open), the feature shall not apply.	**4.3.5 Other Module Circuit Functions**		If the standard requires a jumper, why would the performance without the jumper need to be specified.	Inspection	**Design**
369	This feature is required to operate with the Type 210 Monitor Unit only.	**4.3.5 Other Module Circuit Functions**		Unclear as to why this is in the standard.	**Drop from the standard.**	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
370	A WATCHDOG Circuit shall be provided.	**4.3.5 Other Module Circuit Functions**			Inspection	**Design**
371	The WATCHDOG Circuit shall be enabled by the FIELD I/O software at Power Up with a value of 100 milliseconds.	**4.3.5 Other Module Circuit Functions**		How can this requirement possibly be verified?	Analysis	**Design**
372	The enabled state of the WATCHDOG Circuit shall be machine readable and reported in the FI/O status byte.	**4.3.5 Other Module Circuit Functions**			Analysis	**Design**
373	Once enabled, the watchdog timer shall not be disabled without resetting the FI/O.	**4.3.5 Other Module Circuit Functions**			Analysis Performance Test	**Design**
374	Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.	**4.3.5 Other Module Circuit Functions**			Performance Test	**Design**
375	A synchronizable 1 kilohertz time reference shall be provided.	**4.3.5 Other Module Circuit Functions**			Inspection	**Design**
376	The synchronizable time reference shall maintain a frequency accuracy of +/-0.01% (+/-0.1 counts per second).	**4.3.5 Other Module Circuit Functions**			Analysis	**Design**
377	A 32-bit MILLISECOND COUNTER (MC) shall be provided for “timestamping.”	**4.3.5 Other Module Circuit Functions**			Inspection	**Design**
378	Each 1 KHz reference interrupt shall increment the MC.	**4.3.5 Other Module Circuit Functions**			Analysis	**Design**
379	At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the “E” Bit and a subsequent set output command is processed.	**4.3.5 Other Module Circuit Functions**			Analysis Performance Test	**Design**
380	A LOGIC Switch shall be provided resident on the module board.	**4.3.5 Other Module Circuit Functions**			Inspection	**Design**
382	The purpose of the switch is to prevent multiple use of SP3.	**4.3.5 Other Module Circuit Functions**			Analysis	**Design**
384	System Serial Port 5 (SP5) EIA-485 signal lines shall enter the I/O Module and be split into two multi-drop isolated ports.	**4.3.6 Serial Communications/Logic Circuitry**			Analysis	**Design**
385	One [serial port line of SP5] shall be routed to the FCU and the other converted to EIA-485, then routed to Connector C12S.	**4.3.6 Serial Communications/Logic Circuitry**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
386	System Serial Port 3 (SP3) EIA-485 signal lines shall enter the I/O module and be isolated, converted back to EIA-485 and then routed to connector C12S.	**4.3.6 Serial Communications/Logic Circuitry**			Inspection	**Design**
387	LINE SYNC and POWER DOWN lines shall be split and isolated, one routed to the FCU for shut down functions and the other changed to EIA-485; then routed to connector C12S for external module use.	**4.3.6 Serial Communications/Logic Circuitry**			Inspection	**Design**
388	CPU RESET and POWER UP (SYSRESET) lines shall be isolated and "OR'd" to form NRESET.	**4.3.6 Serial Communications/Logic Circuitry**			Inspection	**Design**
389	NRESET shall be used to reset FCU and other module devices.	**4.3.6 Serial Communications/Logic Circuitry**			Analysis	**Design**
390	NRESET shall also be converted to EIA-485 then routed to connector C12S.	**4.3.6 Serial Communications/Logic Circuitry**			Inspection	**Design**
391	If the Type 2070 module is a –2B, then routing to FCU doesn't apply.	**4.3.6 Serial Communications/Logic Circuitry**			Analysis	**Design**
392	Isolation is between internal +5 VDC / Ground #1 and +12 VDC ISO / VDC Ground #2.	**4.3.6 Serial Communications/Logic Circuitry**			Analysis	**Design**
393	+12 VDC ISO is for board power and external logic.	**4.3.6 Serial Communications/Logic Circuitry**			Analysis	**Design**
394	A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries.	**4.3.7 Buffers**			Analysis	**Design**
395	The Transition Buffer shall default to empty.	**4.3.7 Buffers**			Performance Test	**Design**
396	There shall be two entry types (in the Transition Buffer): Transition and Rollover.	**4.3.7 Buffers**			Analysis	**Design**
397	The inputs (to the Transition Buffer) shall be monitored for state transition.	**4.3.7 Buffers**			Analysis	**Design**
398	At each transition (if the input has been configured to report transition), a transition entry shall be added to the Transition Buffer.	**4.3.7 Buffers**			Performance Test	**Design**
399	The MC shall be monitored for rollover.	**4.3.7 Buffers**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>400</td><td>At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer.</td><td>4.3.7 Buffers</td><td></td><td>In order to test this, one needs to know what causes a roll-over and be able to create on during testing.</td><td>Performance Test</td><td>Design</td></tr>
<tr><td>401</td><td>For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry.</td><td>4.3.7 Buffers</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>402</td><td>Transition Buffer blocks are sent to the CPU module upon command.</td><td>4.3.7 Buffers</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>403</td><td>Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer.</td><td>4.3.7 Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>404</td><td>The entry types are depicted as follows:
Input Transition Entry
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>Transition Entry Identifier</td><td>S</td><td colspan="7">Input Number</td><td>1</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>2</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td></tr>
</table>
Millisecond Counter Rollover Entry
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>Rollover Entry Identifier</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>2</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td></tr>
</table></td><td>4.3.7 Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>405</td><td>Input scanning shall begin at I0 (bit 0) and proceed to the highest numbered input, ascending from LSB to MSB.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>406</td><td>Each complete input scan shall finish within 100 microseconds.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>407</td><td>Once sampled, the logic state of an input shall be held until the next input scan.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>408</td><td>Each input shall be sampled 1,000 times per second.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>409</td><td>The time interval between samples shall be 1 millisecond (+/-100 microseconds).</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>410</td><td>If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer.</td><td>4.3.8 I/O Functions</td><td></td><td>How can one view the Transition Buffer?</td><td>Analysis
Performance Test</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
411	If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing input number.	**4.3.8 I/O Functions**			Analysis Performance Test	**Design**
412	The Millisecond Counter shall be sampled within 10 microseconds of the completion of the input scan.	**4.3.8 I/O Functions**			Analysis	**Design**
413	If configured, the inputs shall be filtered by the FCU to remove signal bounce.	**4.3.8 I/O Functions**		What does "if configured" mean in this context? Why would the inputs not be configured?	Analysis	**Design**
414	The filtered input signals shall then be monitored for changes as noted.	**4.3.8 I/O Functions**			Analysis	**Design**
415	The filtering parameters for each input shall consist of Ignore Input Flag and the ON and OFF filter samples.	**4.3.8 I/O Functions**			Analysis	**Design**
416	If the Ignore Input flag is set, no input transitions shall be recorded.	**4.3.8 I/O Functions**			Analysis	**Design**
417	The ON and OFF filter samples shall determine the number of consecutive samples an input must be ON and OFF, respectively, before a change of state is recognized.	**4.3.8 I/O Functions**			Analysis	**Design**
418	If the change of state is shorter than the specified value, the change of state shall be ignored.	**4.3.8 I/O Functions**			Analysis Performance Test	**Design**
419	The ON and OFF filter values shall be in the range of 0 to 255.	**4.3.8 I/O Functions**			Analysis	**Design**
420	A filter value of 0, for either or both values, shall result in no filtering for this input.	**4.3.8 I/O Functions**			Analysis	**Design**
421	The default values for input signals after reset shall be as follows: *Input Signals* — *Default Value* Filtering — Enabled On and off filter values shall be set to — 5 Transition monitoring — Disabled (Timestamps are not logged)	**4.3.8 I/O Functions**			Inspection	**Design**
422	Simultaneous assertion of all outputs shall occur within 100 microseconds.	**4.3.8 I/O Functions**		What does this requirement mean?	Analysis Performance Test	**Design**
423	Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC.	**4.3.8 I/O Functions**			Analysis	**Design**
424	The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module.	**4.3.8 I/O Functions**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>425</td><td>If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the FI/O status byte shall be updated to reflect the loss of communication from the CPU Module.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>426</td><td>The data and control bits in the CPU Module-FI/O frame protocol shall control each output as follows:
Output Bit Translation
<table>
<tr><th>Case</th><th>Output Data Bit</th><th>Output Control Bit</th><th>Function</th></tr>
<tr><td>A</td><td>0</td><td>0</td><td>Output in the OFF state</td></tr>
<tr><td>B</td><td>1</td><td>1</td><td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.</td></tr>
<tr><td>C</td><td>0</td><td>1</td><td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF</td></tr>
<tr><td>D</td><td>1</td><td>0</td><td>Output is in the ON state.</td></tr>
</table></td><td>4.3.8 I/O Functions</td><td></td><td>Can these bits be toggled independently, or via directed software control with some type of emulator?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>427</td><td>In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>428</td><td>For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 microseconds after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>429</td><td>In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remains ON until otherwise configured.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>430</td><td>All outputs shall never change state unless configured to do so.</td><td>4.3.8 I/O Functions</td><td></td><td>“Never” is very, very difficult to test.</td><td>Analysis</td><td>Design</td></tr>
<tr><td>431</td><td>All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>432</td><td>MILLISECOND Interrupt shall be activated by the 1 kilohertz reference once per millisecond.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>433</td><td>An MC timestamp rollover flag set by MC rollover shall be cleared only on command.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>434</td><td>LINESYNC Interrupt – This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal.</td><td>4.3.8 I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
435	The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 kilohertz source for 0.5 seconds (>/=60 consecutive LINESYNC interrupts).	**4.3.8 I/O Functions**			Analysis	**Design**
436	The LINESYNC interrupt shall synchronize the 1 kilohertz time reference with the 0-1 transition of the LINESYNC signal once a second.	**4.3.8 I/O Functions**			Analysis Performance Test	**Design**
437	A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (>/=500 consecutive millisecond interrupts).	**4.3.8 I/O Functions**			Analysis Performance Test	**Design**
438	A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults.	**4.3.8 I/O Functions**			Analysis	**Design**
439	The communication server shall automatically: *For Transmission* Generate the opening and closing flags Generate the CRC value Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU Provide zero bit insertion *For Receiving* Detect the opening and closing flags Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module Strip out inserted zeros Calculate the CRC value, compare it to the received value, and generate an interrupt on an error Generate an interrupt if an abort sequence is received	**4.3.8 I/O Functions**			Analysis Performance Test	**Design**
440	The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission.	**4.3.8 I/O Functions**			Analysis	**Design**
441	The response message transmission shall begin within 4 milliseconds of the receipt of the received message.	**4.3.8 I/O Functions**			Analysis Performance Test	**Design**
442	The time from the receipt of message to the completion of the commanded task shall not exceed 70 milliseconds.	**4.3.8 I/O Functions**		Is there a list of tasks about which this applies?	Analysis Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
443	This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.	**4.3.8 I/O Functions**			Analysis	**Design**
444	All communication with the CPU Module shall be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 kilobits per second.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
445	The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no FI/O response shall be transmitted.	**4.3.9 Data Communications Protocols**		Words such as “never” and “always” are difficult to test.	Analysis Performance Test	**Design**
446	The amount of bytes of a command or response is dependent upon the I/O Module identification.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
447	The frame type shall be determined by the value of the first byte of the message.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
448	The command frames type values 112-127 and associated response frame type values 240-255 are allocated to the manufacturer diagnostics.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
449	All other frame types not called out are reserved.	**4.3.9 Data Communications Protocols**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th>Pass
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>450</td><td>The command-response Frame Type values and message times shall be as follows:
Frame Types
<table>
<tr><th>Module Command</th><th>I/0 Module Response</th><th>Description</th><th>Minimum Message Time</th><th>Maximum Message Time</th></tr>
<tr><td>0-43</td><td>128-171</td><td>Reserved for NEMA TS-2</td><td></td><td></td></tr>
<tr><td>49</td><td>177</td><td>Request Module Status</td><td>250 microseconds</td><td>275 microseconds</td></tr>
<tr><td>50</td><td>178</td><td>MILLISECOND CTR. Mgmt.</td><td>222.5 microseconds</td><td>237.5 microseconds</td></tr>
<tr><td>51</td><td>179</td><td>Configure Inputs</td><td>344.5 microseconds</td><td>6.8750 milliseconds</td></tr>
<tr><td>52</td><td>180</td><td>Poll Raw Input Data</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>53</td><td>181</td><td>Poll Filtered Input Data</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>54</td><td>182</td><td>Poll Input Transition Buffer</td><td>300 microseconds</td><td>10.25 microseconds</td></tr>
<tr><td>55</td><td>183</td><td>Command Outputs</td><td>405 microseconds</td><td>410 microseconds</td></tr>
<tr><td>56</td><td>184</td><td>Reserved</td><td>340 microseconds</td><td>10.25 milliseconds</td></tr>
<tr><td>57</td><td>185</td><td>Reserved</td><td>340 microseconds</td><td>6.875 milliseconds</td></tr>
<tr><td>58</td><td>186</td><td>Configure Watchdog</td><td>222.5 microseconds</td><td>222.5 microseconds</td></tr>
<tr><td>59</td><td>187</td><td>Controller Identification</td><td>222.5 microseconds</td><td>222.5 microseconds</td></tr>
<tr><td>60</td><td>188</td><td>I/O Module Identification</td><td>222.5 microseconds</td><td>222.5 microseconds</td></tr>
<tr><td>61-62</td><td>189-190</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
<tr><td>63</td><td>191</td><td>Poll variable length raw input</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>64</td><td>192</td><td>Variable length command outputs</td><td>405 microseconds</td><td>410 microseconds</td></tr>
<tr><td>65</td><td>193</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
<tr><td>67</td><td>195</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>451</td><td>Messages 61 / 189, 62 / 190, 65 / 193, and 67 / 195 are reserved for ITS Cabinet Frame Types.</td><td>4.3.9 Data Communications Protocols</td><td></td><td>Software design specification.</td><td>Analysis</td><td>Design</td></tr>
<tr><td>452</td><td>Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of input data bytes.</td><td>4.3.9 Data Communications Protocols</td><td></td><td>Software design specification.</td><td>Analysis</td><td>Design</td></tr>
<tr><td>453</td><td>Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes, plus the following output control bytes.</td><td>4.3.9 Data Communications Protocols</td><td></td><td>Software design specification.
Poorly worded.</td><td>Analysis</td><td>Design</td></tr>
<tr><td>454</td><td>The Command shall be used to request FI/O status information response.
Command/response frames are as follows:
Request Module Status Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 49)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Reset Status Bits</td><td>P</td><td>E</td><td>K</td><td>R</td><td>T</td><td>M</td><td>L</td><td>W</td><td>Byte 2</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td>Poorly worded. “This” command?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>455</td><td>Request Module Status Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 177)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>System Status</td><td>P</td><td>E</td><td>K</td><td>R</td><td>T</td><td>M</td><td>L</td><td>W</td><td>Byte 2</td></tr>
<tr><td>SCC Receive Error Count</td><td colspan="8">Receive Error Count</td><td>Byte 3</td></tr>
<tr><td>SCC Transmit Error Count</td><td colspan="8">Transmit Error Count</td><td>Byte 4</td></tr>
<tr><td>MC Timestamp MSB</td><td colspan="8">MC Timestamp MSB</td><td>Byte 5</td></tr>
<tr><td>MC Timestamp NMSB</td><td colspan="8">MC Timestamp NMSB</td><td>Byte 6</td></tr>
<tr><td>MC Timestamp NLSB</td><td colspan="8">MC Timestamp NLSB</td><td>Byte 7</td></tr>
<tr><td>MC Timestamp LSB</td><td colspan="8">MC Timestamp LSB</td><td>Byte 8</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
456	The response status bits are defined as follows: P - Indicates FI/O hardware reset E - Indicates a communications loss of greater than 2 seconds K - Indicates the Datakey has failed or is not present R - Indicates that the EIA-485 receive error count byte has rolled over T - Indicates that the EIA-485 transmit error count byte has rolled over M - Indicates an error with the MC interrupt L - Indicates an error in the LINESYNC W - Indicates that the FI/O has been reset by the Watchdog	**4.3.9 Data Communications Protocols**			Analysis	**Design**
457	The FI/O status byte shall be updated (set to '1') to reflect the faults noted in clause 4.3.9.2.1.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
458	Each status bit shall only be reset (set to '0') when the corresponding bit of the Request Module Status Command is a '1'.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
459	The Request Module Status Response shall report the current status (subsequent to reset and sampling).	**4.3.9 Data Communications Protocols**			Analysis	**Design**
460	The FI/O shall count the number of errored frames the FI/O Communications Processor reports.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
461	Separate counts shall be maintained for transmit and received frames.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
462	When an individual count rolls over (255-0), the corresponding roll-over flag shall be set.	**4.3.9 Data Communications Protocols**			Analysis Performance Test	**Design**
463	FI/O modules with Datakey: On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key.	**4.3.9 Data Communications Protocols**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>467</td><td>The MC timestamp value shall be sampled just prior to the Request Module Status Response.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>468</td><td>MC MANAGEMENT frame shall be used to set the value of the MC.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>469</td><td>The ‘S’ bit shall return status ‘0’ on completion.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>470</td><td>The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>471</td><td>The frames are as follows:
Millisecond Counter Management Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 50)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>New MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>New MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>New MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 4</td></tr>
<tr><td>New MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 5</td></tr>
</table>
Millisecond Counter Management Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 178)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>S</td><td>Byte 2</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>472</td><td>The Configure Inputs command frame shall be used to change input configurations.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>473</td><td>The command-response frames are as follows:
Configure Inputs Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 51)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Number of Items (n)</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>Byte 2</td></tr>
<tr><td>Item # - Byte 1</td><td>E</td><td colspan="7">Input Number</td><td>Byte 3(I-1)+3</td></tr>
<tr><td>Item # - Byte 2</td><td colspan="8">Leading edge filter (e)</td><td>Byte 3(I-1)+4</td></tr>
<tr><td>Item # - Byte 3</td><td colspan="8">Trailing edge filter I</td><td>Byte 3(I-1)+5</td></tr>
</table>
Configure Inputs Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 179)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>S</td><td>Byte 2</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>474</td><td>Block field definitions shall be as follows:
E - Ignore Input Flag. “1” = do not report transitions for this input, “0” = report transitions for this input
e - A one-byte leading edge filter specifying the number of consecutive input samples which must be “0” before the input is considered to have entered to “0” state from “1” state (range 1 to 255, 0 = disabled)
r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be “1” before the input is considered to have entered to “1” state from “0” state (range 1 to 255, 0 = disabled)
S - return status S = ‘0’ on completion or ‘1’ on input error out of range</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>475</td><td>The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>476</td><td>The response frame shall contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current input status.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>477</td><td>The frames are as follows:
Poll Raw Input Data Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 52)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
</table>
Poll Raw Input Data Response (2070-2A)
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 180)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I63</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 9</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 10</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 11</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 12</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 13</td></tr>
</table>
Poll Raw Input Data Response (2070-8)
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 180)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I119</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 16</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 17</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 18</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 19</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 20</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>478</td><td>The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
479	The response frame shall contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
480	Raw input data shall be provided in the response for inputs that are not configured for filtering.	**4.3.9 Data Communications Protocols**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>481</td><td>The frames are as follows:
Poll Filter Input Data Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 53)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Byte 1</td></tr>
</table>
Poll Filter Input Data Response (2070-2A)
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 180)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I63</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 9</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 10</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 11</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 12</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 13</td></tr>
</table>
Poll Filter Input Data Response (2070-8)
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 181)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I119</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 16</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 17</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 18</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 19</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 20</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>482</td><td>The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>483</td><td>The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>484</td><td>The frames are as follows:
Poll Input Transition Buffer Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 54)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Block Number</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table>
Poll Input Transition Buffer Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 182)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Block Number</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Number of Entries</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>Item #</td><td>S</td><td colspan="7">Input Number</td><td>Byte 3(I-1)+4</td></tr>
<tr><td>Item # MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+5</td></tr>
<tr><td>Item # MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+6</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C</td><td>F</td><td>E</td><td>G</td><td>Byte 3(I-1)+7</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+8</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+9</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+10</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+11</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>485</td><td>Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>486</td><td>The FI/O shall set the ‘F’ bit to ‘1’ when attempting to record a transition and the Transition Buffer is full.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
487	While the Transition Buffer is full, all subsequent entries shall be discarded.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
488	Bit definitions are as follows: S - Indicates the state of the input after the transition C - Indicates the 255 transition entries limit has been exceeded F - Indicates the transition buffer limit has been exceeded G - Indicates the requested block number is out of monotonic increment sequence E - Same block number requested, E is set in response	**4.3.9 Data Communications Protocols**			Analysis	**Design**
489	The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
490	When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
491	If the new Block Number is the same as the previously-sent Block Number, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
492	If the new Block Number is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
493	If the block number is not incremented by one, the status G bit shall be set.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
494	The block number received becomes the current number (even if out of sequence).	**4.3.9 Data Communications Protocols**			Analysis	**Design**
495	The Block Number byte sent in the response block shall be the same as that received in the command block.	**4.3.9 Data Communications Protocols**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
496	Counter rollover shall be considered as a normal increment.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
497	The Timestamp shall equal the MC value at the time the Poll Input Transition Buffer Response is generated.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
498	The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
499	If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
500	If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set.	**4.3.9 Data Communications Protocols**			Analysis	**Design**
501	Loss of LINESYNC reference shall also be indicated in system status information.	**4.3.9 Data Communications Protocols**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>502</td><td>The output bytes depend upon field I/O module. These command and response frames are as follows:
Set Outputs Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 55)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Outputs O0 (lsb) to O7 (msb) Data</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Outputs O8 to O103 Data</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 14</td></tr>
<tr><td>Outputs O0 (lsb) to O7 (msb) Control</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 15</td></tr>
<tr><td>Outputs O8 to O103 Control</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 16 to 27</td></tr>
</table>
Set Outputs Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 183)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>L</td><td>E</td><td>Byte 2</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>503</td><td>The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:
Configure Watchdog Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 58)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Timeout Value</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table>
Configure Watchdog Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 186)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Y</td><td>Byte 2</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>504</td><td>The timeout value shall be in the range between 10 to 100 milliseconds.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>505</td><td>If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>506</td><td>On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>507</td><td>The response frame bit (Y) shall indicate a ‘1’ if the watchdog has been previously set and a ‘0’ if not.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>508</td><td>This is a legacy message command / response for FI/O modules with Datakey resident.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>509</td><td>Upon command, a response frame containing the 128 bytes of the Datakey See previous sections on Request Module Status for FI/O Status Bit ‘K’ definition.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>510</td><td>If “K” bit set, only the first two bytes shall be returned.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>511</td><td>The Command and Response frames are as follows:
Controller Identification Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 59)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
</table>
Controller Identification Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 187)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>K</td><td>Byte 2</td></tr>
<tr><td>Datakey</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 130</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>512</td><td>The I/O Module Identification Command frame shall be used to request the FI/O Identification value.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>513</td><td>A response of “1” shall be returned by 2070-2A, “2” by 2070-8, “3” is reserved for NEMA TS 2 Type 1 FI/O and “32 to 40” are reserved for ITS Cabinets.</td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>514</td><td>The command and response frames are shown as follows:
Controller Identification Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 60)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
</table>
Controller Identification Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 188)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>FI/O I D byte</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table></td><td>4.3.9 Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>367</td><td>With the jumper in and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 milliseconds for 10 seconds or due to CPU Command.</td><td>4.3.5 Other Module Circuit Functions</td><td>n/a</td><td>Because of the lack of an external power supply, this one was not conducted.</td><td>Performance Test</td><td>Performance</td></tr>
<tr><td>381</td><td>The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S.</td><td>4.3.5 Other Module Circuit Functions</td><td>P</td><td>On the Field I/O module, there is an actual mechanical switch that provides this functionality.</td><td>Inspection</td><td>Performance</td></tr>
<tr><td>383</td><td>An LED shall be provided on the module front panel labeled “SP3 ON”. If LED light ON, SP3 is active and available at C12S.</td><td>4.3.5 Other Module Circuit Functions</td><td>P</td><td>Verified as per above.</td><td>Performance Test</td><td>Performance</td></tr>
<tr><td>464</td><td>FI/O modules with Datakey: If [the Datakey is] absent, Status Bit “K” shall be set to ‘1’ and no interrogation shall take place.</td><td>4.3.9 Data Communications Protocols</td><td>n/a</td><td>This is a legacy requirement that is obsolete. It serves the purpose to allow software written for older Field I/O modules to work either way.</td><td>Performance Test</td><td>Performance</td></tr>
<tr><td>465</td><td>FI/O modules with Datakey: If an error occurs during the interrogation, Status Bit “K” shall be set to ‘1’.</td><td>4.3.9 Data Communications Protocols</td><td>n/a</td><td></td><td>Performance Test</td><td>Performance</td></tr>
<tr><td>466</td><td>FI/O modules without Datakey: Status Bit “K” shall always be set to ‘1’</td><td>4.3.9 Data Communications Protocols</td><td>n/a</td><td></td><td>Performance Test</td><td>Performance</td></tr>
</table>

B.5 ATC Type 2070 Front Panel Assembly Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
	The Command Codes shall use the following conventions:					
517	Each key shall have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure.	**4.4.2 Front Panel Assembly – Keyboards**		"Positive tactile indication" is a nebulous specification.	Performance Test	**Design**
518	Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 milliseconds following contact closure.	**4.4.2 Front Panel Assembly – Keyboards**		Design life is a manufacturing specification.	Analysis	**Design**
521	Display A shall have 4 lines of 40 characters each with a minimum character dimension of 0.20 inches wide by 0.41 inches high and an electro – luminescent (EL) backlight.	**4.4.4 Front Panel Assembly – Display**			Inspection	**Design**
523	Each character shall be composed of a 5 x 7 dot matrix with a underline row or a 5 x 8 dot matrix.	**4.4.4 Front Panel Assembly – Display**			Analysis	**Design**
524	The viewing angle of the LCD shall be optimized for direct (90 degrees) viewing, +/-35 degrees vertical, +/-45 degrees horizontal.	**4.4.4 Front Panel Assembly – Display**			Analysis	**Design**
525	The LCD shall have variable contrast with a minimum ratio of 4:1.	**4.4.4 Front Panel Assembly – Display**			Analysis	**Design**
526	The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.	**4.4.4 Front Panel Assembly – Display**		What does "user-defined" mean and how would one know? It appears that the display only needs to handle a subset of the ASCII set.	Inspection	**Design**
528	The backlight and associated circuitry shall consume no power when in off state.	**4.4.4 Front Panel Assembly – Display**			Performance Test	**Design**
530	The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.	**4.4.4 Front Panel Assembly – Display**			Performance Test	**Design**
531	Cursor display shall be turned ON and OFF by command.	**4.4.4 Front Panel Assembly – Display**			Performance Test	**Design**
532	When [the Display is] ON, the cursor shall be displayed at the current cursor position.	**4.4.4 Front Panel Assembly – Display**			Performance Test	**Design**
533	When [the Display is] OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.	**4.4.4 Front Panel Assembly – Display**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
534	The FPA CONTROLLER shall function as the Front Panel Device controller interfacing with the CPU Module.	**4.4.5 Front Panel Assembly – FPA Controller**		What does this specification mean?	Analysis	**Design**
536	The momentary CONTROL switch shall be logic OR'd with the CPU RESET Line, producing a FPA RESET Output.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
537	Upon FPA RESET being active or receipt of a valid Soft Reset display command, the following shall occur: 1. Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF. 2. Each special character shall be set to ASCII SPC (space). 3. The tab stops shall be set to columns 9, 17, 25, and 33. 4. The backlight timeout value shall be set to 6 (60 seconds). 5. The backlight shall be extinguished. 6. The display shall be cleared (all ASCII SPC). 7. The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware RESET BUTTON IS PUSHED. The string is "ESC [PU", hex value "1B 5B 50 55".	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
538	When a keypress is detected, the appropriate key code shall be transmitted to SP6-RxD.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
539	If two or more keys are depressed simultaneously, no code shall be sent.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
540	If a key is depressed while another key is depressed, no additional code shall be sent.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
541	Auto-repeat shall be turned ON and OFF by command.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
542	When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
543	When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
544	The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis Performance Test	**Design**
545	Undefined characters shall be ignored.	**4.4.5 Front Panel Assembly – FPA Controller**		How can an undefined character be generated by the keyboard? If a character is undefined, how can this requirement be tested?	Analysis	**Design**
546	User-composed characters shall be represented in the communication protocol on Page 9-7-12.	**4.4.5 Front Panel Assembly – FPA Controller**		**Error**: Should be 4-7-12 and should be designated as "diagram number" not page.	Analysis	**Design**
547	P1 represents the special character number (1-8).	**4.4.5 Front Panel Assembly – FPA Controller**		What purpose does this clause serve in a standard?	Analysis	**Design**
548	Pn's represent columns of pixels from left to right.	**4.4.5 Front Panel Assembly – FPA Controller**		What purpose does this clause serve in a standard?	Analysis	**Design**
549	The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
550	A logic '1' shall turn the pixel ON.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
551	There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f."	**4.4.5 Front Panel Assembly – FPA Controller**			Inspection	**Design**
552	If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
553	P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.	**4.4.5 Front Panel Assembly – FPA Controller**			Inspection	**Design**
554	Character overwrite mode shall be the only display mode supported.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
555	A displayable character received shall always overwrite the current cursor position on the Display.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
556	The cursor shall automatically move right one character position on the Display after each character write operation.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
557	When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis Performance Test	**Design**
558	Auto-wrap shall be turned ON & OFF by command.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
559	When ON, a new line operation shall be performed after writing to position 40.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
560	When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
562	Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis Performance Test	**Design**
563	Blinking characters shall be supported, and shall be turned ON and OFF by command.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
564	When ON, all subsequently received displayable characters shall blink at the rate of 1 Hertz with a 60% ON / 40% OFF duty cycle.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
565	It shall be possible to display both blinking and non-blinking characters simultaneously.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
566	Tab Stops shall be configurable at all columns.	**4.4.5 Front Panel Assembly – FPA Controller**		Why are Tab Stops being defined in a standard?	**Drop from the standard.**	**Design**
567	A tab stop shall be set at the current cursor position when a SetTabStop command is received.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
568	Tab Stop(s) shall be cleared on receipt of a ClearTabStop command.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
569	On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
570	If no tab stop is set to the right of the current cursor position, the cursor shall not move.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
571	Auto-scroll shall be turned ON and OFF by command.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
572	When [Auto-scroll is] ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
573	When [Auto-scroll is] OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
574	The display shall have a buffer.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
575	The screen shall be refreshed from the buffer at a rate of no less than 20 times per second.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
576	The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
578	This time [the backlight extinguish time] shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis Performance Test	**Design**
579	A value of 1 shall correspond to a timeout interval of 10 seconds.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
580	A value of 0 shall indicate no timeout.	**4.4.5 Front Panel Assembly – FPA Controller**			Performance Test	**Design**
582	1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows: Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros. P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.) Px: Display column number (1-40), using one ASCII character per digit without leading zero. Py: Display line (1-4) one ASCII character …: Continue the list in the same fashion Values of 'h' (0x68) and 'l' (0x6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
583	2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
584	3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 0x00 to 0x7F (7 bits).	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
585	The Controller Circuit shall communicate via a SP6 asynchronous serial interface.	**4.4.5 Front Panel Assembly – FPA Controller**			Inspection	**Design**
586	The interface shall be configured for 38.4 kilobits per second, 8 data bits, 1 stop bit, and no parity.	**4.4.5 Front Panel Assembly – FPA Controller**			Analysis	**Design**
587	C50 ENABLE function when grounded by pins 1 and 5, shall be brought to Connectors A1, pin B21 for the purpose of disabling the module channel 2, (SP4).	**4.4.5 Front Panel Assembly – FPA Controller**			Inspection	**Design**
588	The Front Panel shall include an electronic bell to signal receipt of (0x07).	**4.4.6 Front Panel Assembly – Electronic Bell**			Performance Test	**Design**
589	The bell shall sound at 2,000 Hertz, with a minimum output rating of 85 dB upon receipt of (0x07).	**4.4.6 Front Panel Assembly – Electronic Bell**			Performance Test	**Design**
590	Receipt of all other characters and ESC codes shall continue during the time the bell sounds.	**4.4.6 Front Panel Assembly – Electronic Bell**			Analysis	**Design**
515	Two KEYBOARDS shall be provided, one with sixteen keys for hexadecimal alpha-numeric entry and the other with twelve keys to be used for cursor control and action symbol entry.	**4.4.2 Front Panel Assembly – Keyboards**	P		Inspection	**Performance**
516	Each key shall be engraved or embossed with its function character. **Note**: The operational need here is that the key designations should not wear off, no matter the amount of use.	**4.4.2 Front Panel Assembly – Keyboards**	P	Does “engraved” or “embossed” refer to the depth of the characters? The version we saw was perfectly smooth.	Inspection	**Performance**
519	The cathode of the CPU ACTIVE LED INDICATOR shall be electrically connected to the CPU Activity LED signal and shall be pulled up to +5 VDC.	**4.4.3 CPU Active Indicator**	P		Inspection	**Performance**
520	The DISPLAY shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control.	**4.4.4 Front Panel Assembly – Display**	P		Inspection	**Performance**
522	Display B shall have 8 lines of 40 characters each with minimum dimensions of 0.10 inches wide by 0.17 high and either LED or EL backlight.	**4.4.4 Front Panel Assembly – Display**	P		Analysis	**Performance**
527	The backlight shall be turned on and off by the Controller Circuitry.	**4.4.4 Front Panel Assembly – Display**	P		Performance Test	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
529	A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast.	**4.4.4 Front Panel Assembly – Display**	P		Inspection	**Performance**
535	A FPA RESET Switch shall be provided on the Assembly PCB.	**4.4.5 Front Panel Assembly – FPA Controller**	P		Inspection	**Performance**
561	Cursor positioning shall be non-destructive.	**4.4.5 Front Panel Assembly – FPA Controller**	P		Performance Test	**Performance**
577	The backlight shall extinguish when no key is pressed for a specified time.	**4.4.5 Front Panel Assembly – FPA Controller**	P	It is not clear if there is a default time for this requirement.	Performance Test	**Performance**

B.6 ATC Type 2070 Power Supply Module Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
593	The Type 2070-4B Module shall meet the same requirements as the 2070-4A, except for 3.5 amperes of +5 VDC.	**4.5.1 Power Supply Module – General**			Analysis	**Design**
595	The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.	**4.5.2 Power Supply Module – Module Front**			Analysis	**Design**
596	Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 micro Henries inductance shall be provided (one on the AC+ Line & on the AC- Line).	**4.5.3 Power Supply Module – Input Protection**			Inspection	**Design**
597	Three 20 Joule surge arrestors shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arrestors).	**4.5.3 Power Supply Module – Input Protection**			Analysis	**Design**
598	+5 VDC STANDBY POWER shall be provided to hold up specified circuitry during the power down period.	**4.5.4 +5VDC Standby Power**			Analysis	**Design**
599	It [standby power] shall consist of the monitor circuitry, hold up capacitors, and charging circuitry.	**4.5.4 +5VDC Standby Power**			Analysis	**Design**
600	A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations.	**4.5.4 +5VDC Standby Power**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
601	The Hold Up power requirements shall be a minimum constant drain of 600 microamperes at a range of +5 VDC to +2 VDC for over 600 minutes.	**4.5.4 +5VDC Standby Power**			Performance Test	**Design**
602	MONITOR CIRCUITRY shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.	**4.5.5 Power Supply Module – Monitor Circuitry**			Analysis	**Design**
603	The ACFAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately upon Power Failure.	**4.5.5 Power Supply Module – Monitor Circuitry**			Analysis	**Design**
604	The Lines shall transition to HIGH at Power Restoration.	**4.5.5 Power Supply Module – Monitor Circuitry**			Analysis	**Design**
605	The Lines shall be driven separately.	**4.5.5 Power Supply Module – Monitor Circuitry**		Poorly written.	Inspection	**Design**
608	The Lines shall be driven separately.	**4.5.5 Power Supply Module – Monitor Circuitry**		Poorly written.	Inspection	**Design**
612	The output shall have drive sink capability of 16 milliamperes.	**4.5.5 Power Supply Module – Monitor Circuitry**		This is a performance requirement with little context. Why this specific capability is needed and how this Ma figure was arrived at is at question.	Analysis	**Design**
613	A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC.	**4.5.5 Power Supply Module – Monitor Circuitry**			Inspection	**Design**
615	The LINESYNC shall continue until SYSRESET transitions LOW and begin when SYSRESET transitions HIGH.	**4.5.5 Power Supply Module – Monitor Circuitry**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th>Pass
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>616</td><td>
<table>
<tr><th>Voltage</th><th>Tolerances</th><th>I Minimum</th><th>I Maximum</th></tr>
<tr><td>+5 VDC</td><td>+4.875 to +5.125 VDC</td><td>1.0 ampere</td><td>10.0 ampere- MODULE 2070-4A
3.5 ampere– MODULE 2070-4B</td></tr>
<tr><td>+12 VDC Serial</td><td>+11. 4 to +12. 6 VDC</td><td>0.1 ampere</td><td>0.5 ampere</td></tr>
<tr><td>-12 VDC Serial</td><td>-11. 4 to –12. 6 VDC</td><td>0.1 ampere</td><td>0.5 ampere</td></tr>
<tr><td>+12 VDC</td><td>+11. 4 to +12. 6 VDC</td><td>0.1 AMP</td><td>1.0 AMP</td></tr>
</table>
</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>617</td><td>Line / Load Regulation shall meet the table tolerance values for voltage range of 90 to 135 VDC, the maximum and minimum loads called out in the table and including ripple noise.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>618</td><td>Power Supply Efficiency shall be 70% minimum.</td><td>4.5.6 Power Supply Requirements</td><td></td><td>What does this standard mean relative to the performance of the device?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>619</td><td>Power Supply Ripple and Noise shall be less than 0.2% RMS, 1% peak to peak or 50 millivolts, whichever is greater.</td><td>4.5.6 Power Supply Requirements</td><td></td><td>What does this standard mean relative to the performance of the device?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>620</td><td>Power Supply Output Overshoot shall be no greater than 5%, all outputs.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>621</td><td>Power Supply Overvoltage Protection shall be 130% Vout for all outputs.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>622</td><td>Power Supply Circuit protection shall be implemented to provide automatic recovery upon removal of fault.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>623</td><td>Power Supply Cold Start Inrush shall be less than 25 amperes at 115VAC.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>624</td><td>Power Supply Transient response shall be such that output voltage back to within 1% in less than 500 microseconds on a 50% Load change.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>625</td><td>Power Supply Transient response shall be such that peak transient not to exceed 5%.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>628</td><td>Power Supply Remote sense shall be implemented such that +5 VDC compensates 250 millivolts total line drop.</td><td>4.5.6 Power Supply Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>629</td><td>Power Supply open sense load protection required.</td><td>4.5.6 Power Supply Requirements</td><td></td><td>What does this mean?</td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
591	The Type 2070-4A Power Supply Module shall be independent, self contained Module, vented, and cooled by convection only.	**4.5.1 Power Supply Module – General**	P		Analysis	**Performance**
592	The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.	**4.5.1 Power Supply Module – General**	P		Inspection	**Performance**
594	An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front.	**4.5.2 Power Supply Module – Module Front**	P		Inspection	**Performance**
606	The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/-25 milliseconds after ACFAIL/POWER DOWN transition to LOW.	**4.5.5 Power Supply Module – Monitor Circuitry**	P		Analysis Performance Test	**Performance**
607	The Lines shall transition to HIGH 225 +/-25 milliseconds after Power Restoration and the supply is fully recovered.	**4.5.5 Power Supply Module – Monitor Circuitry**	P		Analysis Performance Test	**Performance**
609	The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.	**4.5.5 Power Supply Module – Monitor Circuitry**	P		Analysis Performance Test	**Performance**
610	The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall be synchronized to the 60-Hertz VAC incoming power line at 120 and 300 degrees.	**4.5.5 Power Supply Module – Monitor Circuitry**	P		Analysis	**Performance**
611	A continuous square wave signal shall be +5 VDC amplitude, 8.333 milliseconds half-cycle pulse duration, and 50 +/-1% duty cycle.	**4.5.5 Power Supply Module – Monitor Circuitry**	P		Analysis Performance Test	**Performance**
614	The monitor circuit shall compensate for missing pulses and line noise during normal operation.	**4.5.5 Power Supply Module – Monitor Circuitry**	P		Analysis	**Performance**
626	The power supply shall supply 30 watts minimum for 550 milliseconds after ACFAIL going LOW.	**4.5.6 Power Supply Requirements**	P		Performance Test	**Performance**
627	The power supply shall be capable of holding up the Unit for two 500 milliseconds Power Loss periods occurring in a 1.5-second period.	**4.5.6 Power Supply Requirements**	P		Analysis Performance Test	**Performance**

B.7 ATC Type 2070 VME Cage Assembly Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
630	The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s).	**4.6.1 VME Cage Assembly – General**			Inspection	**Design**
631	All external screws shall be countersunk and shall be Phillips flat head stainless steel type.	**4.6.1 VME Cage Assembly – General**			Inspection	**Design**
632	The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide.	**4.6.1 VME Cage Assembly – General**			Inspection	**Design**
633	The Chassis shall be cooled by convection only.	**4.6.1 VME Cage Assembly – General**			Inspection	**Design**
634	The top and bottom pieces of the housing shall be slotted for vertical ventilation.	**4.6.1 VME Cage Assembly – General**			Inspection	**Design**
635	Serial Motherboard shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits.	**4.6.2 VME Cage Assembly – Serial Motherboard**			Analysis	**Design**
636	The PCB shall be multi-layered, with one layer plane assigned to DC Ground.	**4.6.2 VME Cage Assembly – Serial Motherboard**			Analysis	**Design**
637	A wiring harness PS2 shall be provided between the Type 2070-4 Power Supply and the Motherboard PCB (provide strain relief).	**4.6.2 VME Cage Assembly – Serial Motherboard**		Manufacturing specification. Appropriate for a standard?	Inspection	**Design**
638	Test points shall be provided on the FPA side of the Motherboard for PS2 lines.	**4.6.2 VME Cage Assembly – Serial Motherboard**			Inspection	**Design**
639	A wiring harness FP shall be provided, linking the Motherboard with the FPA.	**4.6.2 VME Cage Assembly – Serial Motherboard**		Manufacturing specification. Appropriate for a standard?	Inspection	**Design**
640	Type 2070-5 VME Cage Assembly shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness.	**4.6.3 Type 2070-5 VME Cage Assembly**		Why is this part of a standard?	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
641	The VME Cage shall conform to VME Standard IEEE P1014/D12 for 3U Cage. All slot/connectors shall be A24:D16 Interface.	**4.6.3 Type 2070-5 VME Cage Assembly**		Need to dig up this specification. Manufacturing specification. Appropriate for a standard?	Inspection	**Design**
642	The Type 2070 – 1A CPU Main Controller Board shall either be affixed to the Transition Board via at least four stand-off devices or mounted in a one slot VME board assembly (removable).	**4.6.4 Type 2070-1A CPU Main Controller Board**		Manufacturing specification. Appropriate for a standard?	Inspection	**Design**
643	A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector.	**4.6.4 Type 2070-1A CPU Main Controller Board**		Manufacturing specification. Appropriate for a standard?	Inspection	**Design**
644	The VME bus lines shall be terminated by a 100-Ohm resistor per line.	**4.6.4 Type 2070-1A CPU Main Controller Board**			Analysis	**Design**

B.8 ATC Type 2070 Peripheral Equipment Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
	General Notes					
645	1. The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA-232 control lines (TX, RX, RTS, CTS, and DCD) when a ground true state is present at Connector A1, Pin B21 (C50 Enable). The disable lines shall be pulled up on this module				Inspection	**Design**
646	2. Line drivers/receivers shall be socket mounted or surface mounted.			What other mounting options exist? If drivers can be mounted either way, why is it specified?	**Drop from the standard.**	
647	3. Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each modules's circuit shall be capable of reliably passing a minimum of 1.0 megabits per second.			Manufacturing specification.	Analysis	**Design**
648	4. The Comm modules shall be "Hot" swappable without damage to circuitry or operations.			Can this be tested with damaging the modules?	Analysis Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
649	A fused isolated +5 VDC with a minimum of 100 milliamperes power supply shall be provided for external use. Option – Bourns MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse, or approved equal, allowed.	**5.1.1 2070-6 A & B – Power Requirements**			Inspection	**Design**
650	Two LOGIC switches per circuit shall be provided (faceplate mounted).	**5.1.2 2070-6 A & B – Logic Switches**		Why two (2) versus three (3)?	Inspection	**Design**
651	One logic switch shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up).	**5.1.2 2070-6 A & B – Logic Switches**			Inspection	**Design**
652	In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.	**5.1.2 2070-6 A & B – Logic Switches**			Analysis	**Design**
653	A MODEM Enable switch shall be provided such that when in the UP Position shall enable MODEM and disable MODEM in the DOWN Position.	**5.1.2 2070-6 A & B – Logic Switches**			Inspection Analysis	**Design**
654	Two circuits, designated CIRCUIT #1 and CIRCUIT #2, shall be provided.	**5.1.3 2070-6 A & B – Circuitry**			Inspection	**Design**
655	Both circuit functions shall be identical, except for their Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and C2S Connector and CIRCUIT #2 to SP2 [or SP4] and C20S Connector).	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
656	The Circuits shall convert the 2070 UNIT Motherboard SP EIA-485 signals to/from board TTL level signals, isolate and drive the converted EIA-232 Signals interfacing with their associated MODEM and external connector.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
657	Each CIRCUIT shall have a MODEM with the following requirements:	**5.1.3 2070-6 A & B – Circuitry**				**Design**
658	1. Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 600 for Module 2070-6B.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
659	2. Modulation: Phase coherent frequency shift keying (FSK).	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
660	3. Data Format: Asynchronous, serial by bit.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
661	4. Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive):2070-6A - 1.2 KHz MARK and 2.2 KHz SPACE, +/-1% tolerance. 2070-6B - 11.2 KHz MARK and 17.6 KHz SPACE, +/-1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & 2.4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
662	5. Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
663	6. Receiver Input Sensitivity: 0 to -40 dB.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
664	7. Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
665	8. Clear-to-Send (CTS) Delay: 11 +/-3 milliseconds.	**5.1.3 2070-6 A & B – Circuitry**			Performance Test	**Design**
666	9. Receive Line Signal Detect Time: 8 +/-2 milliseconds mark frequency.	**5.1.3 2070-6 A & B – Circuitry**			Performance Test	**Design**
667	10. Receive Line Squelch: 6.5 (+/-1) milliseconds, 0 milliseconds (OUT).	**5.1.3 2070-6 A & B – Circuitry**			Performance Test	**Design**
668	11. Soft Carrier Turn Off Time: 10 +/-2 milliseconds (0.9 kilohertz for 2070- 6A and 7.8 kilohertz for 2070-6B). When the RTS is unasserted, the carrier shall turn off or go to soft carrier frequency.	**5.1.3 2070-6 A & B – Circuitry**			Performance Test	**Design**
669	12. Modem Recovery Time: Capable of receiving data within 22 milliseconds after completion of transmission.	**5.1.3 2070-6 A & B – Circuitry**			Performance Test	**Design**
670	13. Error Rate: Shall not exceed 1 bit in 100 kilobits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hertz band.	**5.1.3 2070-6 A & B – Circuitry**			Performance Test	**Design**
671	14. Transmit Noise: Less than -50 dB across 600-ohms resistive load within the frequency spectrum of 300 to 3,000 Hertz at maximum output.	**5.1.3 2070-6 A & B – Circuitry**			Analysis	**Design**
672	15. Modem interface: EIA-232 Standards.	**5.1.3 2070-6 A & B – Circuitry**		Need to dig up this specification.	Analysis	**Design**
673	A CONTROL switch shall be provided on the module front panel to turn ON (Up) / OFF (Down) all module power.	**5.1.4 2070-6 A & B – Control Switch**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
674	Two circuits, designated CIRCUIT #1 and CIRCUIT #2, shall be provided.	**5.2.1 2070-7A & 7B – Circuitry**			Inspection	**Design**
675	The functions [of the two separate circuits] are identical, except for the CPU Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and Connector C21S and CIRCUIT #2 to SP2 [or SP4] and Connector C22S).	**5.2.1 2070-7A & 7B – Circuitry**			Inspection Analysis	**Design**
676	Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to / from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors.	**5.2.2 2070 -7A**			Analysis	**Design**
677	Connectors shall be DB-9S type.			Manufacturing specification?	Inspection	**Design**
678	Each circuit EIA-485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors.	**5.2.3 2070 - 7B**			Analysis	**Design**
679	Connectors shall be DB-15S type.	**5.2.3 2070 - 7B**		Manufacturing specification?	Inspection	**Design**
680	Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled to function.	**5.2.4 2070-7A & 7B – Indicators**			Inspection	**Design**

B.9 ATC Type 2070-2N NEMA Field I/O Module Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
681	The 2070-2N Field I/O Module provides a TS2-1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor Logic Output via 2070 Serial Port 5 and Output Frame Byte 9 Bit 6 to the NEMA TS2 Cabinet Monitor Unit (CMU).	**6.2.1 Interfaces**			Analysis	**Design**
682	The Module shall meet the 2070–2A Module Requirements with the following exceptions: No C1, C11 and C12 Connectors on the front panel of the module No 64 inputs / 64 outputs requirements Serial Port 5 routed to the FCU MPU Device only Serial Port 3 shall not have a disabling switch	**6.2.2 Type 2070-2N Module Requirements**			Inspection	**Design**
683	The module shall be a 4X type board / front panel with three connectors.	**6.2.3 Physical**			Inspection	**Design**
684	The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a 15 Pin DB 15S C14 Connector.	**6.2.3 Physical**			Inspection	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>685</td><td>Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground).</td><td>6.2.4 Power</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>686</td><td>The power is directly routed to the NEMA 5-15 Receptacle.</td><td>6.2.4 Power</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>687</td><td>Connector A shall intermate with a NEMA TS2 Type 1 (MS3106O-18-1S) cable.</td><td>6.2.4 Power</td><td></td><td>“intermate”? What type of word is that?</td><td>Inspection</td><td>Design</td></tr>
<tr><td>688</td><td>The module shall isolate 2070 Serial Port 3 from the A3 Connector and reconvert the lines to external EIA 485 drivers/receivers which shall be terminated at C14 Connector.</td><td>6.2.5 Serial Port 3 Isolation</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>689</td><td>The Port shall be clocked at 153.6 kilobits per second.</td><td>6.2.5 Serial Port 3 Isolation</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>690</td><td>An FCU output shall drive a open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output.</td><td>6.2.6 FCU Output</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>691</td><td>The transistor shall be capable of sinking 200 milliamperes at 30 VDC.</td><td>6.2.6 FCU Output</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>692</td><td>Connectors A and C14 pin out and functions are as follows:
Connector A
<table>
<tr><th>Pin</th><th>Function</th><th>Pin</th><th>Function</th><th>Pin</th><th>Function</th></tr>
<tr><td>A</td><td>AC Neutral</td><td>E</td><td>NA</td><td>I</td><td>NA</td></tr>
<tr><td>B</td><td>NA</td><td>F</td><td>Fault Monitor J</td><td>NA</td><td></td></tr>
<tr><td>C</td><td>AC Line</td><td>G</td><td>DC#2 Ground</td><td></td><td></td></tr>
<tr><td>D</td><td>NA</td><td>H</td><td>Equip Ground</td><td></td><td></td></tr>
</table>
Connector C14S
<table>
<tr><th>Pin</th><th>Function</th><th>Pin</th><th>Finction</th><th>Pin</th><th>Function</th></tr>
<tr><td>1</td><td>TX Data+</td><td>6</td><td>DC Ground</td><td>11</td><td>TX Clock -</td></tr>
<tr><td>2</td><td>DC Ground</td><td>7</td><td>RX Clock +</td><td>12</td><td>Equip Ground</td></tr>
<tr><td>3</td><td>TX Clock+</td><td>8</td><td>DC Ground</td><td>13</td><td>RX Data -</td></tr>
<tr><td>4</td><td>DC Ground</td><td>9</td><td>TX Data -</td><td>14</td><td>NA</td></tr>
<tr><td>5</td><td>RX Data+</td><td>10</td><td>NA</td><td>15</td><td>RX Clock –</td></tr>
</table></td><td>6.2.7 Connector Pin Assignments</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>693</td><td>Serial Port 3 shall control the TS2 BIU Units using SDLC Protocol that meets the NEMA TS2 Type 1 Frame Command / Response Standards.</td><td>6.2.8 TS2 BIU Control</td><td></td><td>Need to dig up this specification.</td><td>Analysis</td><td>Design</td></tr>
</table>

B.10 ATC Type 2070-4N NEMA Power Supply Module Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
694	The 2070-4N Power Supply Module supports the NEMA TS1 and TS2 Standards. The module is identical to the 2070-4N (A and B) Power Supply Requirements except for the following:	**6.3.1 Requirements**				**Design**
695	1) The power cord shall have a 15 inch +/- 1 inch length as measured from the panel to the plug tips.	**6.3.1 Requirements**			Inspection	**Design**
696	2) The AC Power Fail voltage shall be 85VAC +/-2VAC.	**6.3.1 Requirements**			Inspection	**Design**
697	3) The AC Power Restore voltage shall be 90VAC +/-2VAC.	**6.3.1 Requirements**			Analysis	**Design**
698	4) The 2070-4N (A or B) power supply shall have proper marking Example “2070 4N (A or B)”. A permanent sticker shall be an acceptable marking method.	**6.3.1 Requirements**			Inspection	**Design**

B.11 ATC Type 2070-8 NEMA Field I/O Module Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
	The MODULE FRONT PANEL shall be furnished with the following:					
704	1. ON/OFF POWER Switch mounted vertically with ON in the UP position.	**6.4.2 Module Front Panel**			Inspection	**Design**
705	2. LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 5% and the +24 VDC is within 8%.	**6.4.2 Module Front Panel**			Analysis	**Design**
706	3. Incoming VAC fuse protection.	**6.4.2 Module Front Panel**			Inspection	**Design**
707	4. Two DB-25S COMM connectors labeled "EX1" & "EX2."	**6.4.2 Module Front Panel**			Inspection	**Design**
708	5. Four NEMA Connectors A, B, C, & D.	**6.4.2 Module Front Panel**			Inspection	**Design**
709	A permanent LABEL shall be affixed to the Front Panel.	**6.4.3 Label**			Inspection	**Design**
710	The label shall display the unit's serial number.	**6.4.3 Label**			Inspection	**Design**
711	The number shall be permanent and easy to read.	**6.4.3 Label**		“Easy to read” is a poor specification.	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
712	A MODULE POWER SUPPLY shall be provided and located on the right side of the module as viewed from the front.	**6.4.4 Module Power Supply**			Inspection	**Design**
713	The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control.	**6.4.4 Module Power Supply**			Analysis	**Design**
714	The supply shall [also] meet the following requirements:	**6.4.4 Module Power Supply**				**Design**
715	The standard contains this language: "Specification 4.5.6 POWER SUPPLY REQUIREMENTS except Specification 4.5.3. In the previous section, the standard specifies that Specification 4.5.3 applies.	**6.4.4 Module Power Supply**		There is confusion in the specification.	**Obtain clarification.**	**Design**
716	Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 micro Henries inductance shall be provided (one on the AC+ Line & on the AC- Line).	**6.4.4 Module Power Supply**			Inspection	**Design**
717	Three 20 Joule surge arrestors shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arrestors).	**6.4.4 Module Power Supply**			Analysis	**Design**
719	Line / Load Regulation shall meet the table tolerance values for voltage range of 90 to 135 VDC, the maximum and minimum loads called out in the table and including ripple noise.	**6.4.4 Module Power Supply**			Analysis	**Design**
720	Power Supply Efficiency shall be 70% minimum.	**6.4.4 Module Power Supply**		What does this standard mean relative to the performance of the device?	Analysis	**Design**
721	Power Supply Ripple and Noise shall be less than 0.2% RMS, 1% peak to peak or 50 millivolts, whichever is greater.	**6.4.4 Module Power Supply**		What does this standard mean relative to the performance of the device?	Analysis	**Design**
722	Power Supply Output Overshoot shall be no greater than 5%, all outputs.	**6.4.4 Module Power Supply**			Analysis	**Design**
723	Power Supply Overvoltage Protection shall be 130% Vout for all outputs.	**6.4.4 Module Power Supply**			Analysis	**Design**
724	Power Supply Circuit protection shall be implemented to provide automatic recovery upon removal of fault.	**6.4.4 Module Power Supply**			Analysis	**Design**
725	Power Supply Cold Start Inrush shall be less than 25 amperes at 115VAC.	**6.4.4 Module Power Supply**			Performance Test	**Design**
726	Power Supply Transient response shall be such that output voltage back to within 1% in less than 500 microseconds on a 50% Load change.	**6.4.4 Module Power Supply**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
730	Power Supply Remote sense shall be implemented such that +5 VDC compensates 250 millivolts total line drop.	**6.4.4 Module Power Supply**			Analysis	**Design**
731	Power Supply open sense load protection required.	**6.4.4 Module Power Supply**		What does this mean?	Analysis	**Design**
732	DC Voltage tolerances shall be +/-3%.	**6.4.4 Module Power Supply**			Analysis	**Design**
733	The supplied INCOMING AC POWER shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral).	**6.4.5 Incoming AC Power**			Inspection	**Design**
734	External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN."	**6.4.5 Incoming AC Power**			Inspection	**Design**
735	AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.	**6.4.5 Incoming AC Power**			Inspection	**Design**
736	A MODULE PC Boards shall be mounted vertically.	**6.4.6 Module PC Boards**			Inspection	**Design**
737	Power Down, NRESET, and LINESYNC shall be routed to the module via C12 Connector.	**6.4.7 Power Down, NRESET, and LINESYNC**			Inspection	**Design**
738	The state of the module output ports at the time of Power Down transition to LOW State and until NRESET goes HIGH shall be an open circuit.	**6.4.7 Power Down, NRESET, and LINESYNC**			Analysis	**Design**
739	The requirements from section 4.3 are repeated here for clarity, with all exceptions, as described in the standard.	**6.4.8 Compliance with Type 2070-2 Field I/O Requirements**				**Design**
740	Parallel Ports, consisting of 118 Bits of Input and 102 bits of Output, shall be provided.	**6.4.8.1 Parallel I/O Ports**		The requirements between Sections 6.4.8 and Section 6.4.9 are copied from Section 4.3, as specified in the Standard, and numbered to fit.	Analysis	**Design**
743	The I/O Ports shall provide 64 bits of output.	**6.4.8.1 Parallel I/O Ports**		Is “ground-true” logic important here? Why or why not? What is ground-true logic? It sounds like a brand name.	Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
744	Inputs shall have the following characteristics: 1. A voltage between 0 and 4 volts shall be considered the **Low** (True/Operate) state. 2. A voltage greater than 8 volts shall be considered the **High** (False) state. 3. The transition from the **Low** state to **High** state (and vice versa) shall occur between 4 and 8 volts.	**6.4.8.1 Parallel I/O Ports**			Analysis	**Design**
745	Outputs shall have the following characteristics: 1. The **Low** (True/Operate) voltage shall be between 0 and 3 volts. 2. Current sinking capability in the **Low** state shall be at least 100 milliamperes. 3. With an external impedance of 100 kiloOhms or greater, the transition from 4 to 16 volts (and vice versa) shall be accomplished within 0.1 millisecond. 4. The **High** state impedance shall exceed 1 Megohms to 12 volts DC.	**6.4.8.1 Parallel I/O Ports**			Analysis	**Design**
749	It shall be possible to simultaneously assert all outputs within 100 microseconds of each other.	**6.4.8.1 Parallel I/O Ports**			Performance Test Analysis	**Design**
751	The LINESYNC signal is incoming in differential logic.	**Other Module Circuit Functions**			Analysis	**Design**
752	A maximum capacitive load of 100 picofarads shall be presented to the LINESYNC input signal.	**Other Module Circuit Functions**			Analysis	**Design**
753	An External WDT “Muzzle” Jumper shall be provided on the board.	**Other Module Circuit Functions**			Inspection	**Design**
755	When the jumper is missing (open), the feature shall not apply.	**Other Module Circuit Functions**		If the standard requires a jumper, why would the performance without the jumper need to be specified.	Inspection	**Design**
756	This feature is required to operate with the Type 210 Monitor Unit only.	**Other Module Circuit Functions**		Unclear as to why this is in the standard.	Analysis	**Design**
757	A WATCHDOG Circuit shall be provided.	**Other Module Circuit Functions**			Inspection	**Design**
758	The WATCHDOG Circuit shall be enabled by the FIELD I/O software at Power Up with a value of 100 milliseconds.	**Other Module Circuit Functions**			Analysis	**Design**
759	The enabled state of the WATCHDOG Circuit shall be machine readable and reported in the FI/O status byte.	**Other Module Circuit Functions**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
762	A synchronizable 1 kilohertz time reference shall be provided.	**Other Module Circuit Functions**			Inspection	**Design**
763	The synchronizable time reference shall maintain a frequency accuracy of +/-0.01% (+/-0.1 counts per second).	**Other Module Circuit Functions**			Analysis	**Design**
764	A 32-bit MILLISECOND COUNTER (MC) shall be provided for "timestamping."	**Other Module Circuit Functions**			Inspection	**Design**
765	Each 1 KHz reference interrupt shall increment the MC.	**Other Module Circuit Functions**			Analysis	**Design**
767	A LOGIC Switch shall be provided resident on the module board.	**Other Module Circuit Functions**			Inspection	**Design**
768	The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S.	**Other Module Circuit Functions**			Inspection	**Design**
769	The purpose of the switch is to prevent multiple use of SP3.	**Other Module Circuit Functions**			Analysis	**Design**
770	An LED shall be provided on the module front panel labeled "SP3 ON".	**Other Module Circuit Functions**			Inspection	**Design**
772	The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements.	**6.4.8.2 Serial Communications Circuitry**		Is this a specific standard that we can find?	Analysis	**Design**
773	All signal lines shall be isolated.	**6.4.8.2 Serial Communications Circuitry**			Inspection	**Design**
774	HAR 1 Harness shall be 17 lines minimum with a C12P Connector on one end and soldered with strain relief on the other.	**6.4.8.2 Serial Communications Circuitry**			Inspection	**Design**
775	In addition to the Controller interface, the EIA-485 Signal lines shall be routed to EX1 Connector.	**6.4.8.2 Serial Communications Circuitry**			Inspection	**Design**
776	All necessary driver/receiver and isolation circuitry shall be provided.	**6.4.8.2 Serial Communications Circuitry**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
777	~~System Serial Port 5 (SP5) EIA-485 signal lines shall enter the I/O Module and be split into two multi-drop isolated ports.~~	**6.4.8.2 Serial Communications Circuitry**		Are these the requirements that change given the exception? Not clear!	Analysis	**Design**
778	~~One [serial port line of SP5] shall be routed to the FCU and the other converted to EIA-485, then routed to Connector C12S.~~	**6.4.8.2 Serial Communications Circuitry**		Are these the requirements that change given the exception? Not clear!	Inspection	**Design**
779	~~System Serial Port 3 (SP3) EIA-485 signal lines shall enter the I/O module and be isolated, converted back to EIA-485 and then routed to connector C12S.~~	**6.4.8.2 Serial Communications Circuitry**		Are these the requirements that change given the exception? Not clear!	Inspection	**Design**
780	LINE SYNC and POWER DOWN lines shall be split and isolated, one routed to the FCU for shut down functions and the other changed to EIA-485; then routed to connector C12S for external module use.	**6.4.8.2 Serial Communications Circuitry**			Inspection	**Design**
781	CPU RESET and POWER UP (SYSRESET) lines shall be isolated and "OR'd" to form NRESET.	**6.4.8.2 Serial Communications Circuitry**			Inspection	**Design**
782	NRESET shall be used to reset FCU and other module devices.	**6.4.8.2 Serial Communications Circuitry**			Analysis	**Design**
783	NRESET shall also be converted to EIA-485 then routed to connector C12S.	**6.4.8.2 Serial Communications Circuitry**			Inspection	**Design**
784	If the Type 2070 module is a –2B, then routing to FCU doesn't apply.	**6.4.8.2 Serial Communications Circuitry**		Unclear as to why this is in the standard.	Analysis	**Design**
785	Isolation is between internal +5 VDC / Ground #1 and +12 VDC ISO / VDC Ground #2.	**6.4.8.2 Serial Communications Circuitry**			Analysis	**Design**
786	+12 VDC ISO is for board power and external logic.	**6.4.8.2 Serial Communications Circuitry**		Unclear as to why this is in the standard.	Analysis	**Design**
787	A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries.	**Buffers**			Analysis	**Design**
789	There shall be two entry types (in the Transition Buffer): Transition and Rollover.	**Buffers**			Analysis	**Design**
790	The inputs (to the Transition Buffer) shall be monitored for state transition.	**Buffers**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>792</td><td>The MC shall be monitored for rollover.</td><td>Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>793</td><td>At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer.</td><td>Buffers</td><td></td><td>In order to test this, one needs to know what causes a roll-over and be able to create on during testing.</td><td>Performance Test</td><td>Design</td></tr>
<tr><td>794</td><td>For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry.</td><td>Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>797</td><td>The entry types are depicted as follows:
Input Transition Entry
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>Transition Entry Identifier</td><td>S</td><td colspan="7">Input Number</td><td>1</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>2</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td></tr>
</table>
Millisecond Counter Rollover Entry
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>Rollover Entry Identifier</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>2</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td></tr>
</table></td><td>Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>798</td><td>I/O Functions</td><td></td><td></td><td></td><td></td><td>Design</td></tr>
<tr><td>799</td><td>Input scanning shall begin at I0 (bit 0) and proceed to the highest numbered input, ascending from LSB to MSB.</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>801</td><td>Once sampled, the logic state of an input shall be held until the next input scan.</td><td>I/O Functions</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>802</td><td>Each input shall be sampled 1,000 times per second.</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>803</td><td>The time interval between samples shall be 1 millisecond (+/-100 microseconds).</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>806</td><td>The Millisecond Counter shall be sampled within 10 microseconds of the completion of the input scan.</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>807</td><td>If configured, the inputs shall be filtered by the FCU to remove signal bounce.</td><td>I/O Functions</td><td></td><td>What does “if configured” mean in this context? Why would the inputs not be configured?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>808</td><td>The filtered input signals shall then be monitored for changes as noted.</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
809	The filtering parameters for each input shall consist of Ignore Input Flag and the ON and OFF filter samples.	**I/O Functions**			Analysis	**Design**
810	If the Ignore Input flag is set, no input transitions shall be recorded.	**I/O Functions**			Analysis	**Design**
811	The ON and OFF filter samples shall determine the number of consecutive samples an input must be ON and OFF, respectively, before a change of state is recognized.	**I/O Functions**			Analysis	**Design**
812	If the change of state is shorter than the specified value, the change of state shall be ignored.	**I/O Functions**			Analysis Performance Test	**Design**
813	The ON and OFF filter values shall be in the range of 0 to 255.	**I/O Functions**			Analysis	**Design**
814	A filter value of 0, for either or both values, shall result in no filtering for this input.	**I/O Functions**			Analysis	**Design**
815	The default values for input signals after reset shall be as follows: *Input Signals* — *Default Value* Filtering — Enabled On and off filter values shall be set to — 5 Transition monitoring — Disabled (Timestamps are not logged)	**I/O Functions**			Inspection	**Design**
816	Simultaneous assertion of all outputs shall occur within 100 microseconds.	**I/O Functions**			Analysis Performance Test	**Design**
817	Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC.	**I/O Functions**			Analysis	**Design**
818	The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module.	**I/O Functions**			Analysis	**Design**
819	If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the FI/O status byte shall be updated to reflect the loss of communication from the CPU Module.	**I/O Functions**			Analysis Performance Test	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>820</td><td>The data and control bits in the CPU Module-FI/O frame protocol shall control each output as follows:
Output Bit Translation
<table>
<tr><th>Case</th><th>Output Data Bit</th><th>Output Control Bit</th><th>Function</th></tr>
<tr><td>A</td><td>0</td><td>0</td><td>Output in the OFF state</td></tr>
<tr><td>B</td><td>1</td><td>1</td><td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.</td></tr>
<tr><td>C</td><td>0</td><td>1</td><td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF</td></tr>
<tr><td>D</td><td>1</td><td>0</td><td>Output is in the ON state.</td></tr>
</table></td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>824</td><td>All outputs shall never change state unless configured to do so.</td><td>I/O Functions</td><td></td><td>“Never” is very, very difficult to test.</td><td>Analysis</td><td>Design</td></tr>
<tr><td>825</td><td>All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts.</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>828</td><td>LINESYNC Interrupt – This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal.</td><td>I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>829</td><td>The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 kilohertz source for 0.5 seconds (>/=60 consecutive LINESYNC interrupts).</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>830</td><td>The LINESYNC interrupt shall synchronize the 1 kilohertz time reference with the 0-1 transition of the LINESYNC signal once a second.</td><td>I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>831</td><td>A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (>/=500 consecutive millisecond interrupts).</td><td>I/O Functions</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>832</td><td>A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults.</td><td>I/O Functions</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
833	The communication server shall automatically: *For Transmission* Generate the opening and closing flags Generate the CRC value Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU Provide zero bit insertion *For Receiving* Detect the opening and closing flags Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module Strip out inserted zeros Calculate the CRC value, compare it to the received value, and generate an interrupt on an error Generate an interrupt if an abort sequence is received	**I/O Functions**			Analysis Performance Test	**Design**
834	The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission.	**I/O Functions**			Analysis	**Design**
835	The response message transmission shall begin within 4 milliseconds of the receipt of the received message.	**I/O Functions**			Analysis Performance Test	**Design**
836	The time from the receipt of message to the completion of the commanded task shall not exceed 70 milliseconds.	**I/O Functions**			Analysis Performance Test	**Design**
837	This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.	**I/O Functions**			Analysis	**Design**
838	All communication with the CPU Module shall be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 kilobits per second.	**Data Communications Protocols**			Analysis	**Design**
839	The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no FI/O response shall be transmitted.	**Data Communications Protocols**			Analysis Performance Test	**Design**
840	The amount of bytes of a command or response is dependent upon the I/O Module identification.	**Data Communications Protocols**			Analysis	**Design**
841	The frame type shall be determined by the value of the first byte of the message.	**Data Communications Protocols**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
842	The command frames type values 112-127 and associated response frame type values 240-255 are allocated to the manufacturer diagnostics.	**Data Communications Protocols**			Analysis	**Design**
843	All other frame types not called out are reserved.	**Data Communications Protocols**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>844</td><td>The command-response Frame Type values and message times shall be as follows:
Frame Types
<table>
<tr><th>Module Command</th><th>I/0 Module Response</th><th>Description</th><th>Minimum Message Time</th><th>Maximum Message Time</th></tr>
<tr><td>0-43</td><td>128-171</td><td>Reserved for NEMA TS-2</td><td></td><td></td></tr>
<tr><td>49</td><td>177</td><td>Request Module Status</td><td>250 microseconds</td><td>275 microseconds</td></tr>
<tr><td>50</td><td>178</td><td>MILLISECOND CTR. Mgmt.</td><td>222.5 microseconds</td><td>237.5 microseconds</td></tr>
<tr><td>51</td><td>179</td><td>Configure Inputs</td><td>344.5 microseconds</td><td>6.8750 milliseconds</td></tr>
<tr><td>52</td><td>180</td><td>Poll Raw Input Data</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>53</td><td>181</td><td>Poll Filtered Input Data</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>54</td><td>182</td><td>Poll Input Transition Buffer</td><td>300 microseconds</td><td>10.25 microseconds</td></tr>
<tr><td>55</td><td>183</td><td>Command Outputs</td><td>405 microseconds</td><td>410 microseconds</td></tr>
<tr><td>56</td><td>184</td><td>Reserved</td><td>340 microseconds</td><td>10.25 milliseconds</td></tr>
<tr><td>57</td><td>185</td><td>Reserved</td><td>340 microseconds</td><td>6.875 milliseconds</td></tr>
<tr><td>58</td><td>186</td><td>Configure Watchdog</td><td>222.5 microseconds</td><td>222.5 microseconds</td></tr>
<tr><td>59</td><td>187</td><td>Controller Identification</td><td>222.5 microseconds</td><td>222.5 microseconds</td></tr>
<tr><td>60</td><td>188</td><td>I/O Module Identification</td><td>222.5 microseconds</td><td>222.5 microseconds</td></tr>
<tr><td>61-62</td><td>189-190</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
<tr><td>63</td><td>191</td><td>Poll variable length raw input</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>64</td><td>192</td><td>Variable length command outputs</td><td>405 microseconds</td><td>410 microseconds</td></tr>
<tr><td>65</td><td>193</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
<tr><td>67</td><td>195</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>845</td><td>Messages 61 / 189, 62 / 190, 65 / 193, and 67 / 195 are reserved for ITS Cabinet Frame Types.</td><td>Data Communications Protocols</td><td></td><td>Software design specification.</td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>846</td><td>Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of input data bytes.</td><td>Data Communications Protocols</td><td></td><td>Software design specification.</td><td>Analysis</td><td>Design</td></tr>
<tr><td>847</td><td>Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes, plus the following output control bytes.</td><td>Data Communications Protocols</td><td></td><td>Software design specification.
Poorly worded.</td><td>Analysis</td><td>Design</td></tr>
<tr><td>848</td><td>The Command shall be used to request FI/O status information response.
Command/response frames are as follows:
Request Module Status Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 49)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Reset Status Bits</td><td>P</td><td>E</td><td>K</td><td>R</td><td>T</td><td>M</td><td>L</td><td>W</td><td>Byte 2</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td>Poorly worded. “This” command?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>849</td><td>Request Module Status Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 177)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>System Status</td><td>P</td><td>E</td><td>K</td><td>R</td><td>T</td><td>M</td><td>L</td><td>W</td><td>Byte 2</td></tr>
<tr><td>SCC Receive Error Count</td><td colspan="8">Receive Error Count</td><td>Byte 3</td></tr>
<tr><td>SCC Transmit Error Count</td><td colspan="8">Transmit Error Count</td><td>Byte 4</td></tr>
<tr><td>MC Timestamp MSB</td><td colspan="8">MC Timestamp MSB</td><td>Byte 5</td></tr>
<tr><td>MC Timestamp NMSB</td><td colspan="8">MC Timestamp NMSB</td><td>Byte 6</td></tr>
<tr><td>MC Timestamp NLSB</td><td colspan="8">MC Timestamp NLSB</td><td>Byte 7</td></tr>
<tr><td>MC Timestamp LSB</td><td colspan="8">MC Timestamp LSB</td><td>Byte 8</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>850</td><td>The response status bits are defined as follows:
P - Indicates FI/O hardware reset
E - Indicates a communications loss of greater than 2 seconds
K - Indicates the Datakey has failed or is not present
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
M - Indicates an error with the MC interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the FI/O has been reset by the Watchdog</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
851	The FI/O status byte shall be updated (set to '1') to reflect the faults noted in clause 4.3.9.2.1.	**Data Communications Protocols**			Analysis	**Design**
852	Each status bit shall only be reset (set to '0') when the corresponding bit of the Request Module Status Command is a '1'.	**Data Communications Protocols**			Analysis	**Design**
853	The Request Module Status Response shall report the current status (subsequent to reset and sampling).	**Data Communications Protocols**			Analysis	**Design**
854	The FI/O shall count the number of errored frames the FI/O Communications Processor reports.	**Data Communications Protocols**			Analysis	**Design**
855	Separate counts shall be maintained for transmit and received frames.	**Data Communications Protocols**			Analysis	**Design**
856	When an individual count rolls over (255-0), the corresponding roll-over flag shall be set.	**Data Communications Protocols**			Analysis Performance Test	**Design**
857	FI/O modules with Datakey: On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key.	**Data Communications Protocols**			Analysis	**Design**
861	The MC timestamp value shall be sampled just prior to the Request Module Status Response.	**Data Communications Protocols**			Analysis	**Design**
862	MC MANAGEMENT frame shall be used to set the value of the MC.	**Data Communications Protocols**			Analysis	**Design**
864	The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal.	**Data Communications Protocols**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th>Pass
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>865</td><td>The frames are as follows:
Millisecond Counter Management Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 50)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>New MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>New MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>New MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 4</td></tr>
<tr><td>New MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 5</td></tr>
</table>
Millisecond Counter Management Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 178)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>S</td><td>Byte 2</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>866</td><td>The Configure Inputs command frame shall be used to change input configurations.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>867</td><td>The command-response frames are as follows:
Configure Inputs Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 51)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Number of Items (n)</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>Byte 2</td></tr>
<tr><td>Item # - Byte 1</td><td>E</td><td colspan="7">Input Number</td><td>Byte 3(I-1)+3</td></tr>
<tr><td>Item # - Byte 2</td><td colspan="8">Leading edge filter (e)</td><td>Byte 3(I-1)+4</td></tr>
<tr><td>Item # - Byte 3</td><td colspan="8">Trailing edge filter (r)</td><td>Byte 3(I-1)+5</td></tr>
</table>
Configure Inputs Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 179)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>S</td><td>Byte 2</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
868	Block field definitions shall be as follows: E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled) r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled) S - return status S = '0' on completion or '1' on input error out of range	**Data Communications Protocols**			Analysis	**Design**
869	The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs.	**Data Communications Protocols**			Analysis	**Design**
870	The response frame shall contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current input status.	**Data Communications Protocols**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>871</td><td>The frames are as follows:
Poll Raw Input Data Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 52)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
</table>
Poll Raw Input Data Response (2070-2A)
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 180)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I63</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 9</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 10</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 11</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 12</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 13</td></tr>
</table>
Poll Raw Input Data Response (2070-8)
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 180)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I119</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 16</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 17</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 18</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 19</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 20</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>872</td><td>The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>873</td><td>The response frame shall contain 8 bytes (2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>874</td><td>Raw input data shall be provided in the response for inputs that are not configured for filtering.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>875</td><td>The frames are as follows:
Poll Filter Input Data Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 53)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Byte 1</td></tr>
</table>
Poll Filter Input Data Response (2070-2A)
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 180)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I63</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 9</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 10</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 11</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 12</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 13</td></tr>
</table>
Poll Filter Input Data Response (2070-8)
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 181)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I119</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 16</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 17</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 18</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 19</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 20</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>876</td><td>The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>877</td><td>The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>878</td><td>The frames are as follows:
Poll Input Transition Buffer Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 54)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Block Number</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table>
Poll Input Transition Buffer Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 182)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Block Number</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Number of Entries</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>Item #</td><td>S</td><td colspan="7">Input Number</td><td>Byte 3(I-1)+4</td></tr>
<tr><td>Item # MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+5</td></tr>
<tr><td>Item # MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+6</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C</td><td>F</td><td>E</td><td>G</td><td>Byte 3(I-1)+7</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+8</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+9</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+10</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+11</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>879</td><td>Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>882</td><td>Bit definitions are as follows:
S - Indicates the state of the input after the transition
C - Indicates the 255 transition entries limit has been exceeded
F - Indicates the transition buffer limit has been exceeded
G - Indicates the requested block number is out of monotonic increment sequence
E - Same block number requested, E is set in response</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>883</td><td>The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>889</td><td>The Block Number byte sent in the response block shall be the same as that received in the command block.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>890</td><td>Counter rollover shall be considered as a normal increment.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>892</td><td>The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>893</td><td>If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>894</td><td>If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>895</td><td>Loss of LINESYNC reference shall also be indicated in system status information.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>896</td><td>The output bytes depend upon field I/O module. These command and response frames are as follows:
Set Outputs Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 55)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Outputs O0 (lsb) to O7 (msb) Data</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Outputs O8 to O103 Data</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 14</td></tr>
<tr><td>Outputs O0 (lsb) to O7 (msb) Control</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 15</td></tr>
<tr><td>Outputs O8 to O103 Control</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 16 to 27</td></tr>
</table>
Set Outputs Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 183)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>L</td><td>E</td><td>Byte 2</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>897</td><td>The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 58)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Timeout Value</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table>
Configure Watchdog Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 186)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Y</td><td>Byte 2</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>898</td><td>The timeout value shall be in the range between 10 to 100 milliseconds.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>899</td><td>If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>900</td><td>On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>901</td><td>The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>902</td><td>This is a legacy message command / response for FI/O modules with Datakey resident.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>903</td><td>Upon command, a response frame containing the 128 bytes of the Datakey See previous sections on Request Module Status for FI/O Status Bit ‘K’ definition.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>904</td><td>If “K” bit set, only the first two bytes shall be returned.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>905</td><td>The Command and Response frames are as follows:
Controller Identification Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 59)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
</table>
Controller Identification Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 187)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>K</td><td>Byte 2</td></tr>
<tr><td>Datakey</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 130</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>906</td><td>The I/O Module Identification Command frame shall be used to request the FI/O Identification value.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>907</td><td>A response of "1" shall be returned by 2070-2A, "2" by 2070-8, "3" is reserved for NEMA TS 2 Type 1 FI/O and "32 to 40" are reserved for ITS Cabinets.</td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>908</td><td>The command and response frames are shown as follows:
Controller Identification Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(TypeNumber = 60)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
</table>
Controller Identification Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 188)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>FI/O I D byte</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table></td><td>Data Communications Protocols</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>909</td><td>An EIA-232 Serial Port shall be provided with rate selection by jumper of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 kilobits per second asynchronous and shall be connected at EX1 Connector.</td><td>6.4.9 EIA-232 Serial Port</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>910</td><td>A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the Type 2070 UNIT.</td><td>6.4.10 HAR 2 Harness</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>911</td><td>This provides two Modems or EIA-232 Interfaces with the 2070 UNIT and the outside world.</td><td>6.4.10 HAR 2 Harness</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Test Type	Requirement Type
912	FAULT and VOLTAGE MONITOR circuitry – NEMA TS1 Controller FAULT and VOLTAGE MONITOR functions (outputs to cabinet monitor) shall be provided.	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
913	Two 3-input OR gates shall be provided.	**6.4.11 Fault and Voltage Monitor**			Inspection	**Design**
914	The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24VDC) state.	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
916	A MODULE Watchdog (WDT) circuit shall monitor the output.	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
917	No state change for 2 +/- 0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2).	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
918	Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
919	The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (+/- 0.25).	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
922	The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
923	CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79).	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
924	The bit logic state "1" shall be FCU output FALSE.	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
925	CPU / FCU operation at POWER UP shall be as follows:	**6.4.11 Fault and Voltage Monitor**				**Design**
926	1. FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**
927	2. CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and responds to CPU with "E" bit reset.	**6.4.11 Fault and Voltage Monitor**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Test Type</th><th>Requirement Type</th></tr>
<tr><td>928</td><td>3. Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to “0” will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.</td><td>6.4.11 Fault and Voltage Monitor</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>929</td><td>4. If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.</td><td>6.4.11 Fault and Voltage Monitor</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>930</td><td>5. Performs items 2 & 3 above User Software.</td><td>6.4.11 Fault and Voltage Monitor</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>718</td><td><table><tr><th>Voltage</th><th>Tolerances</th><th>I Minimum</th><th>I Maximum</th></tr><tr><td>+5 VDC</td><td>+4.875 to +5.125 VDC</td><td>1.0 ampere</td><td>10.0 ampere- MODULE 2070-4A
3.5 ampere– MODULE 2070-4B</td></tr><tr><td>+12 VDC Serial</td><td>+11. 4 to +12. 6 VDC</td><td>0.1 ampere</td><td>0.5 ampere</td></tr><tr><td>-12 VDC Serial</td><td>-11. 4 to –12. 6 VDC</td><td>0.1 ampere</td><td>0.5 ampere</td></tr><tr><td>+12 VDC</td><td>+11. 4 to +12. 6 VDC</td><td>0.1 AMP</td><td>1.0 AMP</td></tr></table></td><td>6.4.4 Module Power Supply</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>727</td><td>Power Supply Transient response shall be such that peak transient not to exceed 5%.</td><td>6.4.4 Module Power Supply</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>728</td><td>The power supply shall supply 30 watts minimum for 550 milliseconds after ACFAIL going LOW.</td><td>6.4.4 Module Power Supply</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>729</td><td>The power supply shall be capable of holding up the Unit for two 500 milliseconds Power Loss periods occurring in a 1.5-second period.</td><td>6.4.4 Module Power Supply</td><td></td><td></td><td>Analysis
Performance Test</td><td>Design</td></tr>
<tr><td>741</td><td>Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 microamperes or the input voltage exceeds 16.0 VDC.</td><td>6.4.8.1 Parallel I/O Ports</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>742</td><td>Each input shall have an internal pull-up to the Isolated +24 VDC and shall not deliver greater than 20 milliamperes to a short circuit to ground.</td><td>6.4.8.1 Parallel I/O Ports</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>746</td><td>Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal.</td><td>6.4.8.1 Parallel I/O Ports</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>747</td><td>Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing.</td><td>6.4.8.1 Parallel I/O Ports</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
748	The state of all output circuits at the time of Power Up or in Power Down state shall be open (logic 0).	**6.4.8.1 Parallel I/O Ports**			Performance Test	**Design**
750	An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.	**6.4.8.1 Parallel I/O Ports**		What exactly is the definition of "glitch"? Either this word should be changed or the specification should be dropped from the standard. (Depending upon how the user of the standard used this specification.)	Performance Test	**Design**
754	With the jumper in and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 milliseconds for 10 seconds or due to CPU Command.	**Other Module Circuit Functions**			Performance Test	**Design**
760	Once enabled, the watchdog timer shall not be disabled without resetting the FI/O.	**Other Module Circuit Functions**			Analysis Performance Test	**Design**
761	Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.	**Other Module Circuit Functions**			Performance Test	**Design**
766	At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit and a subsequent set output command is processed.	**Other Module Circuit Functions**			Analysis Performance Test	**Design**
771	If LED light ON, SP3 is active and available at C12S.	**Other Module Circuit Functions**		Further explanation needed.	Performance Test	**Design**
788	The Transition Buffer shall default to empty.	**Buffers**			Performance Test	**Design**
791	At each transition (if the input has been configured to report transition), a transition entry shall be added to the Transition Buffer.	**Buffers**			Performance Test	**Design**
795	Transition Buffer blocks are sent to the CPU module upon command.	**Buffers**			Performance Test	**Design**
796	Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer.	**Buffers**			Analysis	**Design**
800	Each complete input scan shall finish within 100 microseconds.	**I/O Functions**			Analysis Performance Test	**Design**
804	If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer.	**I/O Functions**			Analysis Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
805	If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing input number.	**I/O Functions**			Analysis Performance Test	**Design**
821	In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured.	**I/O Functions**			Performance Test	**Design**
822	For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 microseconds after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle.	**I/O Functions**			Analysis Performance Test	**Design**
823	In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remains ON until otherwise configured.	**I/O Functions**			Performance Test	**Design**
826	MILLISECOND Interrupt shall be activated by the 1 kilohertz reference once per millisecond.	**I/O Functions**			Analysis Performance Test	**Design**
827	An MC timestamp rollover flag set by MC rollover shall be cleared only on command.	**I/O Functions**			Analysis	**Design**
858	If absent, Status Bit “K” shall be set to '1' and no interrogation shall take place.	**Data Communications Protocols**			Performance Test	**Design**
859	If an error occurs during the interrogation, Status Bit “K” shall be set to '1'.	**Data Communications Protocols**			Performance Test	**Design**
860	FI/O modules without Datakey: Status Bit "K" shall always be set to '1'	**Data Communications Protocols**			Performance Test	**Design**
863	The 'S' bit shall return status '0' on completion.	**Data Communications Protocols**			Performance Test	**Design**
880	The FI/O shall set the 'F' bit to '1' when attempting to record a transition and the Transition Buffer is full.	**Data Communications Protocols**			Analysis	**Design**
881	While the Transition Buffer is full, all subsequent entries shall be discarded.	**Data Communications Protocols**			Analysis	**Design**
884	When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command.	**Data Communications Protocols**			Analysis	**Design**
885	If the new Block Number is the same as the previously-sent Block Number, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame.	**Data Communications Protocols**			Analysis	**Design**
886	If the new Block Number is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent.	**Data Communications Protocols**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Test Type	Requirement Type
887	If the block number is not incremented by one, the status G bit shall be set.	**Data Communications Protocols**			Analysis	**Design**
888	The block number received becomes the current number (even if out of sequence).	**Data Communications Protocols**			Analysis	**Design**
891	The Timestamp shall equal the MC value at the time the Poll Input Transition Buffer Response is generated.	**Data Communications Protocols**			Analysis	**Design**
915	The FCU Port 10, Bit 7 output shall normally change its state every 100 milliseconds.	**6.4.11 Fault and Voltage Monitor**			Performance Test	**Design**
920	If the voltage exceeds the limits, the circuit output shall generate a FALSE output (input to gates 1 and 2).	**6.4.11 Fault and Voltage Monitor**			Performance Test	**Design**
921	Normal operation shall return the output state to TRUE state.	**6.4.11 Fault and Voltage Monitor**			Performance Test	**Design**
699	The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors.	**6.4.1 Type 2070-8 Field I/O Module**			Inspection	**Procurement**
700	The Module CHASSIS shall be made of 0.06-inch minimum aluminum sheet and treated with clear chromate.	**6.4.1 Type 2070-8 Field I/O Module**		Manufacturing specification. Why is this in the standard?	Inspection	**Procurement**
701	All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel.	**6.4.1 Type 2070-8 Field I/O Module**		Manufacturing specification. Why is this in the standard?	Inspection	**Procurement**
702	The matching nuts shall be permanently captive on the mating surfaces.	**6.4.1 Type 2070-8 Field I/O Module**		Manufacturing specification. Why is this in the standard?	Inspection	**Procurement**

B.12 ITS Cabinet General Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
5	Sheet, Rod, Bar and Extruded shall be Type 1018/1020.	**3.1.6 Metals**		What performance requirement is addressed by this standard?	Inspection	**Design**
7	All cold roll steel shall be plated.	**3.1.6 Metals**			Inspection	**Design**
8	All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class l or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.	**3.1.6 Metals**		Need to dig up this specification.	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
9	All bolts, nuts, washers, screws, hinges and hinge pins shall be stainless steel unless otherwise specified.	**3.1.6 Metals**			Inspection	**Design**
10	Within the circuit of any device, module, or Printed Circuit Board (PCB), electrical isolation shall be provided between DC logic ground, equipment ground and the AC- conductor.	**3.1.6 Metals**			Inspection	**Design**
11	They [the DC logic ground and AC conductor] shall be electrically isolated from each other by 500 megohms, minimum, when tested at the input terminals with 500 VDC.	**3.1.6 Metals**			Performance Test	**Design**
12	Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards shall be mechanically secured with a minimum of four spacers/metal screws.	**3.1.6 Metals**		It is sufficient to specify that the daughter boards are mechanically secured. Specifying the number of screws is not necessary and creates a useless requirement.	Inspection	**Design**
13	Connectors shall be either Flat Cable or PCB Headers.	**3.1.6 Metals**			Inspection	**Design**
14	Components are allowed to be mounted under the daughter board.	**3.1.9 Daugher Boards**		This requirement provides no value.	**Drop from the standard.**	**Design**
15	All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:	**3.2.2 Components – General**		Manufacturing and/or supply chain specification. What performance requirement is addressed by this standard?	Inspection	**Design**
16	When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.	**3.2.2 Components – General**		This is a procurement requirement and has nothing to do with a design standard.	**Drop from the standard.**	**Design**
17	The electronic circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.	**3.2.2 Components – General**			Inspection	**Design**
18	No device shall be socket mounted unless specifically called out.	**3.2.2 Components – Electronic**			Inspection	**Design**
19	No component shall be operated above 80% of its maximum rated voltage, current or power ratings.	**3.2.2 Components – Electronic**		~~This is a procurement requirement and has nothing to do with the design of the cabinet~~.	Analysis	**Design**
20	Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.	**3.2.2 Components – Electronic**			Analysis	**Design**
21	No component shall be provided where the manufactured date is three years older than the contract award date.	**3.2.2 Components – Electronic**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
22	The design life of all components, operating for twenty-four hours a day and operating in their circuit application, shall be ten years or longer.	**3.2.2 Components – Electronic**			Analysis	**Design**
24	Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.	**3.2.2 Components – Electronic**		How is the possibility for damage by shock or vibration quantified?	Inspection	**Design**
26	The Manufacturer shall certify that the component application meets the requirements of this standard.	**3.2.2 Components – Electronic**		Procurement requirement.	Analysis	**Design**
27	The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150%.	**3.2.3 Capacitors**			Analysis	**Design**
28	Capacitor encasements shall be resistant to cracking, peeling and discoloration.	**3.2.3 Capacitors**		What does this mean and how is it verified?	Inspection	**Design**
29	All capacitors shall be insulated and shall be marked with their capacitance values and working voltages.	**3.2.3 Capacitors**			Inspection	**Design**
30	Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.	**3.2.3 Capacitors**			Inspection	**Design**
31	Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements.	**3.2.4 Potentiometers**		Need to dig up this specification.	Analysis	**Design**
36	Resistance values shall be indicated by the EIA color codes, or stamped value.	**3.2.5 Resistors**			Inspection	**Design**
38	Special ventilation or heat sinking shall be provided for all 2-watt or greater resistors.	**3.2.5 Resistors**			Inspection	**Design**
39	They [all resistors] shall be insulated from the PCB.	**3.2.5 Resistors**			Inspection	**Design**
40	All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable.	**3.2.6 Semiconductor Devices**		Need to dig up this specification.	Inspection	**Design**
41	All metal oxide semiconductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.	**3.2.6 Semiconductor Devices**			Inspection	**Design**
42	Device pin "1" locations shall be properly marked on the PCB adjacent to the pin.	**3.2.6 Semiconductor Devices**			Inspection	**Design**
44	All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.	**3.2.7 Transformers and Inductors**		Need to dig up this specification.	Inspection	**Design**
45	Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with thermal conductive compound or material, in addition to being mechanically secured.	**3.2.8 Triacs**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
47	The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the ampere rating shall be visible from the front of the breaker.	**3.2.9 Circuit Breakers**			Inspection	**Design**
49	Overload tripping shall not be influenced by an ambient air temperature range of from -18 degrees C to 50 degrees C.	**3.2.9 Circuit Breakers**			Performance Test	**Design**
50	The minimum Interrupting Capacity shall be 5,000 amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity.	**3.2.9 Circuit Breakers**			Performance Test	**Design**
51	For circuit breakers 80 amperes and above, the minimum interrupting capacity shall be 10,000 amperes, RMS.	**3.2.9 Circuit Breakers**			Performance Test	**Design**
52	Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carlingswitch Time Delay Curve #24 or equal).	**3.2.9 Circuit Breakers**		Need to dig up this specification.	Analysis	**Design**
53	The Load Circuit Breakers located on the PDA that are used to control Output Assembly Model 200 Switch Packs shall have auxiliary switches.	**3.2.9 Circuit Breakers**			Inspection	**Design**
54	The auxiliary switches shall “open” when the load breaker has tripped and the system will transfer the power from the Main Contactor to the Flash or Blank condition.	**3.2.9 Circuit Breakers**			Performance Test	**Design**
55	All Fuses that are resident in a bayonet style fuse holder shall have the fuse size rating labeled on the holder or on the panel adjacent to the holder.	**3.2.10 Fuses**			Inspection	**Design**
56	Fuses shall be easily accessible and removable without use of tools.	**3.2.10 Fuses**		Words such as, “easily accessible” are not of value in a standard, since they can neither be defined nor measured.	Inspection	**Design**
57	Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 milliamperes, 30 VDC.	**3.2.11 Switches**			Inspection	**Design**
59	The contacts shall be gold over brass.	**3.2.11 Switches**			Inspection	**Design**
60	The switch contacts shall be rated for a minimum of 1 ampere resistive load at 120 VAC and shall be silver over brass (or equal).	**3.2.11 Switches**			Inspection	**Design**
61	The switch shall be rated for a minimum of 40,000 operations.	**3.2.11 Switches**			Inspection	**Design**
63	The switch shall be rated for a minimum of 40,000 operations.	**3.2.11 Switches**			Inspection	**Design**
67	Screw size [for the terminal blocks] is called out under the associated file, panel or assembly.	**3.2.12 Terminal Blocks**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
68	Provided the connectors mate, screw lug cam driven devices or crimp pin connectors shall be allowable if the interface is part of a harness.	**3.2.13 Screw Lug and Cam Driven Connectors**			Inspection	**Design**
69	For field termination, screw lug and cam driven assemblies are interchangeable for field wiring termination, provided they both accommodate 22-gauge wire on the inputs and 22-gauge wire on the outputs.	**3.2.13 Screw Lug and Cam Driven Connectors**		Is specifying an exact gauge of wire appropriate? Maybe 22-gauge wire is a minimum size. Can the 22-gauge specification be expressed in terms of performance?	Inspection	**Design**
70	Harnesses shall be neat, firm and properly bundled with external protection.	**3.2.14 Wiring, Cabling, and Harnesses**		Words like "neat" have no value in a standard and are both untestable and undefined.	Inspection	**Design**
71	They shall be tie-wrapped and routed to minimize crosstalk and electrical interference.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
72	Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
74	Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
75	Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
76	Wiring shall be routed to prevent conductors from being in contact with metal edges.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
77	Wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Design**
82	Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.	**3.2.14 Wiring, Cabling, and Harnesses**		Why is insulation less than 15 mils allowed? Need to dig up this specification.	Inspection	**Design**
84	All indicators and character displays shall be readily visible at a radius of up to 4 feet within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 footcandles) of white light with the light source at 45 degrees (+/-2 degrees) to the front panel.	**3.2.15 Indicators and Character Displays**			Inspection	**Design**
85	All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted.	**3.2.15 Indicators and Character Displays**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
86	All indicators shall be self-luminous.	**3.2.15 Indicators and Character Displays**			Inspection	**Design**
87	All indicators shall have a rated life of 100,000 hours minimum.	**3.2.15 Indicators and Character Displays**			Inspection	**Design**
89	Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance shall be provided.	**3.2.15 Indicators and Character Displays**			Inspection	**Design**
90	Liquid Crystal Displays (LCD) shall be readable at temperatures of -20 degrees C to +70 degrees C.	**3.2.15 Indicators and Character Displays**			Performance Test	**Design**
93	Type T connector shall be a single row, 10 position, feed through terminal block.	**3.2.16 Connectors**			Inspection	**Design**
94	The terminal block shall be a barrier type with 6-32, 0.25 inches or longer, nickel plated brass binder head screws.	**3.2.16 Connectors**			Inspection	**Design**
95	Each terminal shall be permanently identified as to its function.	**3.2.16 Connectors**			Inspection	**Design**
96	Pin and socket contacts for connectors shall be beryllium copper construction subplated with 1.27 microns nickel and plated with 0.76 microns gold.	**3.2.16 Connectors**			Inspection	**Design**
97	Pin diameter shall be 0.0618 inches.	**3.2.16 Connectors**			Inspection	**Design**
98	All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.	**3.2.16 Connectors**		Are they actually specifying a particular tool to be used for assembly? This is an assembly procedure not a design requirement. Why is a specific tool specified?	Inspection	**Design**
99	Edge connectors shall have bifurcated gold-plated contacts.	**3.2.16 Connectors**			Inspection	**Design**
100	The PCB receptacle connector shall meet or exceed the following: Operating Voltage: 600 VAC (RMS) Current Rating: 5.0 Amperes Insulation Material: Diallyl Phthalate or Thermoplastic Insulation Resistance: 5,000 Megohms Contact Material: Copper alloy plated with 0.00005 inches of nickel and 0.000010 inches of gold Contact Resistance: 0.006 Ohm maximum	**3.2.16 Connectors**			Performance Test	**Design**
101	The two-piece PCB connector shall meet or exceed the DIN 41612.	**3.2.16 Connectors**		Need to dig up this specification.	Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
102	The PCB 22/44 Connector shall have 22 independent contacts per side; dual sided with 0.156 inch contact centers.	**3.2.16 Connectors**			Inspection	**Design**
103	Each wire terminal shall be solder-less with PVC insulation and a heavy duty short-locking spade type connector.	**3.2.16 Connectors**		~~The type of crimping tool is an assembly procedure, not a design requirement~~.	Inspection	**Design**
104	All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.	**3.2.16 Connectors**		The crimping tool is specified due to the likelihood that improper crimps will result in poor connections. It could possibly be specified in a more direct manner.	Inspection	**Design**
105	Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 0.00015 inches of gold over 0.00005 inches of nickel; and shall have a current rating of 1 Ampere minimum and an insulation resistance of 5 Megohms minimum.	**3.2.16 Connectors**			Inspection Performance Test	**Design**
106	Each PCB header socket block shall be 0.025 inches square by 0.3425 inches high from the plane of the PCB to the end of the pin; shall be mounted on 0.10 inch centers; and shall be tempered hard brass plated with 0.00015 inches of gold over 0.00005 inches of nickel.	**3.2.16 Connectors**			Inspection	**Design**
107	Each PCB header socket contact shall be nylon or diallyl phthalate.	**3.2.16 Connectors**			Inspection	**Design**
108	Each PCB header socket contact shall be removable, but crimp-connected to its conductor.	**3.2.16 Connectors**			Inspection	**Design**
109	The Manufacturer shall list the part number of the extraction tool recommended by its manufacturer.	**3.2.16 Connectors**			Inspection	**Design**
110	Each PCB header socket contact shall be brass or phosphor bronze plated with 0.0010 inches of gold over 0.00005 inches of nickel.	**3.2.16 Connectors**			Inspection	**Design**
113	Assemblies shall be provided with two guides for each plug-in PCB or associated device (except relays).	**3.3.1 Assemblies**			Inspection	**Design**
114	The guides shall extend to within 0.75 inches from the face of either the socket or connector and front edge of the assembly.	**3.3.1 Assemblies**			Inspection	**Design**
115	If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.	**3.3.1 Assemblies**			Inspection	**Design**
116	All screw type fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.	**3.3.2 Locking Devices**			Inspection	**Design**
119	The manufacturer's model number and circuit issue or revision number shall appear on the rear panel of all equipment supplied (where such panel exists).	**3.3.4 Model and Serial Numbers**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
120	In addition to any assignment of model numbers by the manufacturer, the TYPE number shall be displayed on the front panel in bold type, at least 0.25 inches high.	**3.3.4 Model and Serial Numbers**			Inspection	**Design**
121	A permanent label shall be affixed to the inside near and center floor of the Type 2070 unit chassis when viewed from the front. The label shall display the unit's serial number. The number shall be permanent and easy to read.	**3.3.4 Model and Serial Numbers**		Words like "easy to read" are undefined and as such, untestable.	Inspection	**Design**
122	Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.	**3.3.5 Workmanship**			**Drop from the standard.**	**Design**
123	The following tolerances shall apply, except as specifically shown on the plans or in these specifications: *TYPE* *DIMENSIONAL TOLERANCE* Sheet Metal +/-0.0525 inch PCB +0 inch, - 0.010 inch Edge Guides +/-0.015 inch *Note: These dimensional tolerances do not apply to material gauge or thickness.	**3.3.5 Tolerances**			Inspection	**Design**
126	PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors.	**3.4.1 Human Engineering**		As a standard requirement, this first phrase is worthless.	Inspection	**Design**
127	PCBs shall require a force no less than 5 pounds-force or greater than 50 pounds-force for insertion or removal.	**3.4.1 Human Engineering**			Inspection	**Design**
128	The design shall be inherently temperature compensated to prevent abnormal operation.	**3.4.2 Design Engineering**		What does "inherently temperature compensated" mean? I think their try to refer to using natural convection for cooling rather than using a fan since a fan is not fail-safe. The standard should say that more clearly.	Analysis	**Design**
129	The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range.	**3.4.2 Design Engineering**		What does this specification mean?	**Drop from the standard.**	**Design**
132	No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.	**3.4.3 Generated Noise**		At what noise level does processing and communications undergo interference?	**Reword to include an actual specification.**	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
23	Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance.	**3.2.2 Components – Electronic**	P	Legacy requirements and performance needs have driven a system that is completely modular. The operational need for this requirement is clear. What is not clear is how a vendor would know they met the standard.	Inspection	**Performance**
88	Each LED indicator shall be white or clear when off. We did find on old EDI Switchpack that had red colored, and found that when under intense ambient light, it was not as easy to determine that the LED was flashing or off.	**3.2.15 Indicators and Character Displays**	P/F	The operational need is that the LED cannot look like it is "on" when lit by ambient light. As such, there must be no reflector behind it. A reflector would allow for a brighter LED with the same current, but it is important that only LEDs that are powered appear to be on.	Inspection	**Performance**
91	Connectors shall be keyed to prevent improper insertion of the wrong connector where equipment damage or operator injury may result. **Note**: We found SIU that were identical in function from two different vendors, and took pictures, showing that they were labeled with bogus numbers.	**3.2.16 Connectors**	P	The operational need is to make sure that different devices will not go into slots designed for other devices. The standard has drawings showing where the connectors should be placed.	Inspection	**Performance**
92	The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).	**3.2.16 Connectors**	P/F	DB25 is not keyed, but plugging in the wrong plug won't break anything.	Inspection	**Performance**
131	No item, component or subassembly shall emit an audible noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted.	**3.4.3 Generated Noise**	P	Dave Miller has a certification procedure showing the noise test and will provide those results. Furthermore, Dave Miller had his noise meter shipped to the HCTX site and we verified this requirement directly.	Performance Test	**Performance**
1	All sharp edges and corners shall be rounded and free of any burrs.	**3.1.6 Metals**			Inspection	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
2	Aluminum sheets shall be Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy.	**3.1.6 Metals**		This appears to be a manufacturing or manufacturer specification. What specific, measurable, performance standard is met by using a particular thickness or type of material?	Inspection	**Procurement**
3	Rod, Bar and Extruded shall be Type 6061-T6, or equal.	**3.1.6 Metals**		Same comment as above.	Inspection	**Procurement**
4	Sheet shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.	**3.1.6 Metals**			Inspection	**Procurement**
6	Cold Rolled Steel sheet, rod, bar and extruded shall be Type 1018/1020.	**3.1.6 Metals**			Inspection	**Procurement**
25	The Manufacturer shall submit detailed engineering technical data on all components at the request of the AGENCY.	**3.2.2 Components – Electronic**		This specifies a documentation task for the manufacturer that has no affect on the cabinet design.	Analysis	**Procurement**
32	Potentiometers with ratings less than one-watt shall be used only for trimmer type functions.	**3.2.4 Potentiometers**			Inspection	**Procurement**
33	The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.	**3.2.4 Potentiometers**			Analysis	**Procurement**
34	Fixed carbon film, deposited carbon, or composition insulated resistors shall conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684.	**3.2.5 Resistors**		Need to dig up this specification.	Inspection	**Procurement**
35	All resistors shall be insulated and shall be marked with their resistance values.	**3.2.5 Resistors**			Inspection	**Procurement**
37	The value of the resistors shall not vary by more than 5% between -37 degrees C and 74 degrees C.	**3.2.5 Resistors**			Analysis	**Procurement**
43	All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination.	**3.2.7 Transformers and Inductors**			Inspection	**Procurement**
46	Circuit breakers shall be listed by UL or ETL.	**3.2.9 Circuit Breakers**			Inspection	**Procurement**
48	Contacts shall be silver alloy and enclosed in an arc quenching chamber.	**3.2.9 Circuit Breakers**			Inspection	**Procurement**
58	The switch contact resistance shall be 100 milliohms maximum at 2 milliamperes, 30 VDC.	**3.2.11 Switches**			Performance Test	**Procurement**
62	The switch contacts shall be rated for a minimum of 5 amperes resistive load at 120 VAC or 28 VDC and shall be silver over brass (or equal).	**3.2.11 Switches**			Inspection	**Procurement**
64	Ratings shall be the same as CONTROL, except the contact rating shall be a minimum of 10 amperes at 125 VAC.	**3.2.11 Switches**			Inspection	**Procurement**
65	The terminal blocks shall be barrier type, rated at 20 amperes and 600 VAC RMS minimum.	**3.2.12 Terminal Blocks**			Inspection	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
66	The terminal screws shall be 0.3125 inches minimum length nickel plated brass binder head type with screw inserts of the same material.	**3.2.12 Terminal Blocks**			Inspection	**Procurement**
73	Conductors within an encased harness have no color requirements.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Procurement**
78	All conductors, except those that can be readily traced, shall be labeled.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Procurement**
79	Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Procurement**
80	All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper.	**3.2.14 Wiring, Cabling, and Harnesses**		Need to dig up this specification.	Inspection	**Procurement**
81	The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater.	**3.2.14 Wiring, Cabling, and Harnesses**			Inspection	**Procurement**
83	Conductor color identification shall be as follows: AC- circuits – white Equip. Ground – solid green or continuous green color with 1 or more yellow stripes. DC logic ground – continuous white with a red stripe. AC+ circuits – continuous black or black with colored stripe. DC logic ungrounded or signal – any color not specified.	**3.2.14 Wiring, Cabling, and Harnesses**		Is this an industry recognized color codes scheme or just something someone made up? Need to find the source of these color codes.	Inspection	**Procurement**
111	The surge suppression device shall comply with ANSI/IEEE C62.41 (100 Kilohertz Ring Wave, the 1.2/50 microseconds – 8/20 Combination Wave and the EFT Burst) at voltages and currents specified at "Location Category B2" and at "Test Severity" level III (i.e. up to 4.0 Kilovolts, open-circuit).	**3.2.17 Surge Protection Device**		Need to dig up this specification.	Inspection	**Procurement**
112	All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs.	**3.3.1 Assemblies**		Words like, "easily replaceable" are undefined and as such, un-testable.	Inspection	**Procurement**
117	No components, traces, brackets or obstructions shall be within 0.125 inches of the board edge (guide edges).	**3.3.3 PCB Design and Connectors**			Inspection	**Procurement**
118	The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs.	**3.3.3 PCB Design and Connectors**			Inspection	**Procurement**
124	The equipment shall be engineered for simplicity, ease of operation and maintenance.	**3.4.1 Human Engineering**			**Drop from the standard.**	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
125	Knobs shall be a minimum of 0.5 inches in diameter and a minimum separation of 0.5 inches edge to edge.	**3.4.1 Human Engineering**			Inspection	**Procurement**
130	The design shall take into consideration the protection of personnel from all dangerous voltages.	**3.4.2 Design Engineering**		What does "take into consideration" actually mean and how is it assessed?	**Drop from the standard.**	**Procurement**

B.13 ITS Cabinet PCBoard Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
133	All contacts on PCBs shall be plated with a minimum thickness of 0.00003 inches gold over a minimum thickness of 0.000075 inches nickel.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
134	PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Performance Test	**Design**
136	NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0625 inches minimum thickness shall be used.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
137	Inter-component wiring shall be by laminated copper clad track having a minimum weight of 0.2 ounces per square foot with adequate cross section for current to be carried.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
138	All copper tracks shall be plated or soldered to provide complete coverage of all exposed copper tracks.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
139	Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
140	All PCBs shall conform to Section 3.3 of Military Specification MIL-P-13949G. Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better.	**3.5.1 PCB – Design, Fabrication, and Mounting**		Need to dig up this specification.	Inspection	**Design**
141	The class of permissible bow or twist shall be Class C (Table V) or better.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
142	The class of permissible warp or twist shall be Class A (Table II) or better.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
143	Sections 4.2 through 6.6 of Military Specification MIL-P-13949G (inclusive) shall be omitted except as referenced in previous sections of this specification.	**3.5.1 PCB – Design, Fabrication, and Mounting**		Need to dig up this specification.	Inspection	**Design**
144	The mounting of parts and assemblies on the PCB shall conform to Military Specification MIL-STD-275E, except as follows:	**3.5.1 PCB – Design, Fabrication, and Mounting**		Need to dig up this specification.	Inspection	**Design**
145	Semiconductor devices that dissipate more than 250 milliwatts or cause a temperature rise of 10 degrees C or more shall be mounted with spacers, transipads or heat sinks to prevent contact with the PCB.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Analysis	**Design**
146	When completed, all residual flux shall be removed from the PCB.	**3.5.1 PCB – Design, Fabrication, and Mounting**		This is okay, but should be worded differently. This reads like a manufacturing step. Maybe it should just say that the PCB shall be free of all residual flux.	Inspection	**Design**
147	The resistance between any two isolated, independent conductor paths shall be at least 100 Megohms when a 500 VDC potential is applied.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Performance Test	**Design**
148	All PCBs shall be coated with a moisture resistant coating.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
149	Where less than 0.25 inches lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.0625 inches (+/-0.0005 inches) Thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
150	Each PCB connector edge shall be chamfered at 30 degrees from board side planes.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
151	The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
152	The key slots shall be 0.045 inches (+/- 0.005 inches) for 0.1 inches spacing and 0.055 inches (+/- 0.005 inches) for 0.156 inches spacing.	**3.5.1 PCB – Design, Fabrication, and Mounting**			Inspection	**Design**
153	Hand soldering shall comply with Military Specification MIL-STD-2000.	**3.5.2 PCB – Soldering**		Need to dig up this specification.	Inspection	**Design**
154	Automatic flow soldering shall be a constant speed conveyor system with the conveyor speed set at optimum to minimize solder peaks or points.	**3.5.2 PCB – Soldering**		This is a manufacturing process requirement rather than a design requirement. The soldering process is specified due to the likelihood that poor solder points will result in poor connections. It could possibly be specified in a more direct manner. The quality of the solder points is not directly testable. As such, determining if this standard has been met becomes an exercise in verifying the performance of the board supplier. Is the quality of the vendor an item for a standard?	Inspection	**Design**
155	Temperature shall be controlled to within +/- 8 degrees C of the optimum temperature.	**3.5.2 PCB – Soldering**			Inspection	**Design**
156	The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process.	**3.5.2 PCB – Soldering**			Inspection	**Design**
157	Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.	**3.5.2 PCB – Soldering**			Inspection	**Design**
158	If exposure to the temperature bath is of such a time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.	**3.5.2 PCB – Soldering**		This is a manufacturing process requirement rather than a design requirement.	Inspection	**Design**
159	Definitions for the purpose of this section on PCBs shall be taken from MIL-P-55110D Section 3.3 and any current addendum.	**3.5.3 PCB – Definitions**		Need to dig up this specification.	Inspection	**Design**
160	Jumpers are not allowed unless called out in the specifications or approved by the AGENCY.	**3.5.4 PCB – Jumpers**			**Drop from the standard.**	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
135	Fabrication of PCBs shall be in compliance with Military Specification MIL-P-13949, except as follows:	**3.5.1 PCB – Design, Fabrication, and Mounting**		Need to dig up this specification.	Inspection	**Procurement**

B.14 ITS Cabinet Models 200 and 204 Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
161	The unit chassis shall be made of metal suitable to meet rigid support and environmental requirements.	**4.1.1 Models 200 and 204 General**		This requirement could refer to road-side constraints, but it still seems odd.	Inspection	**Design**
162	Where electrical isolation is the only requirement, plastic insulation material may be used in lieu of metal.	**4.1.1 Models 200 and 204 General**			Analysis Inspection	**Design**
163	The unit control circuitry and switches shall be readily accessible by the use of a screwdriver or wrench.	**4.1.1 Models 200 and 204 General**			Inspection	**Design**
165	The unit shall be constructed so that no live voltage is exposed.	**4.1.1 Models 200 and 204 General**			Inspection	**Design**
166	A handle shall be attached to the front panel for insertion or removal from the unit mating connector.	**4.1.1 Models 200 and 204 General**			Inspection	**Design**
167	The unit shall be so constructed that its lower surface shall be no more than 2.06 inches below the centerline of the connector and no part shall extend more than 0.9 inches to the left or 1.1 inches to the right of the connector centerline.	**4.1.1 Models 200 and 204 General**			Inspection	**Design**
168	Continuous edge guides shall be provided on the unit.	**4.1.1 Models 200 and 204 General**			Inspection	**Design**
169	Each switch shall be capable of switching any current from 0.050 Amperes to 10.0 Amperes (AC) load with power factor of 0.85 or higher.	**4.1.1 Models 200 and 204 General**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
164	Only one type of screw head end (Slotted or Phillips) shall be used.	**4.1.1 Models 200 and 204 General**	F	The operational need is to avoid a maintenance person having to go back to his vehicle, but communications ports *only* come with slotted screws. As a result, the cabinet already has a mix of screw types and must.	Inspection	**Performance**
170	Unit indicators shall be vertically centered on the front panel with indicators positioned no more than one inch from said center. **Note**: The front panels are not shown in the standard and, as a result, the different vendors do not follow a consistent labeling criterion, that is, some switchpacks show "flasher" versus "signal" and do not have consistent numbering schemes.	**4.1.1 Models 200 and 204 General**	P	The operational need is to maintain a similar look and feel. There is no drawing of the front, yet three different vendors accomplished the task in a very similar way, meeting the standard.	Inspection	**Performance**
171	Model plug connectors shall be: Model 200 BEAU P 5412 – LAB or approved equal	**4.1.2 Model Plug Connectors**			Inspection	**Procurement**

B.15 ITS Cabinet Model 200 Switch Pack Unit Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
172	The Model 200 Switch Pack Unit shall be a modular plug-in device containing three solid-state switches.	**4.2.1 General**			Inspection	**Design**
173	Each switch shall open or close a connection between applied power and external load.	**4.2.1 General**			Inspection	**Design**
174	A Ground True Controller Unit Input (0 VDC to 6 VDC) shall cause the switch to conduct (ON) and a Ground False (16 VDC or more) shall cause it to not conduct (OFF), State transition shall occur between 6 VDC and 16 VDC.	**4.2.1 General**			Inspection	**Design**
175	The input shall not sink more than 20 milliamperes or be subjected to more than 30 VDC. The input shall have reverse polarity protection.	**4.2.1 General**			Inspection	**Design**
177	Each switch shall have an OFF state dv/dt rating of 100 Volts per microsecond or better.	**4.2.1 General**			Inspection	**Design**
178	Each switch shall provide isolation between inputs and outputs of at least 2000 Vdc and at least 100 megaohms resistive.	**4.2.1 General**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
182	The resistance between the AC+ input terminal and the AC+ output terminal of each switch shall be a minimum of 15K Ohms when the switch is in open (OFF) state.	**4.2.1 General**			Performance Test	**Design**
183	When the switch is in the OFF state, the output current through the load shall not exceed 10 milliamperes peak.	**4.2.1 General**			Performance Test	**Design**
176	With all switches ON, the unit shall not draw more than 60 milliamperes at +16 VDC or more from the +24 VDC cabinet power supply.	**4.2.1 General**		The operational need is that the switchpack does not draw too much current.	Performance Test	**Performance**
179	The unit front panel shall have an indicator on the input to each switch.	**4.2.1 General**	P		Inspection	**Performance**
180	The indicator shall be labeled or color-coded “Red”-top switch, “Yellow”-middle switch, and “Green”-bottom switch.	4.2.1 General	P		Inspection	**Performance**
181	The middle switch indicator shall be vertically centered on the unit front panel with the other indicators positioned one inch above and below.	**4.2.1 General**	F	None of the devices found had LEDs one inch apart. The Caltrans approved device had LEDs ¾ inch apart.	Inspection	**Performance**

B.16 ITS Cabinet Model 204 Flasher Unit and Model 205 Flash Transfer Unit Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
184	The FLASHER UNIT shall be a modular plug-in device containing a flasher control circuit and two solid-state switches.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Design**
185	The unit’s function is to alternatively open and close connections between applied power and external load.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Design**
186	The unit shall generate its own internal DC power from the AC Line.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Design**
188	Each switch shall have an OFF state dv/dt rating of 200 V/microsecond or better.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Design**
192	The two indicators shall be centered with one inch minimum spacing.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Design**
193	Each circuit shall be designed to operate in an open-circuit condition without load for 10 years minimum.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
194	A surge arrestor shall be provided between AC (pin 11) and Flasher Output (pins 7 & 8).	**4.3.1 Model 204 Flasher Unit**			Inspection	**Design**
195	The [surge] arrestor shall meet the following requirements: Recurrent Peak Voltage: 212 Volts Maximum Energy Rating: 50 Joules Average Power Dissipation: 0.85 Watts Peak Current for pulses less than 6 microseconds: 2000 Amperes Standby Current: less than one mA	**4.3.1 Model 204 Flasher Unit**			Performance Test	**Design**
196	Each switch shall be designed for a minimum of 100,000 (reference is a 10-year lifespan) operations while switching a tungsten load of 1000 Watts at 70 degrees C. Switch isolation between DC input and AC output circuit shall be at least 10,000 Megohms at 2000 VDC.	**4.3.2 Model 205 Flash Transfer Unit**			Analysis	**Design**
197	The Flash Transfer Relay Unit shall be of electromechanical type, designed for continuous duty.	**4.3.2 Model 205 Flash Transfer Unit**			Inspection	**Design**
198	Each unit shall be enclosed in a removable, clear plastic cover.	**4.3.2 Model 205 Flash Transfer Unit**			Inspection	**Design**
199	The manufacturer's name, electrical rating, and part number shall be placed on the cover.	**4.3.2 Model 205 Flash Transfer Unit**			Inspection	**Design**
200	They shall be durable, permanent and readily visible.	**4.3.2 Model 205 Flash Transfer Unit**		Specifications such as "readily visible" need to be quantified or omitted.	Inspection	**Design**
201	Each unit shall be provided with DPDT contacts.	**4.3.2 Model 205 Flash Transfer Unit**			Inspection	**Design**
202	The contact points shall be of fine silver, silver alloy or a superior alternate material.	**4.3.2 Model 205 Flash Transfer Unit**			Inspection	**Design**
203	Contact points and arms shall be capable of switching 20 Amperes or one Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitation.	**4.3.2 Model 205 Flash Transfer Unit**			Analysis	**Design**
204	The points and arms shall be able to withstand 10 Gs, 10 –55 Hertz without contact chatter.	**4.3.2 Model 205 Flash Transfer Unit**			Performance Test	**Design**
205	The relay coil shall have a power consumption of 10 Volt - Ampere maximum	**4.3.2 Model 205 Flash Transfer Unit**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
206	Each relay shall withstand a potential of 1500 VAC at 60 Hertz between insulated parts and between current carrying or non-carrying parts.	**4.3.2 Model 205 Flash Transfer Unit**			Analysis	**Design**
207	Each relay shall have a one cycle surge rating of 175 Amperes RMS and pickup and drop out within 20 milliseconds.	**4.3.2 Model 205 Flash Transfer Unit**			Performance Test	**Design**
187	The unit shall commence flashing operation when AC power is applied providing 50 to 60 flashes per minute per switch with a 50 % duty cycle.	**4.3.1 Model 204 Flasher Unit**	P	How long after application should flashing begin? What is the tolerance around 50% duty cycle? Tolerances are located in the glossary of the standard!	Performance Test	**Performance**
189	The resistance between the AC+ input terminal and the AC+ output terminal of each switch shall be a minimum of 15K Ohms when the switch is in open (OFF) state.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Performance**
190	When the switch is in OFF state the output current shall not exceed 10 milliamperes peak.	**4.3.1 Model 204 Flasher Unit**			Inspection	**Performance**
191	An indicator showing each switch output state shall be provided.	**4.3.1 Model 204 Flasher Unit**	P		Inspection	**Performance**

B.17 ITS Cabinet Model 212 Monitor Unit (CMU) Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
	The following indicators shall be provided (Top to Bottom):					
230	This input shall be considered active when the input voltage exceeds 89 Volts RMS.	**4.4.9 Input Signals**			Performance Test	
231	This input shall not be considered active when the input voltage is less than 70 Volts RMS.	**4.4.9 Input Signals**			Performance Test	
277	Clear LEDs shall not depend on a reflector or diffusion as part of its design.	**4.4.11 Front Panel Devices**		This verbiage actually defines "clear" LEDs.	Inspection	
208	**4.4.1 General – 4.4.6 Exit From Failed State Action**	**4.4.1 General – 4.4.6 Exit From Failed State Action**		I haven't a clue how to set these requirements up for "testing" via the standard!		**Design**
209	The CMU shall compare the active states of the field signals with the states reported by the ATC Controller Unit in the Type 61 frame.	**4.4.7 Field Output Check**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
210	When a mismatch is detected for less than 700 milliseconds the CMU shall not cause a LFSA.	**4.4.7 Field Output Check**			Performance Test	**Design**
212	When a mismatch is detected for more than 700 milliseconds but less than 1000 milliseconds, the CMU may or may not cause a LFSA.	**4.4.7 Field Output Check**		This is almost "over specified" and could be left out.	Performance Test	**Design**
214	There shall be a programming in the serial memory key to disable Field Output Check monitoring on a field input basis.	**4.4.7 Field Output Check**			Analysis	**Design**
215	The CMU shall compare the active states of the field signals with the states reported by the ATC Controller Unit in the Type 61 frame.	**4.4.7 Field Output Check**			Analysis	**Design**
216	When a mismatch is detected while a Conflict, Lack of Signal, or Multiple fault is timing, Field Check Status shall be reported with the fault to indicate the faulty channel(s) and color(s).	**4.4.7 Field Output Check**			Analysis	**Design**
217	Field Output Check monitoring shall be disabled when the MAIN CONTACTOR COIL STATUS input is not active.	**4.4.7 Field Output Check**			Analysis	**Design**
218	There shall be a programming in the serial memory key to disable Field Output Check monitoring on a field input basis.	**4.4.7 Field Output Check**			Analysis	**Design**
219	The CMU shall measure the temperature at the CMU and report this value in the Type 182 frame.	**4.4.8 CMU Temperature**			Analysis	**Design**
220	Temperature accuracy shall be +/-6 degrees C over the operating temperature range of the CMU.	**4.4.8 CMU Temperature**			Analysis	**Design**
221	A Green or Yellow signal input shall be sensed active when it exceeds 25 Volts RMS and shall not be sensed active when it is less than 15 Volts RMS.	**4.4.9 Input Signals**			Analysis	**Design**
222	A Green or Yellow signal between 15 Volts RMS and 25 Volts RMS may or may not be sensed active.	**4.4.9 Input Signals**		What does specifying that a signal may or may not be sensed active accomplish?	Analysis	**Design**
223	There shall be a programming in the serial memory key to disable the Yellow input for each physical channel.	**4.4.9 Input Signals**			Analysis	**Design**
226	A channel shall be sensed active when the load current exceeds 105% of the Channel Current Sense Threshold programmed for that channel in the serial memory key.	**4.4.9 Input Signals**			Analysis	**Design**
227	A channel shall not be sensed active when the load current is less than 95% of the Channel Current Sense Threshold programmed for that channel in the serial memory key.	**4.4.9 Input Signals**			Analysis	**Design**
228	A load current value between 95% and 105% of the Channel Current Sense Threshold may or may not be sensed active.	**4.4.9 Input Signals**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
229	This input shall be internally connected to the CMU Output Relay COM pin.	**4.4.9 Input Signals**			Inspection	**Design**
232	Signals between 89 Volts RMS and 70 Volts RMS may or may not be considered active.	**4.4.9 Input Signals**		This requirement defines "active" but the specification is not used further. If the signal can be considered either, what value is the specification?	Performance Test	**Design**
233	Operation of the cabinet in AUTO mode shall place AC+ on this input.	**4.4.9 Input Signals**			Analysis	**Design**
234	Operation of the cabinet in FLASH mode shall be open circuit on this input.	**4.4.9 Input Signals**			Analysis	**Design**
235	The CMU shall report the state of this input in the Type 189 frame.	**4.4.9 Input Signals**			Analysis	**Design**
236	The MAIN CONTACTOR COIL STATUS input shall be connected to the AC+ Raw side of the main contactor signal bus relay coil.	**4.4.9 Input Signals**			Inspection	**Design**
237	An active signal on this input indicates the Signal Bus should be powering the Switch Packs.	**4.4.9 Input Signals**			Analysis	**Design**
238	This input shall be considered active when the input voltage exceeds 89 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
239	This input shall not be considered active when the input voltage is less than 70 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
240	Signals between 89 Volts RMS and 70 Volts RMS may or may not be considered active.	**4.4.9 Input Signals**		This requirement defines "active" but the specification is not used further. If the signal can be considered either, what value is the specification?	Performance Test	**Design**
241	The CMU shall report the state of this input in the Type 189 frame.	**4.4.9 Input Signals**			Performance Test	**Design**
242	The MAIN CONTACTOR SECONDARY STATUS input shall be connected to the output side of the main contactor signal bus relay.	**4.4.9 Input Signals**			Inspection	**Design**
243	This input shall be considered active when the input voltage exceeds 89 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
244	This input shall not be considered active when the input voltage is less than 70 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
245	Signals between 89 Volts RMS and 70 Volts RMS may or may not be considered active.	**4.4.9 Input Signals**		This requirement defines "active" but the specification is not used further. If the signal can be considered either, what value is the specification?	Performance Test	**Design**
246	The CMU shall report the state of this input in the Type 189 frame.	**4.4.9 Input Signals**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
247	The FTR COIL DRIVE STATUS input shall be connected to the FTR COIL DRIVE signal in the AC SIGNAL POWER BUS.	**4.4.9 Input Signals**			Inspection	**Design**
248	This input shall be considered active when the input voltage exceeds 89 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
249	This input shall not be considered active when the input voltage is less than 70 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
250	Signals between 89 Volts RMS and 70 Volts RMS may or may not be considered active.	**4.4.9 Input Signals**			Performance Test	**Design**
251	The CMU shall report the state of this input in the Type 189 frame.	**4.4.9 Input Signals**			Analysis	**Design**
252	The CB TRIP STATUS input shall be connected to the Auxiliary Switch output of the circuit breaker unit.	**4.4.9 Input Signals**			Inspection	**Design**
253	This input shall be considered active when the input voltage exceeds 89 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
254	This input shall not be considered active when the input voltage is less than 70 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
255	Signals between 89 Volts RMS and 70 Volts RMS may or may not be considered active.	**4.4.9 Input Signals**			Performance Test	**Design**
256	The CMU shall report the state of this input in the Type 189 frame.	**4.4.9 Input Signals**			Analysis	**Design**
258	These inputs shall be considered active (door open) when the input voltage exceeds 89 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
259	These inputs shall not be considered active (door closed) when the input voltage is less than 70 Volts RMS.	**4.4.9 Input Signals**			Performance Test	**Design**
260	Signals between 89 Volts RMS and 70 Volts RMS may or may not be considered active.	**4.4.9 Input Signals**		How does this specification aid the implementer of the standard?	Performance Test	**Design**
261	The CMU shall report the state of these inputs in the Type 189 frame.	**4.4.9 Input Signals**			Analysis	**Design**
262	The MONITOR INTERLOCK input shall be connected to VDC GROUND within the CMU.	**4.4.9 Input Signals**			Inspection	**Design**
263	The Address Select input pins ADDRESS 0 and ADDRESS 1 define the Serial Bus #1 address of the CMU.	**4.4.9 Input Signals**			Inspection	**Design**
264	The pins are left open for a logical False, and are connected to VDC GROUND for a logical True.	**4.4.9 Input Signals**			Inspection	**Design**
265	*ADDRESS 1* / *ADDRESS 0* / *SB #1 Address* False / False / 0x0F False / True / 0x10 True / False / 0x11 True / True / 0x12	**4.4.9 Input Signals**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
266	The CMU shall be operational over the voltage range of 80 Volts RMS to 135 Volts RMS.	**4.4.10 Power and Circuit Requirements**			Analysis	**Design**
267	It [the CMU] shall be capable of insertion and removal while AC power is applied to the cabinet.	**4.4.10 Power and Circuit Requirements**			Performance Test	**Design**
268	Surge current on AC+ Raw shall be less than 2 Amperes peak.	**4.4.10 Power and Circuit Requirements**			Performance Test	**Design**
269	The CMU shall not use the Cabinet +24VDC Power Supply to run any of its internal circuitry.	**4.4.10 Power and Circuit Requirements**			Analysis	**Design**
270	The +24 VDC MONITOR and +12 VDC MONITOR input circuits shall be optically isolated from the AC+ Raw circuitry.	**4.4.10 Power and Circuit Requirements**			Inspection	**Design**
271	The maximum current into the +24 VDC or +12 VDC Monitor inputs over the voltage range of 0 VDC to 30 VDC shall be less than 20 milliamperes.	**4.4.10 Power and Circuit Requirements**			Performance Test	**Design**
272	The Output relay of the CMU shall have one set of isolated Form C contacts.	**4.4.10 Power and Circuit Requirements**			Inspection	**Design**
273	These relay contacts shall be rated for a minimum of three Amperes at 120 Volts RMS and 100,000 operations.	**4.4.10 Power and Circuit Requirements**			Inspection	**Design**
274	Contact opening/closing time shall be 30 milliseconds or less.	**4.4.10 Power and Circuit Requirements**			Performance Test	**Design**
275	The relay coil shall be energized in the No Fault state and de-energized in the FSA state.	**4.4.10 Power and Circuit Requirements**			Performance Test	**Design**
276	All indicators shall be clear LEDs.	**4.4.11 Front Panel Devices**			Inspection	**Design**
294	A yellow indicator shall illuminate for 40 milliseconds (+/-5 milliseconds) each time the CMU correctly receives a frame on Serial Bus #1.	**4.4.11 Front Panel Devices**			Performance Test	**Design**
295	A yellow indicator shall illuminate for 40 milliseconds (+/-5 milliseconds) each time the CMU correctly receives a frame on Serial Bus #3.	**4.4.11 Front Panel Devices**			Performance Test	**Design**
296	The Serial Bus #3 RxD+ input shall be terminated on the CMU to the Serial Bus #3 EIA-485 supply voltage through a 560 Ohm resistor.	**4.4.11 Front Panel Devices**			Inspection	**Design**
297	The Serial Bus #3 RxD- input shall be terminated on the CMU to AC Raw- through a 560 Ohm resistor.	**4.4.11 Front Panel Devices**			Inspection	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>298</td><td>A 120 Ohm resistor shall be connected on the CMU between RxD+ and RxD-.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>299</td><td>The CMU Serial Bus #3 TxD drivers shall remain in the mark state with drivers enabled when the CMU is not transmitting a command frame.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>300</td><td>Note: A 120 Ohm resistor shall be connected between TxD+ and TxD- on the Serial Bus #3 cable assembly in the last Output Assembly installed in the Serial Bus #3 daisy chain.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>301</td><td>An EIA-232-E Data Terminal Equipment (DTE) interface and connector shall be provided for interconnecting to a personal computer.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>302</td><td>Where differences occur between the EIA-232 standard and this document, this document shall govern.</td><td>4.4.11 Front Panel Devices</td><td></td><td>Need to dig up this specification.</td><td>Inspection</td><td>Design</td></tr>
<tr><td>303</td><td>The connector shall be mounted on the front panel and shall be a 9-position subminiature D-type connector with metal shell.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>304</td><td>The connector shall utilize female contacts with 15 millionths of an inch gold plating in the mating areas.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>305</td><td><table><tr><th>Pin #</th><th>Function</th><th>I/O</th></tr><tr><td>1</td><td>Reserved</td><td>-</td></tr><tr><td>2</td><td>RxD</td><td>I</td></tr><tr><td>3</td><td>TxD</td><td>O</td></tr><tr><td>4</td><td>Reserved</td><td>-</td></tr><tr><td>5</td><td>Signal Ground</td><td>-</td></tr><tr><td>6</td><td>Reserved</td><td>-</td></tr><tr><td>7</td><td>Reserved</td><td>-</td></tr><tr><td>8</td><td>Reserved</td><td>-</td></tr><tr><td>9</td><td>Reserved</td><td>-</td></tr></table></td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>306</td><td>The RxD input shall contain the serial data input to the CMU.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>307</td><td>The TxD output shall contain the serial data output from the CMU.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>308</td><td>All signals shall be referenced to Signal Ground and shall be optically isolated from the CMU.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>309</td><td>Transmission shall be in asynchronous start/stop mode.</td><td>4.4.11 Front Panel Devices</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
310	The format shall be 8 bit data, 1 stop bit, even parity, and 9600 bits per second (+/-2%) at a minimum.	**4.4.11 Front Panel Devices**			Analysis	**Design**
311	The CMU shall be capable of full duplex operation.	**4.4.11 Front Panel Devices**			Inspection	**Design**
312	Flow control shall use XON/XOFF procedures.	**4.4.11 Front Panel Devices**			Inspection	**Design**
211	When a mismatch is detected for 1000 milliseconds or more, the CMU shall cause a LFSA.	**4.4.7 Field Output Check**	P	Verified because Mr. Johnson pulled out a relay "hot" and we saw the unit go into flash.	Performance Test	**Performance**
213	Field Output Check monitoring shall be disabled when the MAIN CONTACTOR COIL STATUS input is not active.	**4.4.7 Field Output Check**	P		Analysis	**Performance**
224	A Red signal input shall be sensed active when it exceeds 70 Volts RMS and shall not be sensed active when it is less than 50 Volts RMS.	**4.4.9 Input Signals**	P	Verified by changing the input voltage via a variac, monitored in RMS with a Tektronix Scope. The operational need for using 70 Vols revolves around the fact that at that voltage, the light is seen as "on."	Performance Test	**Performance**
225	A Red signal between 50 Volts RMS and 70 Volts RMS may or may not be sensed active.	**4.4.9 Input Signals**	P		Performance Test	**Performance**
257	The CMU shall monitor the DOOR SWITCH FRONT and DOOR SWITCH REAR inputs.	**4.4.9 Input Signals**	P	If either door is open the door is open, but only when both doors are closed does it report closed.	Inspection	**Performance**
278	Clear LEDs shall only show the die and not appear to be ON when exposed to ambient light.	**4.4.11 Front Panel Devices**	P	This verbiage actually defines "clear" LEDS. Verified by shing a high intensity light into the flashing LEDs in the Cabinet.	Inspection	**Performance**
279	A green POWER indicator shall illuminate to indicate AC+ Raw voltage is proper.	**4.4.11 Front Panel Devices**	P		Performance Test	**Performance**
280	It [the green POWER indicator] shall flash at a 2 Hertz rate when the NRESET or POWERDOWN input is True.	**4.4.11 Front Panel Devices**	P		Performance Test	**Performance**
281	It [the green POWER indicator] shall remain off when the voltage is less than 80 Volts RMS (+/-2 Volts RMS).	**4.4.11 Front Panel Devices**	P	This occurred at around 69V RMS.	Performance Test	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
282	A red 24VDC FAIL indicator shall illuminate when the CMU is in FSA as a result of a 24VDC cabinet power supply fault.	**4.4.11 Front Panel Devices**	P	Verified by removing the fuse.	Performance Test	**Performance**
283	A red 12VDC FAIL indicator shall illuminate when the CMU is in FSA as a result of a 12VDC cabinet power supply fault.	**4.4.11 Front Panel Devices**	n/a	The Seimens cabinet we used was not programmed for this functionality.	Performance Test	**Performance**
284	The 12VDC FAIL indicator shall flash at a 2 Hertz rate when the 12 VDC monitor function is disabled.	**4.4.11 Front Panel Devices**	P	Because our unit was programmed as above, we could verify this could be tested.	Performance Test	**Performance**
285	A red CONFLICT indicator shall illuminate when the CMU is in FSA as a result of a Conflicting Channels fault.	**4.4.11 Front Panel Devices**	P		Performance Test	**Performance**
286	A red LACK OF SIGNAL indicator shall illuminate when the CMU is in FSA as a result of a Lack of Signal Inputs fault.	**4.4.11 Front Panel Devices**	P		Performance Test	**Performance**
287	A red MULTIPLE indicator shall illuminate when the CMU is in FSA as a result of a Multiple Inputs fault.	**4.4.11 Front Panel Devices**	P	In our case, we had a conflict running concurrently, so we could not see this on the CMU we were looking at. We re-ran with the conflict cleared to verify.	Performance Test	**Performance**
288	A red ATC/LOCAL FLASH indicator shall illuminate when the CMU is in FSA as a result of a Type 62 – Send to Local Flash Command from the ATC Controller Unit, the LOCAL FLASH STATUS input sensed inactive, or CB TRIP STATUS active.	**4.4.11 Front Panel Devices**	P	Verified via CB TRIP.	Performance Test	**Performance**
289	A red CLEARANCE indicator shall illuminate when the CMU is in FSA as a result of a Yellow Clearance or Yellow Plus Red Clearance fault.	**4.4.11 Front Panel Devices**	P		Performance Test	**Performance**
290	A red SB #1 ERROR indicator shall illuminate when the CMU is in FSA as a result of a Serial Bus #1 fault.	**4.4.11 Front Panel Devices**	P		Performance Test	**Performance**
291	A red SB #3 ERROR indicator shall illuminate when the CMU is in FSA as a result of a Serial Bus #3 fault.	**4.4.11 Front Panel Devices**	P		Performance Test	**Performance**
292	A red DIAGNOSTIC indicator shall illuminate when the CMU is in FSA as a result of a Diagnostic fault.	**4.4.11 Front Panel Devices**	P	Verified by removing the Key.	Performance Test	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
293	The DIAGNOSTIC indicator shall flash at a 4 Hertz rate if the serial memory key is not present and a FSA state does not exist.	**4.4.11 Front Panel Devices**	P	Verified by removing the Key.	Performance Test	**Performance**

B.18 ITS Cabinet Model 214 Auxiliary Monitor Unit (AMU) Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
	The following indicators shall be provided (Top to Bottom):					**Design**
313	The AMU shall reside in each of the Output Assemblies.	**4.5.1 General**			Inspection	**Design**
314	The AMU shall interface to the CMU via Serial Bus #3.	**4.5.1 General**			Inspection	**Design**
315	An AMU shall operate in a fourteen-channel mode (14 Pack) or a six-channel mode (6 Pack) depending on the Address Select inputs.	**4.5.1 General**			Inspection	**Design**
316	The Address Select input pins ADDRESS 0, ADDRESS 1, and ADDRESS 2 shall define the Serial Bus #3 address of the AMU and the number of channels reported.	**4.5.1 General**			Inspection	**Design**
317	The [Address Select input] pins shall be left open for a logical False, and are connected to ADDRESS COMMON for a logical True.	**4.5.1 General**			Inspection	**Design**
318	*Mode / Position* / *ADDRESS 2* / *ADDRESS 1* / *ADDRESS 0* / *SB #3 ADDRESS* 14 Ch/1 and 2 / False / False / True / 0x01 14 Ch/3 and 4 / False / True / True / 0x03 6 Ch/1 / True / False / True / 0x05 6 Ch/2 / True / True / False / 0x06 6 Ch/3 / True / True / True / 0x07 6 Ch/4 / True / False / False / 0x04	**4.5.1 General**			Analysis	**Design**
319	A 14 Pack Output Assembly configured in position 1 and 2 shall respond as AMU #1 with AMU #2 reserved.	**4.5.1 General**			Inspection	**Design**
320	A 14 Pack Output Assembly configured in position 3 and 4 shall respond as AMU #3 with AMU #4 reserved.	**4.5.1 General**			Inspection	**Design**
321	The 6 Pack Output Assembly shall have ADDRESS 2 permanently connected to ADDRESS COMMON on the assembly.	**4.5.1 General**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
322	All AC RMS voltage measurements shall be made over an RMS period of 33.3 milliseconds (two AC Line cycles).	**4.5.2 AC Voltage Sensing**			Performance Test	**Design**
323	All AC signals shall be sampled at a minimum of 1920 samples per second.	**4.5.2 AC Voltage Sensing**			Analysis	**Design**
324	A True RMS voltage measurement shall be made regardless of phase or wave-shape, including both positive and negative half wave sinusoids, over the voltage range of 0 Volts RMS to 135 Volts RMS.	**4.5.2 AC Voltage Sensing**			Analysis	**Design**
325	AC voltage measurements shall be accurate to +/-2 Volts RMS.	**4.5.2 AC Voltage Sensing**			Analysis	**Design**
326	Three inputs shall be provided for each of fourteen channels (36 total) to permit the monitoring of voltages at the Green, Yellow, and Red signal field terminals.	**4.5.3 Field Signal Sensing**			Inspection	**Design**
327	The AMU shall be designed so that unused Green, Yellow, or Red signal inputs are not sensed as active signals.	**4.5.3 Field Signal Sensing**			Analysis	**Design**
329	Each field input voltage shall be reported in the Type 129 or 130 frame.	**4.5.3 Field Signal Sensing**			Performance Test	**Design**
331	The AC Line voltage shall be reported in the Type 129 or 130 frame.	**4.5.4 AC Line Sensing**			Performance Test	**Design**
333	Each FLASHER input voltage shall be reported in the Type 129 or 130 frame.	**4.5.5 Flasher Line Sensing**			Performance Test	**Design**
335	Voltages at, or greater than, +22 VDC shall be considered proper for Assembly operation.	**4.5.6 +24 VDC Sensing**			Analysis	**Design**
336	Voltages at, or less than, +18 VDC shall be considered not proper for Assembly operation.	**4.5.6 +24 VDC Sensing**			Analysis	**Design**
337	The +24 VDC MONITOR state shall be reported in the Type 129 or 130 frames.	**4.5.6 +24 VDC Sensing**			Performance Test	**Design**
338	The +24 VDC MONITOR voltage section shall be electrically isolated from the AC- Raw referenced circuitry.	**4.5.6 +24 VDC Sensing**			Performance Test	**Design**
339	All AC RMS current measurements shall be made over a period of two AC Line cycles (33.3 milliseconds).	**4.5.7 Current Sensing**		Current Sensing is currently not implemented in this design.	Analysis	**Design**
340	A True RMS current measurement shall be made regardless of phase or wave-shape, including both positive and negative half wave sinusoids.	**4.5.7 Current Sensing**			Analysis	**Design**
341	AC current measurements shall be accurate to +/-35%.	**4.5.7 Current Sensing**			Performance Test	**Design**
342	The AMU shall sense the total output current of each Switch Pack.	**4.5.7 Current Sensing**			Analysis	**Design**
343	Each Switch Pack output current shall be reported in the Type 129 or 130 frames.	**4.5.7 Current Sensing**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
344	The input impedance of the COIL+ input with respect to the COIL-input shall be 1000 Ohms.	**4.5.7 Current Sensing**			Analysis	**Design**
345	Full-scale current is set by the number of primary turns through the transformer and shall be a maximum of four turns.	**4.5.7 Current Sensing**			Inspection	**Design**
346	Unless specified otherwise, one turn shall be provided.	**4.5.7 Current Sensing**			Inspection	**Design**
347	The Switch Pack current sensing transformers shall meet the following requirements: Linearity 25% from 10 milliamperes to 1Ampere (single primary turn) Accuracy +/-25% (Rin = 1000 Ohms) Primary Current 10 Amperes maximum Minimum hole size 0.25 inch diameter Insulation Resistance 100 Megohms at 500 VDC	**4.5.7 Current Sensing**			Performance Test	**Design**
348	The transformer shall output a voltage of 1.0 Volts RMS (+/-5%) across 1K Ohms when driven by 1.0 Arms sinusoidal current through one primary turn.	**4.5.7 Current Sensing**			Performance Test	**Design**
349	Sufficient secondary turns shall be provided to compensate for differences in core material and losses to produce the 1.0 Volts RMS output.	**4.5.7 Current Sensing**			Inspection	**Design**
350	The AMU shall be provided with a resident series of self-check diagnostic capabilities.	**4.5.8 Diagnostic Error**			Analysis	**Design**
351	At a minimum, the AMU shall contain provisions to verify all memory elements on power-up and Reset.	**4.5.8 Diagnostic Error**			Analysis	**Design**
353	This test [the RAM diagnostic] shall verify that all RAM elements are operating correctly at power-up.	**4.5.8 Diagnostic Error**			Analysis	**Design**
354	Patterns shall be written to RAM.	**4.5.8 Diagnostic Error**			Performance Test	**Design**
355	Each Write shall be followed by a Read to verify that it contains the written pattern.	**4.5.8 Diagnostic Error**			Performance Test	**Design**
356	This test [the non-volatile memory diagnostic] shall verify that the nonvolatile ROM(s) contain the proper program.	**4.5.8 Diagnostic Error**			Analysis	**Design**
357	The routine shall perform a check on each ROM and make a comparison with a preprogrammed check value.	**4.5.8 Diagnostic Error**			Analysis	**Design**
358	This test shall be performed at power-up and at a minimum rate of 1024 bits per second during operation.	**4.5.8 Diagnostic Error**			Performance Test	**Design**
359	The AMU shall monitor the operation of its microprocessor.	**4.5.8 Diagnostic Error**			Analysis	**Design**
360	At a minimum, the monitoring circuit shall be triggered at least every 100 milliseconds.	**4.5.8 Diagnostic Error**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
361	The microprocessor shall be reset and the DIAGNOSTIC indicator illuminated if the monitoring circuit has not been triggered for a maximum of 1000 milliseconds.	**4.5.8 Diagnostic Error**			Performance Test	**Design**
362	The AMU shall generate its own power supply voltage from the AC+ Raw input using no more than 5 Watts.	**4.5.9 Power Requirements**			Performance Test	**Design**
363	It [the AMU] shall be capable of insertion and removal while AC power is applied to the cabinet.	**4.5.9 Power Requirements**			Performance Test	**Design**
364	Surge current on AC+ Raw input shall be less than 2 Amperes peak.	**4.5.9 Power Requirements**			Performance Test	**Design**
365	The AMU shall be operational over the voltage range of 80 Volts RMS to 135 Volts RMS.	**4.5.9 Power Requirements**			Analysis	**Design**
366	The AMU shall be fully functional within 500 milliseconds following AC+ Raw voltage exceeding 80 Volts RMS or Reset.	**4.5.9 Power Requirements**			Performance Test	**Design**
367	During the loss of AC+ Raw voltage for 700 milliseconds or less the AMU shall continue to operate.	**4.5.9 Power Requirements**			Performance Test	**Design**
368	All indicators shall be clear LEDS.	**4.5.10 AMU User Interface**			Inspection	**Design**
369	Clear LEDs shall not depend on a reflector or diffusion as part of its design.	**4.5.10 AMU User Interface**			Inspection	**Design**
370	Clear LEDs shall only show the die and not appear to be ON when exposed to ambient light.	**4.5.10 AMU User Interface**			Inspection	**Design**
376	The [yellow] indicator shall pulse ON for 40 milliseconds each time the AMU correctly receives a frame with its address on the Bus #3 input.	**4.5.10 AMU User Interface**			Performance Test	**Design**
377	This [yellow] indicator shall be labeled SB #3 RX.	**4.5.10 AMU User Interface**			Inspection	**Design**
381	A recessed RESET switch shall be provided which applies a direct reset to the microprocessor device on the AMU.	**4.5.10 AMU User Interface**			Analysis	**Design**
382	All voltage and current data shall be initialized to zero following Reset.	**4.5.10 AMU User Interface**			Performance Test	**Design**
383	The access hole shall be 0.25 inches in diameter.	**4.5.10 AMU User Interface**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
384	The AMU connector shall be a DIN 4161296 Header Type.	**4.5.10 AMU User Interface**			Inspection	**Design**
385	Pins A31 (Equipment Ground), B32 (AC-Raw), and C32 (AC-Raw) shall pre-mate before all other pins.	**4.5.10 AMU User Interface**			Inspection	**Design**
386	The AMU pin assignments shall be as shown on drawing 4-11-6.	**4.5.10 AMU User Interface**		Need to have the full standard available to reference these drawings.	Inspection	**Design**
387	TxD+, TxD- and RxD+, RxD- shall consist of two interface links conforming to the requirements of the Electronic Industries Association EIA-485, Standard for Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems, dated April 1983.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
388	Where differences occur between the EIA-485 standard and this document, this document shall govern.	**4.5.11 Bus #3 Profile**		Need to dig up this specification.	Inspection	**Design**
389	All voltage potentials on the Bus #3 TxD+, TxD-, RxD+, and RxD- interface links shall be referenced to AC- Raw.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
390	The data link layer protocol is based on a subset of HDLC as defined by ISO/IEC 3309. Each frame shall consist of the following fields: 1. Flag byte = 0x7E 2. Address byte = 0x01 through 0x07 3. Control byte = 0x13 (U Format) 4. Information field = defined below in section 4.5.12, Frame Types 5. Frame Check Sequence = 16 bit FCS procedure defined in clause 4.6.2 of ISO/IEC 3309. 6. Flag byte = 0x7E	**4.5.11 Bus #3 Profile**			Analysis	**Design**
391	Transmission shall be in start/stop mode with basic transparency defined by clause 4.5.2.2 of ISO/IEC 3309 applied.	**4.5.11 Bus #3 Profile**		Need to dig up this specification.	Analysis	**Design**
392	The format shall be 8 bit data, 1 stop bit, no parity, and 153,600 bits per second (+/-2%).	**4.5.11 Bus #3 Profile**			Analysis	**Design**
393	Only asynchronous half duplex operation shall be permitted.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
394	Frames transmitted by the CMU shall be referred to as command frames and frames transmitted by the AMU shall be referred to as response frames.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
395	Command frames shall be transmitted only to those AMUs that are present, as determined by the programming entries made in the CMU.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
396	Response frames shall only be transmitted as a result of correctly receiving a command frame.	**4.5.11 Bus #3 Profile**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
397	The first eight bits in each information field shall contain the frame Type number.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
398	There shall be a maximum of 64 different command frame types and 64 different response frame types.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
399	Additionally, there shall be 64 different command frame types reserved for special application use and 64 different response frame types reserved for special application use, as outlined below. *FRAME TYPES* — *FUNCTION* 1-63 — Command frame defined by this standard 0, 64-127 — Command frame reserved 128-191 — Response frame defined by this standard 192-255 — Response frame reserved	**4.5.11 Bus #3 Profile**			Analysis	**Design**
400	Reserved bits shall always be set to zero by the transmitting station.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
401	The AMU shall begin its response to command frames from the CMU within a designated period of time following the correct reception of a complete command frame including the closing flag.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
402	This [designated period for the AMU to begin its response] period shall be known as the Service Time and shall have a maximum value of 500 microseconds.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
403	The AMU TxD link output shall be in its high impedance state outside of the interval defined by the Service Time plus Response Time.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
404	The AMU shall complete its transmission of the response frame including the closing flag within a designated time known as the Response Time, depending on the number of bytes transmitted in the response frame.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
405	The AMU TxD link output shall be in its high impedance state a maximum of 200 microseconds following the transmission of the closing flag.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
406	The Response Time period shall have a maximum value of (1.2)*(# of bytes in information field +6)*(10/153600).	**4.5.11 Bus #3 Profile**			Analysis	**Design**
407	Note that due to the transparency mechanism, any occurrence of the flag byte (0x7E) or control escape byte (0x7D) in the information field adds a second byte to the count. Thus, the number of bytes in the information field could be doubled if all characters are 0x7E or 0x7D.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
408	Following the transmission of each command frame, there shall be a Dead Time during which the CMU does not transmit.	**4.5.11 Bus #3 Profile**			Analysis	**Design**
409	This Dead Time shall be a minimum of the Service Time plus the Response Time.	**4.5.11 Bus #3 Profile**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>410</td><td>This frame [Type 1 Command Frame] shall be transmitted from the CMU to each AMU-6 at least once every RMS period (33.3 milliseconds, two AC Line cycles, averaging time for RMS measurement).</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>411</td><td>Its [the Type I Command Frame] purpose is to request the status from an AMU-6.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>412</td><td>Polling the AMU-6 more often than the RMS period may result in the same response frame being repeated.
<table>
<tr><th>Byte #</th><th>Contents</th><th>Description</th></tr>
<tr><td>1</td><td>01</td><td>Frame Type</td></tr>
</table></td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>413</td><td>This AMU-6 Status frame shall be transmitted only if a Type 1 command frame has been correctly received from the CMU.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>414</td><td>The AMU-6 shall report the data for the most recent RMS period calculated when the Type 1 command is received.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>415</td><td>The Type 1 command frame polling rate shall not affect the accuracy or RMS period of the data.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>416</td><td>
<table>
<tr><th>Byte #</th><th>Contents</th><th>Description</th></tr>
<tr><td>1</td><td>129</td><td>Frame Type</td></tr>
<tr><td>2</td><td>AMU Status</td><td>6 Pack AMU Status
b0 = set to 1 if +24 VDC MONITOR input is Low
b1:4 = reserved
b5 = set if AMU has reset since last poll
b6 = set if last RMS period data was not transmitted
b7 = diagnostic failure</td></tr>
<tr><td>3</td><td>0-135</td><td>AC+ Raw voltage</td></tr>
<tr><td>4</td><td>Channel 1 Red</td><td rowspan="13">Channel RMS Voltages</td></tr>
<tr><td>5</td><td>Channel 2 Red</td></tr>
<tr><td>6</td><td>Channel 3 Red</td></tr>
<tr><td>7</td><td>Channel 4 Red</td></tr>
<tr><td>8</td><td>Channel 5 Red</td></tr>
<tr><td>9</td><td>Channel 6 Red</td></tr>
<tr><td>10</td><td>Channel 1Yellow</td></tr>
<tr><td>11</td><td>Channel 2 Yellow</td></tr>
<tr><td>12</td><td>Channel 3 Yellow</td></tr>
<tr><td>13</td><td>Channel 4 Yellow</td></tr>
</table></td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
	14 Channel 5 Yellow 15 Channel 6 Yellow 16 Channel 1 Green 17 Channel 2 Green 18 Channel 3 Green 19 Channel 4 Green 20 Channel 5 Green 21 Channel 6 Green 22 Flasher #1-1 23 Flasher #1-2 24 Flasher #2-1 25 Flasher #2-2 — Flasher RMS Voltages 26 Channel 1 27 Channel 2 28 Channel 3 29 Channel 4 30 Channel 5 31 Channel 6 — Channel Load Current: The current value reported shall be the measured current in Amperes times 255 divided by the Full Scale (FS) parameter. For 1 primary turn, FS =1.0 (range is 0 to 1.0 Arms) For 2 primary turns, FS =0.5 (range is 0 to 0.5 Arms) For 3 primary turns, FS = 0.33 (range is 0 to 0.33 Arms) For 4 primary turns, FS =0.25 (range is 0 to 0.25 Arms) 32 0 Reserved 33 0 Reserved					
417	This frame [Type 2 Command Frame] shall be transmitted from the CMU to each AMU-14 at least once every RMS period.	**4.5.12 Frame Types**			Analysis	**Design**
418	Its [Type 2 Command Frame] purpose is to request the status from an AMU-14.	**4.5.12 Frame Types**			Analysis	**Design**
419	Polling the AMU-14 more often than the RMS period may result in the same response frame being repeated.	**4.5.12 Frame Types**		It is not clear what part this type of information plays in a standard.	Analysis	**Design**
420	*Byte #* / *Contents* / *Description* 1 / 02 / Frame Type	**4.5.12 Frame Types**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>421</td><td>This AMU-14 Status frame shall be transmitted only if a Type 2 command frame has been correctly received from the CMU.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>422</td><td>The AMU-14 shall report the data for the most recent RMS period calculated when the Type 2 command is received.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>423</td><td>The Type 2 command frame polling rate shall not affect the accuracy or RMS period of the data.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>424</td><td>
<table>
<tr><th>Byte #</th><th>Contents</th><th>Description</th></tr>
<tr><td>1</td><td>130</td><td>Frame Type</td></tr>
<tr><td>2</td><td>AMU Status</td><td>14 Pack AMU Status
b0 = set to 1 if +24 VDC MONITOR input is Low
b1:4 = reserved
b5 = set if AMU has reset since last poll
b6 = set if last RMS period data was not transmitted
b7 = diagnostic failure</td></tr>
<tr><td>3</td><td>0-135</td><td>AC+ Raw voltage</td></tr>
<tr><td>4</td><td>Channel 1 Red</td><td rowspan="15">Channel RMS Voltages</td></tr>
<tr><td>5</td><td>Channel 2 Red</td></tr>
<tr><td>6</td><td>Channel 3 Red</td></tr>
<tr><td>7</td><td>Channel 4 Red</td></tr>
<tr><td>8</td><td>Channel 5 Red</td></tr>
<tr><td>9</td><td>Channel 6 Red</td></tr>
<tr><td>10</td><td>Channel 7 Red</td></tr>
<tr><td>11</td><td>Channel 8 Red</td></tr>
<tr><td>12</td><td>Channel 9 Red</td></tr>
<tr><td>13</td><td>Channel 10 Red</td></tr>
<tr><td>14</td><td>Channel 11 Red</td></tr>
<tr><td>15</td><td>Channel 12 Red</td></tr>
<tr><td>16</td><td>Channel 13 Red</td></tr>
<tr><td>17</td><td>Channel 14 Red</td></tr>
<tr><td>18</td><td>Channel 1Yellow</td></tr>
</table>
</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)			Document Section	Pass / Fail	Comments	Type	Requirement Type
	19	Channel 2 Yellow						
	20	Channel 3 Yellow						
	21	Channel 4 Yellow						
	22	Channel 5 Yellow						
	23	Channel 6 Yellow						
	24	Channel 7Yellow						
	25	Channel 8 Yellow						
	26	Channel 9 Yellow						
	27	Channel 10 Yellow						
	28	Channel 11 Yellow						
	29	Channel 12 Yellow						
	30	Channel 13 Yellow						
	31	Channel 14 Yellow						
	32	Channel 1 Green						
	33	Channel 2 Green						
	34	Channel 3 Green						
	35	Channel 4 Green						
	36	Channel 5 Green						
	37	Channel 6 Green						
	38	Channel 7 Green						
	39	Channel 8 Green						
	40	Channel 9 Green						
	41	Channel 10 Green						
	42	Channel 11 Green						
	43	Channel 12 Green						
	44	Channel 13 Green						
	45	Channel 14 Green						
	46	Flasher #1-1	Flasher RMS Voltages					
	47	Flasher #1-2						
	48	Flasher #2-1						
	49	Flasher #2-2						

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td></td><td>
<table>
<tr><td>50</td><td>Channel 1</td><td rowspan="14">Channel Load Current
The current value reported shall be the measured current in Amperes times 255 divided by the Full Scale (FS) parameter.
For 1 primary turn, FS =1.0 (range is 0 to 1.0 Arms)
For 2 primary turns, FS =0.5 (range is 0 to 0.5 Arms)
For 3 primary turns, FS = 0.33 (range is 0 to 0.33 Arms)
For 4 primary turns, FS =0.25 (range is 0 to 0.25 Arms)</td></tr>
<tr><td>51</td><td>Channel 2</td></tr>
<tr><td>52</td><td>Channel 3</td></tr>
<tr><td>53</td><td>Channel 4</td></tr>
<tr><td>54</td><td>Channel 5</td></tr>
<tr><td>55</td><td>Channel 6</td></tr>
<tr><td>56</td><td>Channel 7</td></tr>
<tr><td>57</td><td>Channel 8</td></tr>
<tr><td>58</td><td>Channel 9</td></tr>
<tr><td>59</td><td>Channel 10</td></tr>
<tr><td>60</td><td>Channel 11</td></tr>
<tr><td>61</td><td>Channel 12</td></tr>
<tr><td>62</td><td>Channel 13</td></tr>
<tr><td>63</td><td>Channel 14</td></tr>
<tr><td>64</td><td>0</td><td>Reserved</td></tr>
<tr><td>65</td><td>0</td><td>Reserved</td></tr>
</table>
</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>425</td><td>This frame shall be transmitted from the AMU to the CMU as a Negative Acknowledge response frame if the AMU correctly receives a command frame with an invalid parameter.</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>426</td><td>
<table>
<tr><th>Byte #</th><th>Contents</th><th>Description</th></tr>
<tr><td>1</td><td>128</td><td>Frame Type (Negative Acknowledge)</td></tr>
<tr><td>2</td><td>Status</td><td>AMU SB #3 Error Type
b0 = set to 1 if invalid frame type received
b1:7 = reserved</td></tr>
</table>
</td><td>4.5.12 Frame Types</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>328</td><td>The AMU shall sense an input at less than 15 Volts RMS when connected to AC Line through 1500 picofarads.</td><td>4.5.3 Field Signal Sensing</td><td>P</td><td></td><td>Performance Test</td><td>Performance</td></tr>
<tr><td>330</td><td>The AMU shall include the capability of monitoring the AC Line voltage applied to its AC+ Raw input.</td><td>4.5.4 AC Line Sensing</td><td>P</td><td></td><td>Inspection</td><td>Performance</td></tr>
<tr><td>332</td><td>Four inputs shall be provided for sensing of voltages at the FLASHER #1-1, FLASHER #1-2, FLASHER #2-1, and FLASHER #2-2 signal input terminals of the Output Assembly.</td><td>4.5.5 Flasher Line Sensing</td><td>P</td><td></td><td>Inspection</td><td>Performance</td></tr>
<tr><td>334</td><td>The AMU shall sense the state of the +24 VDC MONITOR input.</td><td>4.5.6 +24 VDC Sensing</td><td>P</td><td></td><td>Analysis</td><td>Performance</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
352	When an error is detected, the AMU shall illuminate the DIAGNOSTIC indicator and disable the Serial Bus #3 port.	**4.5.8 Diagnostic Error**	P		Performance Test	**Performance**
372	A green POWER indicator shall be provided.	**4.5.10 AMU User Interface**	p		Inspection	**Performance**
373	The [green POWER] indicator shall be illuminated when the AC+ Raw input is 80 Volts RMS (+/-2 Volts RMS) or greater.	**4.5.10 AMU User Interface**	p		Inspection	**Performance**
374	This [green] indicator shall be labeled POWER.	**4.5.10 AMU User Interface**	p		Inspection	**Performance**
375	A yellow Serial Bus #3 indicator shall be provided.	**4.5.10 AMU User Interface**	p		Inspection	**Performance**
378	A red DIAGNOSTIC indicator shall be provided.	**4.5.10 AMU User Interface**	P		Inspection	**Performance**
379	The [red DIAGNOSTIC] indicator shall be ON when an internal diagnostic error is detected.	**4.5.10 AMU User Interface**		Cannot be performed.	Performance Test	**Performance**
380	This [red] indicator shall be labeled DIAGNOSTIC.	**4.5.10 AMU User Interface**	p		Inspection	**Performance**

B.19 ITS Cabinet Model 216-12 & 216-24 Power Supply Unit Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
429	When resident in the PDA ITS, the units shall be held firmly in place by its stud screws and wing nut.	**4.6.1 General Requirements**			Inspection	**Design**
430	Two units, 216-12 and 216-24 shall provide +12 and +24 VDC, respectively, to the cabinet assemblies.	**4.6.1 General Requirements**			Inspection	**Design**
431	They shall be of ferro-resonant design.	**4.6.1 General Requirements**		What does “ferro-resonant” mean?	Inspection	**Design**
432	They [unit chassis] shall have no active components and conform to the requirements of this section.	**4.6.1 General Requirements**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
434	This [line and load regulation] includes ripple noise; from 90 VAC to 135 VAC at 60 Hertz, plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 Ampere to 5 Amperes with a maximum temperature rise of 30 degrees C above ambient.	**4.6.1 General Requirements**			Analysis	**Design**
435	Design Center Voltage shall be +24 VDC (+/-0.5 VDC) and +12 VDC (+/-0.5 VDC) at full load, at 30 degrees C, and with 115 VAC incoming after a 30-minute warm-up period.	**4.6.1 General Requirements**			Analysis	**Design**
436	Full Load Current shall be 5 AMPERES each for +24 VDC and +12 VDC, minimum.	**4.6.1 General Requirements**			Analysis	**Design**
437	Ripple Noise shall be 2 Volts peak-to-peak and 500 millivolts RMS at full load.	**4.6.1 General Requirements**			Analysis	**Design**
438	Line Voltage shall be 90 VAC to 135 VAC.	**4.6.1 General Requirements**			Analysis	**Design**
439	Efficiency shall be 70% minimum.	**4.6.1 General Requirements**			Analysis	**Design**
440	Circuit capacitors shall be rated for 40 Volts minimum.	**4.6.1 General Requirements**			Analysis	**Design**
441	The front panel shall include AC and DC fuses, power ON light and banana clip test points for monitoring the output voltages.	**4.6.1 General Requirements**			Inspection	**Design**
442	The unit, including terminals, shall be protected with a 1K Ohm, 0.5 watt resistor to prevent accidental contact with energized parts.	**4.6.1 General Requirements**			Inspection	**Design**
427	The unit chassis shall be vented.	**4.6.1 General Requirements**	P	Units are usually open.	Inspection	**Performance**
428	The power supply cage and transformers shall be securely braced to prevent damage in transit.	**4.6.1 General Requirements**	P		Inspection	**Performance**
433	Line and load regulation shall meet the two power supply ranges for +24 VDC (23.0 VDC to 26 VDC) and +12 VDC (11.65 VDC to 13.35 VDC).	**4.6.1 General Requirements**	P	Saw a slight overage on the +12 VDC line at either end of the input voltage – 77 – 125V. By plugging in some load detectors that actually used the DC line, we saw expected performance out of the power supply.	Analysis	**Performance**

B.20 ITS Cabinet Type 218 – Serial Interface Unit (SIU) Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
	The SIU includes three interrupt sources as follows:	**4.7.11 Interrupts**				**Design**
445	In advanced detectors, the status outputs may be converted to per channel resets.	**4.7.1 General**			Inspection	**Design**
446	When installed in an ITS 14 Pack Output Assembly, the SIU controls fourteen Switch Pack Units (forty-two Outputs) and four Optical Inputs through the CDC socket.	**4.7.1 General**			Inspection	**Design**
447	The SIU requires a nominal supply voltage of 24 VDC (+/-2 VDC).	**4.7.2 Power Requirements**			Inspection	**Design**
448	A voltage of 16 VDC or less shall be considered loss of power and a voltage of 18 VDC or greater shall be considered adequate for operation.	**4.7.2 Power Requirements**			Analysis	**Design**
449	The SIU shall not require more than 300 milliamperes over the voltage range of 16 VDC to 30 VDC and the power surge shall be limited to a maximum of 1.25 Amperes from initial application of DC power.	**4.7.2 Power Requirements**			Analysis	**Design**
450	The SIU shall not be damaged by insertion to, or removal from, powered input or output assemblies.	**4.7.2 Power Requirements**			Performance Test	**Design**
451	The SIU operates normally for 700 milliseconds after power loss.	**4.7.2 Power Requirements**			Performance Test	**Design**
452	The SIU Controller Unit shall include a microprocessor/controller unit together with all required clocking and support circuitry.	**4.7.3 Microprocessor**			Inspection	**Design**
453	Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware or internal Flash memory.	**4.7.4 Memory**			Inspection	**Design**
454	The SIU uses NRESET lines for SIU shut down/turn on operations matching the ATC Controller Unit CPU.	**4.7.5 Control Signals**			Analysis	**Design**
455	The SIU shall be fully initialized and providing specified operation upon NRESET Line going HIGH (Power Up).	**4.7.5 Control Signals**			Performance Test	**Design**
456	In the ATC Controller, the NRESET operation shall cause the SIU program restart.	**4.7.5 Control Signals**			Performance Test	**Design**
457	No prior message operation data retention is required [after an SIU program restart].	**4.7.5 Control Signals**			Analysis	**Design**
458	The Request Module Status Response may report this restart as either a Power On or Watchdog.	**4.7.5 Control Signals**			Performance Test	**Design**
459	ATC Controller Unit LINESYNC is used as a system time reference.	**4.7.5 Control Signals**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
460	The microprocessor/controller unit is reset by any of the following: Pushbutton Reset NRESET Signal +5 VDC out of regulation Microprocessor/controller unit watchdog	**4.7.5 Control Signals**			Performance Test	**Design**
461	The SIU includes a 1 Kilohertz Time Reference to provide system response time stamps.	**4.7.6 Time References**			Inspection	**Design**
462	The 1 Kilohertz Time Reference shall maintain a frequency accuracy of +/-0.01% (+/-0.1 counts per second).	**4.7.6 Time References**			Performance Test	**Design**
463	A watchdog circuit shall be provided.	**4.7.7 Watchdog**			Analysis	**Design**
464	The SIU shall power up with the watchdog enabled.	**4.7.7 Watchdog**			Performance Test	**Design**
465	Within the first watchdog time period, the watchdog value shall be set to 200 milliseconds +/-100 milliseconds.	**4.7.7 Watchdog**			Performance Test	**Design**
466	The watchdog state shall be reported in the SIU status byte as an indication that a watchdog has occurred, which will remain until cleared in the Request Module Status command.	**4.7.7 Watchdog**			Performance Test	**Design**
467	Failure of the SIU to reset the watchdog timer shall result in hardware reset.	**4.7.7 Watchdog**			Performance Test	**Design**
468	A 32-bit Millisecond Counter shall be provided for “time stamping.”	**4.7.8 Millisecond Counter**			Inspection	**Design**
469	Each 1 Kilohertz reference shall increment the Millisecond Counter.	**4.7.8 Millisecond Counter**			Performance Test	**Design**
470	A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries.	**4.7.9 Buffers**			Analysis	**Design**
471	The Transition Buffer shall default to empty.	**4.7.9 Buffers**			Performance Test	**Design**
472	There shall be two entry types [in the Transition Buffer]: Transition and Rollover.	**4.7.9 Buffers**			Analysis	**Design**
473	The inputs shall be monitored for state transition.	**4.7.9 Buffers**			Analysis	**Design**
474	At each transition (if the input has been configured to report transition, 4.7.15.4), a transition entry shall be added to the Transition Buffer.	**4.7.9 Buffers**			Performance Test	**Design**
475	If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing input number.	**4.7.9 Buffers**			Performance Test	**Design**
476	The Millisecond Counter shall be monitored for rollover.	**4.7.9 Buffers**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>477</td><td>At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer.</td><td>4.7.9 Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>478</td><td>For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry.</td><td>4.7.9 Buffers</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>479</td><td>A new entry shall be discarded when storage is not available for the new entry.</td><td>4.7.9 Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>480</td><td>Transition Buffer blocks are sent to the ATC Controller Unit upon command.</td><td>4.7.9 Buffers</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>481</td><td>Upon confirmation of their reception, the [Transition Buffer] blocks shall be removed from the Transition Buffer. See Section 4.7.15.7.</td><td>4.7.9 Buffers</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>482</td><td>The entry types are as follows:

Input Transition Entry
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>Transition Entry Identifier</td><td>S</td><td colspan="7">Input Number (I0 – I59)</td><td>1</td></tr>
<tr><td>Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>2</td></tr>
<tr><td>Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td></tr>
</table>
Millisecond Counter Rollover Entry
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>Rollover Entry Identifier</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>2</td></tr>
<tr><td>Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>3</td></tr>
</table></td><td>4.7.9 Buffers</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>483</td><td>At Power Up, the SIU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the “E” Bit and a subsequent set output command is processed.</td><td>4.7.10 Power Up Initialization</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>484</td><td>All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts.</td><td>4.7.11 Interrupts</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>485</td><td>MILLISECOND Interrupt shall be activated by the Time Reference.</td><td>4.7.11 Interrupts</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>486</td><td>A timestamp rollover flag set by Millisecond Counter (MC) rollover shall be cleared only on command.</td><td>4.7.11 Interrupts</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>487</td><td>The LINESYNC signal shall be generated by the controller power supply.</td><td>4.7.11 Interrupts</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
488	LINESYNC Interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal.	**4.7.11 Interrupts**			Performance Test	**Design**
489	The LINESYNC interrupt shall monitor the Millisecond Counter interrupt and set the Millisecond Counter error flag if there has not been an interrupt from the 1 Kilohertz source for 0.5 seconds (≥60 consecutive LINESYNC interrupts).	**4.7.11 Interrupts**			Analysis	**Design**
490	The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second.	**4.7.11 Interrupts**			Performance Test	**Design**
491	A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (≥500 consecutive millisecond interrupts).	**4.7.11 Interrupts**			Performance Test	**Design**
492	The Line Frequency Reference input pin shall receive a square wave signal from the cabinet power supply for the purposes of synchronizing SIU outputs with the AC line.	**4.7.11 Interrupts**			Analysis	**Design**
493	Line Frequency Reference Interrupt shall be generated by both the 0-1 and 1-0 transitions of the Line Frequency Reference signal.	**4.7.11 Interrupts**			Performance Test	**Design**
494	The Line Frequency Reference interrupt shall monitor the Millisecond Counter interrupt and set the Millisecond Counter error flag if there has not been an interrupt from the 1 Kilohertz source for 0.5 seconds (≥60 consecutive Line Frequency Reference interrupts).	**4.7.11 Interrupts**			Performance Test	**Design**
495	The Line Frequency Reference interrupt shall synchronize the Time Reference with the 0-1 transition of the Line Frequency Reference signal once a second.	**4.7.11 Interrupts**			Analysis	**Design**
496	A Line Frequency Reference error flag shall be set if the Line Frequency Reference interrupt has not successfully executed for 0.5 seconds or longer (≥500 consecutive millisecond interrupts).	**4.7.11 Interrupts**			Performance Test	**Design**
497	The electrical characteristics of the Line Frequency input are as follows: 1. A voltage between 0 and 8 volts shall be considered the LOW state, and shall occur when the AC line is in the positive half cycle. 2. A voltage between 16 and 26 volts shall be considered the High state, and shall occur when the AC line is in the negative half-cycle. 3. The Line Frequency Reference input shall exhibit a nominal impedance of 10K (+/-10%) to the +24 VDC input and shall not have more than 1000 picofarads of load capacitance. 4. The rise and fall time of the signal connected to this input shall not exceed 50 microseconds.	**4.7.11 Interrupts**			Analysis	**Design**
498	The SIU/BIU input shall be used by the SIU to determine the AC timing source.	**4.7.11 Interrupts**			Analysis	**Design**
499	If the SIU/BIU input is grounded, LINESYNC shall be used as the interrupt source.	**4.7.11 Interrupts**			Analysis	**Design**
500	If the SIU/BIU input is pulled up, Line Frequency Reference shall be used as the interrupt source.	**4.7.11 Interrupts**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
501	A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults.	**4.7.11 Interrupts**			Analysis	**Design**
502	The communication server shall automatically: *For Transmission:* Generate the opening and closing flags Generate the CRC value Generate the abort sequence (minimum of eight consecutive '1' bits) when commanded by the Microprocessor Unit Provide zero bit insertion *For Reception:* Detect the opening and closing flags Provide address comparison, generating an interrupt for messages addressed to the SIU, and ignoring messages not addressed to the SIU Strip out inserted zeros Calculate the CRC value, compare it to the received value, and generate an interrupt on an error Generate an interrupt if an abort sequence is received	**4.7.11 Interrupts**			Analysis	**Design**
503	The task shall be to process the command messages received from the ATC Controller Unit, prepare, and start response transmission.	**4.7.12 Communication Processing**			Analysis	**Design**
504	The response message transmission shall begin within four milliseconds of the receipt of the received message.	**4.7.12 Communication Processing**			Performance Test	**Design**
505	The SIU shall complete the execution of each command within 70 milliseconds of the end of each response message transmission.	**4.7.12 Communication Processing**			Performance Test	**Design**
506	This task shall process the raw input data scanned in by the 1 milliseconds interrupt routine, perform all filtering, and maintain the transition queue entries.	**4.7.13 Imput Processing**			Analysis	**Design**
507	The SIU shall have four Optically Coupled Inputs, fifty-four Parallel Input/Outputs and four Serial Ports.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
508	The Opto Common input shall be the common reference pin for four Opto Inputs.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
509	The Opto Inputs are intended to provide optical isolation for Pedestrian Detection, internal cabinet functions, Remote Interconnect or other auxiliary inputs.	**4.7.14 Inputs and Outputs**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
510	The Opto Inputs are intended to connect through external 27K Ohm, 1-Watt resistors for 120 VAC operations, and are intended for direct connection to 12 VAC for Pedestrian Detector applications.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
511	These [Opto] inputs may also be used for low-true DC applications when the Opto Common pin is connected to -24 VDC.	**4.7.14 Inputs and Outputs**		This specification appears to be informational only.	Inspection	**Design**
512	These inputs may function in the place of 242/252 isolator modules. 1. The Opto Inputs shall provide electrical isolation of 10 Megohms minimum resistance and 1000 VAC RMS minimum breakdown to all connector pins except the Opto Common pin, at a maximum breakdown leakage current of 1 milliamperes RMS. 2. These inputs shall exhibit nominal impedance to the Opto Common pin of 5000 Ohms, +10% to the Opto Common input. 3. The Opto Inputs shall not recognize 3 Volts RMS (AC sinusoid or DC) or less relative to the Opto Common input. 4. The Opto Inputs shall recognize 8 Volts RMS (AC sinusoid or DC) or more relative to the Opto Common input. 5. Any steady state voltage applied between an Opto Input and the Opto Common shall not exceed 35 VAC RMS. 6. Opto Inputs shall not be acknowledged when active for 25 milliseconds or less, and shall be acknowledged when active for 50 milliseconds or more. 7. The Opto Inputs shall conform to transient immunity specifications of section 3.7.5.4.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
513	The first Output Assembly assignments shall be dedicated as follows: *PIN* — *1st OUTPUT ASSEMBLY* — *APPLICABLE HOUSING TYPE* Opto Input 1 — Manual Control Enable — All Opto Input 2 — Interval Advance — All Opto Input 3 — Stop Time — All Opto Input 4 — Manual Flash — All Opto Input Common — AC- — All	**4.7.14 Inputs and Outputs**			Analysis	**Design**
514	SIU shall control fifty-four input/output lines using ground-true logic.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
515	Each input shall be read logic "1" (ON) when the input voltage at its field connector input is less than 8 VDC, and shall be read logic "0" (OFF) when the input voltage exceeds 16 VDC.	**4.7.14 Inputs and Outputs**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
516	Each input shall have an internal pull-up to +24 VDC of 11K Ohms maximum, and shall not deliver greater than 10 milliamperes to a short circuit to ground.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
517	Each output written as a logic "1" (ON) shall have a voltage at its field connector output of less than 4.0 VDC.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
518	Each output written as logic "0" (OFF) shall provide an open circuit (1 Megohm or more) at its field connector output.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
519	Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 milliamperes minimum.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
520	Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 microseconds when connected to a load of 100K Ohms minimum.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
521	Each output circuit shall be protected from transients of 10 microseconds (+/-2 microseconds) duration, +/-300 VDC from a 1K Ohm source, with a maximum rate of 1 pulse per second.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
522	Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
523	Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
524	The state of all output circuits at the time of Power Up or in Power Down state shall be OFF.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
525	It shall be possible to simultaneously assert all outputs within 100 microseconds of each other.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
526	An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.	**4.7.14 Inputs and Outputs**		What is the exact meaning of “glitch” in this specification?	Analysis	**Design**
527	Each parallel Input/Output function contains all of the functions listed below of both the Input Function and Output Function.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
528	Input scanning shall begin at I0 (bit 0) and proceed to the highest numbered input, ascending from LSB to MSB.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
529	Each complete input scan shall finish within 100 microseconds.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
530	Once sampled, the logic state of an input shall be held until the next input scan.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
531	Each input shall be sampled 1,000 times per second.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
532	The time interval between samples shall be 1 milliseconds (+/-100 microseconds).	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
533	The Millisecond Counter shall be sampled within 10 microseconds of the completion of the input scan.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
534	If configured, the inputs shall be filtered by the SIU to remove signal bounce.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
535	The filtered input signals shall then be monitored for changes as noted.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
536	The filtering parameters for each input shall consist of Ignore Input Flag and the ON and OFF filter samples.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
537	If the Ignore Input flag is set, no input transition entries shall be placed into the Input Transition buffer.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
538	The ON and OFF filter samples shall determine the number of consecutive samples an input must be ON and OFF, respectively, before a change of state is recognized.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
539	If the change of state is shorter than the specified value, the change of state shall be ignored.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
540	The ON and OFF filter values shall be in the range of 0 to 255.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
541	A filter value of 0, for either or both values, shall result in no filtering for this input.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
542	The default values for input signals after reset shall be as follows: Filtering: Enabled: On and off filter values shall be set to: 5 Transition monitoring: Disabled (Timestamps are not logged)	**4.7.14 Inputs and Outputs**			Analysis	**Design**
543	Simultaneous assertion of all outputs shall occur within 100 microseconds.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
544	Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC.	**4.7.14 Inputs and Outputs**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>545</td><td>The condition of the outputs shall only be "ON" if the SIU continues to receive active communications from the ATC Controller Unit.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>546</td><td>If there is no valid communications with the ATC Controller Unit for 2.0 seconds, all outputs shall revert to the OFF condition, and the SIU status byte shall be updated to reflect the loss of communication from the ATC Controller Unit.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>547</td><td>The data and control bits in the ATC Controller Unit-SIU frame protocol shall control each output as follows:
Output Bit Translation
<table>
<tr><th>Case</th><th>Output Data Bit</th><th>Output Control Bit</th><th>Function</th></tr>
<tr><td>A</td><td>0</td><td>0</td><td>Output in the OFF state</td></tr>
<tr><td>B</td><td>1</td><td>1</td><td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.</td></tr>
<tr><td>C</td><td>0</td><td>1</td><td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF</td></tr>
<tr><td>D</td><td>1</td><td>0</td><td>Output is in the ON state.</td></tr>
</table></td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>548</td><td>In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>549</td><td>For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 microseconds after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>550</td><td>In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>551</td><td>All outputs shall never change state unless configured to do so.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>554</td><td>Communications circuitry shall be capable of 614.4 Kilobits per second of data pass through.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>555</td><td>Port 1 shall interface the SIU to Serial Bus 1 of the ITS cabinet Modular Bus Assemblies.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>556</td><td>All communications circuitry and protocol shall match Serial Bus 1 requirements.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>557</td><td>The SIU shall function as the “LOCAL” command node for this network responding with appropriate action.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>558</td><td>See ATC Controller Unit specification, CPU Field I/O, for protocol and requirements.</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>559</td><td>The SP5 SDLC frame address assignments (Command/Responses) are as follows:
<table>
<tr><th rowspan="2">Address</th><th rowspan="2">SYSTEM ASSEMBLY / UNIT</th><th colspan="8">SIU ADDRESS</th></tr>
<tr><th>A7</th><th>A6</th><th>A5</th><th>A4</th><th>A3</th><th>A2</th><th>A1</th><th>A0</th></tr>
<tr><td>0</td><td colspan="8">Reserved</td></tr>
<tr><td>1</td><td>14 Pack in position 1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>2</td><td colspan="8">Reserved</td></tr>
<tr><td>3</td><td>14 Pack in position 3</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>6 Pack in position 4</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>5</td><td>6 Pack in position 1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>6</td><td>6 Pack in position 2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>7</td><td>6 Pack in position 3</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>8</td><td colspan="8">Reserved</td></tr>
<tr><td>9</td><td>Input #1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>10</td><td>Input #2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11</td><td>Input #3</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>12</td><td>Input #4</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>13</td><td>Input #5</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>14</td><td colspan="8">Reserved</td></tr>
<tr><td>15</td><td>CMU #1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>16</td><td>CMU #2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>17</td><td>CMU #3</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>18</td><td>CMU #4</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>19</td><td>CPU</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>20</td><td>FI/O 2A or 8</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>21 to 254</td><td colspan="8">Reserved</td></tr>
<tr><td>255</td><td>Broadcast All</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note 1: A0 to A3 are Input to SIU with DC ground as common.
Note 2: 0 = open or ground false. 1= closed or ground true (shunted)</td><td>4.7.14 Inputs and Outputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
560	SIU Port 2 shall interface to Serial Bus 2 of the ITS cabinet Modular Bus Assemblies providing a communications path to the ATC Controller Unit for block data retrieval.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
561	No connection exists between SIU Port 1 and SIU Port 2.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
562	Similarly, no connection exists between SIU Port 2 and the microprocessor/controller unit.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
563	All data transfers between SIU Ports 1 and 2 shall be accomplished by the ATC Controller Unit. For example, data sent back may include monitor diagnostic status and communication status; input diagnostics status (detector sensor or isolator); and processed channel inputs data such as rate counts, occupancies, average speeds, speed classification and incident/presence.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
564	If the ATC Controller Unit is communicating via Logical Port SP3S, SIU Port 2 shall communicate in SDLC format and protocol, and the hardware requirements shall match Serial Bus 2 (synchronous TX/RX using TxC from the ATC Controller Unit CPU for common clocking).	**4.7.14 Inputs and Outputs**			Analysis	**Design**
565	If the ATC Controller Unit is communicating via Logical Port SP3, SIU Port 2 shall communicate in an asynchronous START BIT/STOP BIT format and protocol.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
566	The SIU Port 3 shall be provided for communication to a personal computer via a front panel 9-position subminiature D-type connector and EIA-232 logic.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
567	Its [SIU Port 3] purpose is to upload diagnostic information, and to download the SIU program.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
568	The SIU Port 3 protocol shall be defined by the vendor, and operate with vendor-supplied software.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
569	The pin assignments of SIU Port 3 shall match that of ATC Controller Unit C60 port.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
570	SIU Port 4 consists of Detector Rack signal INBUS TxD, INBUS RxD, INBUS TxC, and INBUS RxC, and shall conform to the electrical standards of EIA-485, single-ended.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
571	In this scheme, the RxD- and RxC- inputs of the EIA-485 receivers are connected to 2.5 Volts, while the TxD- and TxC- outputs of the EIA-485 drivers are not used.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
572	SIU Port 4 receivers shall withstand +/-25 Volts, suitable for reception of EIA-232 bipolar signals.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
573	All four INBUS signals shall be terminated at each receiver with impedance of 6,800 Ohms (+/-5%), connected from signal to +5V Ground on the SIU.	**4.7.14 Inputs and Outputs**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
574	The detector vendor shall define the SIU Port 4 messages.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
575	The detector vendor shall define the SIU Port 4 protocol.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
576	The SIU provides one inversion to ensure a controller MARK equates to a detector MARK.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
577	The SIU shall provide an LED indicator for TxD and RxD, such that is illuminated during a MARK (START Bit, for example) and extinguished during a SPACE (STOP Bit, for example).	**4.7.14 Inputs and Outputs**			Analysis	**Design**
578	SIU Port 4 provides the buffering to SIU Port 2, allowing the ATC Controller Unit to communicate directly to the detectors, as follows:	**4.7.14 Inputs and Outputs**				**Design**
579	If the ATC Controller Unit is communicating to detectors via Logical Port SP3S, the SIU Port 4 buffers shall convert SIU Port 2 TxD+ and TxD- to EIA-485 which shall then be transmitted to the detectors via INBUS TxD.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
580	Likewise, the SIU Port 4 buffers shall convert SIU Port 2 TxC+ and TxC- to EIA-485, which shall then be transmitted to the detectors via INBUS TxC.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
581	If the ATC Controller Unit is communicating to detectors via Logical Port SP3S, the SIU Port 4 buffers shall convert INBUS RxD from EIA-485, which shall then be transmitted to the ATC Controller Unit via SIU Port 2 RxD+ and RxD-.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
582	Likewise, the SIU Port 4 buffers shall convert INBUS RxC from EIA-485, which shall then be transmitted to the ATC Controller Unit via SIU Port 2 RxC+ and RxC-.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
583	If the ATC Controller Unit is communicating to detectors via Logical Port SP3, the SIU Port 4 buffers shall convert SIU Port 2 TxD+ and TxD- to EIA-485 which shall be transmitted to the detectors via INBUS TxD.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
584	If the ATC Controller Unit is communicating to detectors via Logical Port SP3, the SIU Port 4 buffers shall convert INBUS RxD is from EIA-485, which shall be transmitted to the ATC Controller Unit via SIU Port 2 RxD+ and RxD-.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
585	Asynchronous operation shall not use Port 2 TxC+, TxC-, RxC+, RxC-, nor Port 4 INBUS TxC, or INBUS RxC.	**4.7.14 Inputs and Outputs**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
586	The SIU shall sense the rack address block and generate a square wave on the ASSEMBLY ADDRESS signal as follows: *ASSEMBLY ADDRESS* — *ASSEMBLY ADDRESS FREQUENCY (Hertz)(+/-15%)* 1 — 60 2 — 30 3 — 15 4 — 7.5 5 — 3.75	**4.7.14 Inputs and Outputs**			Analysis	**Design**
587	The INBUS RTS line shall be pulled to +24 Volts via a 10K Ohm resistor on the SIU.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
588	In systems using legacy detectors that do not use INBUS RTS, this line [INBUS RTS] shall not be used (no connection).	**4.7.14 Inputs and Outputs**			Analysis	**Design**
589	Detectors equipped with INBUS RTS shall drive this line low when transmitting data from that detector to the SIU via INBUS.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
590	When not transmitting data, this line shall not be driven low and is pulled to +24V via the 10K Ohm resistor.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
591	The controller transmits a message on Serial Bus 2 which shall be received by each detector via the SIU INBUS TxD and INBUS TxC.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
592	If the detector is asynchronous, INBUS TxC shall be ignored.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
593	Each detector shall compare the address field of the message with its own slot address and assembly address.	**4.7.14 Inputs and Outputs**			Analysis	**Design**
594	If the address matches, that detector shall respond with data on INBUS RxD and INBUS RxC.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
595	If the detector is asynchronous, INBUS RxC shall not be used.	**4.7.14 Inputs and Outputs**			Inspection	**Design**
596	The SIU of the responding detector shall enable its EIA-485 line drivers to transmit the response from INBUS to SB2.	**4.7.14 Inputs and Outputs**			Performance Test	**Design**
597	This driver [Serial Bus 2 Control] shall be enabled by any of the three following conditions: Activity on INBUS RxD Activity on INBUS RxC INBUS RTS at low (true)	**4.7.14 Inputs and Outputs**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
598	This driver [Serial Bus 2 Control] shall be disabled by either of the following two conditions: Lack of activity on both INBUS RxD and RxC for 1.5 milliseconds Inbus RTS transitions from low (true) to high (false)	**4.7.14 Inputs and Outputs**			Analysis	**Design**
599	All communication with the ATC Controller Unit shall be SDLC-compatible command-response protocol, support 0-bit stuffing, and operate at a data rate of 614.4 Kilobits per second.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
600	The ATC Controller Unit shall always initiate the communication and should the command frame be incomplete or in error, no SIU response shall be transmitted.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
601	There is no requirement for a Command message Queue that results in a response stream of messages.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
602	An incoming Command Message may abort a planned response or truncate a response already in progress.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
603	Command Frame Errors shall include Microprocessor identified abnormalities, such as CRC errors, bit alignment or bit stuffing problems.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
604	Message irregularities shall include unknown Message numbers or improper command lengths.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
605	The frame type shall be determined by the value of the first byte of the message.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
606	The command frames type values $70 - $7F and associated response frame type values $F0 - $FF are allocated to the Manufacturer diagnostics.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
607	All other frame types not called out are reserved.	**4.7.15 Data Communications Protocol**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>608</td><td>The command-response Frame Type values and message times shall be as follows:
Frame Types
<table>
<tr><th>Module Command</th><th>I/0 Module Response</th><th>Description</th><th>Minimum Message Time</th><th>Maximum Message Time</th></tr>
<tr><td>49</td><td>177</td><td>Request Module Status</td><td>250 microseconds</td><td>275 microseconds</td></tr>
<tr><td>50</td><td>178</td><td>MILLISECOND CTR. Mgmt.</td><td>222.5 microseconds</td><td>237.5 microseconds</td></tr>
<tr><td>51</td><td>179</td><td>Configure Inputs</td><td>344.5 microseconds</td><td>6.8750 milliseconds</td></tr>
<tr><td>52</td><td>180</td><td>Poll Raw Input Data</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>53</td><td>181</td><td>Poll Filtered Input Data</td><td>317.5 microseconds</td><td>320 microseconds</td></tr>
<tr><td>54</td><td>182</td><td>Poll Input Transition Buffer</td><td>300 microseconds</td><td>10.25 milliseconds</td></tr>
<tr><td>55</td><td>183</td><td>Command Outputs</td><td>405 microseconds</td><td>410 microseconds</td></tr>
<tr><td>56</td><td>184</td><td>Config. Input Tracking Functions</td><td>340 microseconds</td><td>10.25 milliseconds</td></tr>
<tr><td>57</td><td>185</td><td>Config. Complex Output Functions</td><td>340 microseconds</td><td>6.875 milliseconds</td></tr>
<tr><td>58</td><td>186</td><td>Reserved</td><td>---</td><td>---</td></tr>
<tr><td>59</td><td>187</td><td>Reserved</td><td>---</td><td>---</td></tr>
<tr><td>60</td><td>188</td><td>SIU Identification</td><td>222.5 microseconds</td><td>222.5 microseconds</td></tr>
<tr><td>61-62</td><td>189-190</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
<tr><td>63</td><td>191</td><td>Reserved</td><td>---</td><td>---</td></tr>
<tr><td>64</td><td>192</td><td>Reserved</td><td>---</td><td>---</td></tr>
<tr><td>65</td><td>193</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
<tr><td>66</td><td>---</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
<tr><td>67</td><td>195</td><td>Reserved (note below)</td><td>---</td><td>---</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>609</td><td>Messages 61/189, 62/190, 65/193, and 67/195 shall be for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 (section 25) for Command and Response Frames. Message 66/No Response is a Broadcast Message to Address 255 containing the current time. Any device may receive and process this message if it has the software capacity.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>610</td><td>The Command [Request Mode Status] shall be used to request SIU status information response.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>611</td><td>Command/Response frames shall be as follows:
Request Module Status Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 49)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Reset Status Bits</td><td>P</td><td>E</td><td>K</td><td>R</td><td>T</td><td>M</td><td>L</td><td>W</td><td>Byte 2</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>612</td><td>Request Module Status Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 177)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>System Status</td><td>P</td><td>E</td><td>K</td><td>R</td><td>T</td><td>M</td><td>L</td><td>W</td><td>Byte 2</td></tr>
<tr><td>SCC Receive Error Count</td><td colspan="8">Receive Error Count</td><td>Byte 3</td></tr>
<tr><td>SCC Transmit Error Count</td><td colspan="8">Transmit Error Count</td><td>Byte 4</td></tr>
<tr><td>MC Timestamp MSB</td><td colspan="8">MC Timestamp MSB</td><td>Byte 5</td></tr>
<tr><td>MC Timestamp NMSB</td><td colspan="8">MC Timestamp NMSB</td><td>Byte 6</td></tr>
<tr><td>MC Timestamp NLSB</td><td colspan="8">MC Timestamp NLSB</td><td>Byte 7</td></tr>
<tr><td>MC Timestamp LSB</td><td colspan="8">MC Timestamp LSB</td><td>Byte 8</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>613</td><td>The response status bits are defined as follows:
P - Indicates SIU hardware reset
E - Indicates a communications loss of greater than two seconds
M - Indicates an error with the Millisecond Counter interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the SIU has been reset by the Watchdog
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
K - Not Used</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>614</td><td>Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>615</td><td>The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>616</td><td>The Millisecond Counter Management Frame shall be used to set the value of the Millisecond Counter.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>617</td><td>The 'S' bit shall return status '0' on completion or '1' on error.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>618</td><td>The 32-bit value shall be loaded into the Millisecond Counter at the next 0-1 transition of the LINESYNC signal.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>619</td><td>The frames shall be as follows:
Millisecond Counter Management Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 50)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>New MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>New MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>New MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 4</td></tr>
<tr><td>New MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 5</td></tr>
</table>
Millisecond Counter Management Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 178)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>S</td><td>Byte 2</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>620</td><td>The Configure Inputs command frame shall be used to change input configurations.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>621</td><td>The command-response frames shall be as follows:
Configure Inputs Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 51)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Number of Items (n)</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>n</td><td>Byte 2</td></tr>
<tr><td>Item # - Byte 1</td><td>E</td><td colspan="7">Input Number (I0 – I59)</td><td>Byte 3(I-1)+3</td></tr>
<tr><td>Item # - Byte 2</td><td colspan="8">Leading edge filter (e)</td><td>Byte 3(I-1)+4</td></tr>
<tr><td>Item # - Byte 3</td><td colspan="8">Trailing edge filter (r)</td><td>Byte 3(I-1)+5</td></tr>
</table>
NOTE: In the case of an invalid parameter error, the entire message shall be rejected.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>622</td><td>Configure Inputs Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 179)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>S</td><td>Byte 2</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>623</td><td>Block field definitions shall be as follows:
E - Ignore Input Flag. "1" = do not record transition entries for this input, "0" = record transition entries for this input
e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = filtering disabled)
r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = filtering disabled)
S - return status S = '0' on completion or '1' on error</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>624</td><td>The Poll Raw Input Data frame shall be used to poll the SIU for the current unfiltered status of all inputs.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>625</td><td>The response frame shall contain 8 bytes (Inputs 0-63) of information indicating the current input status.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>626</td><td>The frames shall be as follows:
Poll Raw Input Data Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 52)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
</table>
Poll Raw Input Data Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 180)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I53, I56 to I59</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 9</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 10</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 11</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 12</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 13</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>627</td><td>The Poll Filtered Input Data frame shall be used to poll the SIU for the current filtered status of all inputs.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>628</td><td>The response frame shall contain 8 bytes (Inputs 0-63) of information indicating the current filtered status of the inputs.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>629</td><td>Raw input data shall be provided in the response for inputs that are not configured for filtering.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>630</td><td>The frames shall be as follows:
Poll Filter Input Data Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 53)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Byte 1</td></tr>
</table>
Poll Filter Input Data Response
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 181)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Inputs I0 (lsb) to I7 (msb)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Inputs I8 to I53, I56 to I59</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 9</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 10</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 11</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 12</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 13</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>631</td><td>The Poll Input Transition Buffer frame shall poll the SIU for the contents of the input transition buffer.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>632</td><td>The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>633</td><td>The frames are as follows:
Poll Input Transition Buffer Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 54)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Block Number</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table>
Poll Input Transition Buffer Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 182)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Block Number</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Number of Entries = N</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>Item #</td><td>S</td><td colspan="7">Input Number (I0 – I59)</td><td>Byte 3(I-1)+4</td></tr>
<tr><td>Item # MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+5</td></tr>
<tr><td>Item # MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(I-1)+6</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C</td><td>F</td><td>E</td><td>G</td><td>Byte 3(I-1)+7</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(N-1)+8</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(N-1)+9</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(N-1)+10</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3(N-1)+11</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>634</td><td>Each detected state transition for each active input (see 4.7.9 and 4.7.15.4) is placed in the queue as it occurs.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>635</td><td>Bit definitions are as follows:
S - Indicates the state of the input after the transition, bit is 1 if the Input is ON after the transition, bit is 0 if the Input is OFF after the transition
C - Indicates the 255 entry buffer limit has been exceeded
F - Indicates the 1024 buffer limit has been exceeded
G - Indicates the requested block number is out of monotonic increment sequence
E - Same block number requested, E is set in response</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
636	The entries provided within the Transition Buffer Poll response shall be ordered from the start of the reply as the oldest to newest.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
637	The very first access provides the oldest entry.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
638	The SIU device shall initialize, upon Power Up or Reset, its last Block Number received value to 0xFF in order to facilitate suppression of the G Bit response when the ATC Controller Unit program starts and uses 0x00 as the first Block Number.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
639	Subsequent responses are subject to the old-buffer purge mechanism stated below.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
640	The ATC Controller Unit program monotonically increases the Block Number after each command issued to purge the old buffer.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
641	When the SIU Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
642	If it [the latest command received by the SIU Module] is the same [as the previous command received by the SIU Module], the previous buffer shall be re-sent to the ATC Controller Unit and the 'E' flag set in the status response frame.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
643	If it [the latest command received by the SIU Module] is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
644	If the block number is not incremented by one, the status G bit shall be set.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
645	The block number received becomes the current number (even if out of sequence).	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
646	The Block Number byte sent in the response block shall be the same as that received in the command block.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>647</td><td>The Set Outputs frame shall be used to command the SIU to set the Outputs according to the data in the frame.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>648</td><td>If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>649</td><td>If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>650</td><td>Loss of LINESYNC reference shall also be indicated in system status information.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>651</td><td>These command and response frames are as follows:
Set Outputs Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 55)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Outputs O0 (lsb) to O7 (msb) Data</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
<tr><td>Outputs O8 to O54 Data</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 3 to 8</td></tr>
<tr><td>Outputs O56 to O63 Data (reserved)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Byte 9</td></tr>
<tr><td>Outputs O0 (lsb) to O7 (msb) Control</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 10</td></tr>
<tr><td>Outputs O8 to O54 Control</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Bytes 11 to 16</td></tr>
<tr><td>Outputs O56 to O63 Control (reserved)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Byte 17</td></tr>
</table>
Set Outputs Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 183)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>L</td><td>E</td><td>Byte 2</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>652</td><td>The Configure Input Tracking Functions frame shall be used to configure the definition for an output that responds to transitions on a particular input. The maximum number of active definitions is 8. Refer to ‘Tracking Functions Overview’ for additional details.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>653</td><td>Please note that Configure Input Tracking Functions is not intended for use with Traffic Signal Control Applications. (Authorized Engineering Information)</td><td>4.7.15 Data Communications Protocol</td><td></td><td>What value does this specification add to the standard?</td><td>Analysis</td><td>Design</td></tr>
<tr><td>654</td><td>The command and response frames for Input Tracking Functions shall be as follows:
Configure Input Tracking Functions Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 56)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Number of Items</td><td colspan="8">Number of Items</td><td>Byte 2</td></tr>
<tr><td>Item # - Byte 1</td><td>E</td><td colspan="7">Output Number (O0 – O54)</td><td>Byte 2(I-1)+3</td></tr>
<tr><td>Item # - Byte 2</td><td>I</td><td colspan="7">Input Number (I0 – I59)</td><td>Byte 2(I-1)+4</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>655</td><td>Number of Items: 0-16 Tracking Definitions are contained in this message.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>656</td><td>Field Definitions:
E '1’ - Enable Input Tracking function for this Output
'0' - Remove Input Tracking function for this Output
I '1' - Output is OFF when Input is ON, ON when Input OFF
'0' - Output is ON when Input is ON, OFF when Input is OFF</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>657</td><td>Output Number: 0 - Maximum Output Number for the SIU device type.
Input Number: 0 - Maximum Input Number for the SIU device type.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>658</td><td>Configure Input Tracking Functions Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 184)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>V</td><td>Byte 2</td></tr>
<tr><td>MC Timestamp MSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>MC Timestamp NMSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 4</td></tr>
<tr><td>MC Timestamp NLSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 5</td></tr>
<tr><td>MC Timestamp LSB</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 6</td></tr>
</table>
Field Definitions:
V '1' - Maximum number of configurable outputs will be exceeded.
'0' - No error</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>659</td><td>The timestamp value shall be sampled prior to the response frame.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>660</td><td>Outputs, which track inputs, shall be updated no less than once per millisecond. Input to output signal propagation delay shall not exceed 2 milliseconds.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>661</td><td>A maximum of eight different [Tracking Functions] Output numbers may be activated by specifying eight definitions.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>662</td><td>One complete definition for an Output that tracks an Input consists of two bytes containing four parameters: 1) the instruction to install or to remove the definition, 2) the Output Number, 3) the relationship of the state of the Output to the Input and 4) the Input Number.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>663</td><td>Each definition specifies the controlling Input number for that unique output number.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>664</td><td>More than one output definition may specify the same Input controlling source. [That is, the same input may be used as the control source for more than one Tracking Output.]</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>665</td><td>A complete definition [of an Output that tracks an Input] is called an Item in the Command Message frame.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
666	The 'Number of Items' byte specifies the quantity of complete definitions contained in the Command Frame.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
667	If the value is 0, all existing active Input Tracking definitions shall be removed.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
668	The transmission of a definition may: a) Install a new active Tracking definition. b) Remove an existing active Tracking definition. When an Input Tracking definition is removed, the output is set according to the most recently received Set Outputs Command. c) Convert an active output definition from Complex or Square Wave definition to Tracking. Conversion removes the existing definition and assigns the Tracking definition without a transition through the 'output is set according to the most recently received Set Outputs Command' state. The most recent state of the output remains until the new function changes it. d) Redefine an existing Tracking definition.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
669	If a command frame to be processed by the SIU would result in having more than the maximum number (8) of definitions activated, the entire command frame shall be rejected.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
670	[After an entire command frame is rejected due to having more than the maximum number of definitions activated,] The response V bit shall be set to 1.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
671	The V bit response is based on counting the current active quantity plus the projected Enable definitions after accounting for Remove definitions and invalid Output numbers.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
672	The V bit response evaluation takes the currently active definition quantity, adds the projected Enable definitions, subtracts the Remove definitions, ignores invalid Input and Output numbers and compares the result to the Maximum Number of active Tracking definitions allowed.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
673	If the quantity of Active definitions would become greater than the Maximum Number of active Tracking definitions, or if there are more Remove definitions than existing active definitions, the V Bit shall be set in the response.	**4.7.15 Data Communications Protocol**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
674	While processing an Enable request, an Out of Range Input number shall preclude processing for that definition.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
675	The Out of Range Output and Input numbers shall not affect the active definition count.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
676	No error response is returned.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
677	The rest of the message shall be processed.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
678	The "Number of Items" field is valid from 0 to 16 because the longest message may contain 8 Enable and 8 Remove definitions.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
679	The Input state always comes from the Filtered Input Data source.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
680	Valid Input and Output Number Ranges: ITS SIU device types: Inputs 0 - 53 & 56 - 59, Outputs 0 – 54	**4.7.15 Data Communications Protocol**			Analysis	**Design**
681	The Configure Complex Output Functions frame shall be used to configure the definition for an output that provides a complex operation.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
682	The maximum number of active definitions is 8. Refer to 'Complex Output Functions Overview' for additional details.	**4.7.15 Data Communications Protocol**		It is unclear what the implementer should gather by referring to 'Complex Output Functions Overview'.	Analysis	**Design**
683	Please note that Configure Complex Output Functions is not intended for use with Traffic Signal Control Applications. (Authorized Engineering Information)	**4.7.15 Data Communications Protocol**		It is unclear what this requirement means.	Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>684</td><td>The command and response frames shall be as follows:
Configure Complex Output Functions Command
<table>
<tr><th>Description</th><th colspan="8">msb lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 57)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Number of Items</td><td colspan="8">Number of Items</td><td>Byte 2</td></tr>
<tr><td>Item # - Byte 1</td><td>0</td><td colspan="7">Output Number (O0 – O54)</td><td>Byte 7(I-1)+3</td></tr>
<tr><td>Item # - Byte 2</td><td colspan="8">Primary Duration (MSB)</td><td>Byte 7(I-1)+4</td></tr>
<tr><td>Item # - Byte 3</td><td colspan="8">Primary Duration (LSB)</td><td>Byte 7(I-1)+5</td></tr>
<tr><td>Item # - Byte 4</td><td colspan="8">Secondary Duration (MSB)</td><td>Byte 7(I-1)+6</td></tr>
<tr><td>Item # - Byte 5</td><td colspan="8">Secondary Duration (LSB)</td><td>Byte 7(I-1)+7</td></tr>
<tr><td>Item # - Byte 6</td><td>0</td><td colspan="7">Input Number (I0 – I59)</td><td>Byte 7(I-1)+8</td></tr>
<tr><td>Item # - Byte 7</td><td>P</td><td>W</td><td>G</td><td>E</td><td>J</td><td>F</td><td>R</td><td>L</td><td>Byte 7(I-1)+9</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>685</td><td>Number of Items: 0-16 Complex Output Definitions are contained in this message.
Output Number: 0 - Maximum Output Number for the SIU device type.
Primary Duration: MSB & LSB form a 16 bit Hex numerical value 0x0000 - 0xffff.
Secondary Duration: MSB & LSB form a 16 bit Hex numerical value 0x0000 - 0xffff.
Input Number: 0 - Maximum Input Number for the SIU device type.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
686	Field Definitions: P '1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled. '0' - The output is configured for continuous oscillation. W '1' - It is triggered by the specified input. Triggered complex output shall commence within 2 milliseconds of the associated trigger recognition. '0' - Operation shall begin within two milliseconds of the command receipt. G '1' - Operation shall be gated active by the specified input. '0' - Gating is inactive. E '1' Enable complex output function for this output '0' Remove complex output function for this output J '1' During primary duration, the output shall be written as a logic '1'. During secondary duration, the output shall be written as a logic '0'. '0' During primary duration, the output shall be written as a logic '0'. During secondary duration, the output shall be written as a logic '1' F '1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input. '0' - The trigger or gate shall be derived from the raw input. R '1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF. '0' - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON. L '1' - The LINESYNC based clock shall be used for the time ticks. '0' - The Millisecond Counter shall be used for the time ticks.	**4.7.15 Data Communications Protocol**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>687</td><td>Configure Complex Output Functions Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number = 185)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Byte 1</td></tr>
<tr><td>Status</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>V</td><td>Byte 2</td></tr>
<tr><td>MC Timestamp (MSB)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 3</td></tr>
<tr><td>MC Timestamp (NMSB)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 4</td></tr>
<tr><td>MC Timestamp (NLSB)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 5</td></tr>
<tr><td>MC Timestamp (LSB)</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 6</td></tr>
</table>
Field Definitions:
V '1' - Maximum number of configurable outputs will be exceeded.
'0' - No error</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>688</td><td>Controlling input signals shall be sampled at least once per millisecond.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>689</td><td>A maximum of eight different Output numbers may be activated by specifying eight definitions.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>690</td><td>One complete definition for a Complex Output consists of seven bytes containing fourteen parameters:
1) the Output Number,
2, 3) Primary Duration: MSB & LSB form a 16 bit Hex numerical value,
4, 5) Secondary Duration: MSB & LSB form a 16 bit Hex numerical value,
6) the Input Number,
7) Bit P: One Pulse or Continuous Oscillation,
8) Bit W: Output Operation is Edge Triggered by Input or Not Triggered by Input,
9) Bit G: Output Operation is Gated by Input or is Continuous Oscillation,
10) Bit E: Enable Definition or Remove Definition,
11) Bit J: Defines Primary/Secondary Duration relationship: ON/OFF or OFF/ON,
12) Bit F: Input from Filtered or Raw Data,
13) Bit R: Selects Edge for Triggered by Input ON to OFF or OFF to ON. Bit R: Selects State for Gated to be active by Input OFF or by Input ON,
14) Linesync edges or Millisecond Counter provides tick timing.</td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
691	Each definition [of a Complex Output] specifies the controlling Input number for that unique output number.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
692	The Input is a functional control only when the operation is specified as Triggered (W=1) or Gated (G=1).	**4.7.15 Data Communications Protocol**			Analysis	**Design**
693	Otherwise [when the Input is not functional], the Input number is ignored.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
694	More than one output definition may specify the same Input controlling source. [That is, the same input may be used as the control source for more than one Complex Output.]	**4.7.15 Data Communications Protocol**			Analysis	**Design**
695	If both W=1 and G=1 are set in the definition, the G=1 shall be used as if W=0.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
696	The primary duration is the first timed interval of a pulse or the first portion of a continuous oscillation.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
697	The first portion [of a continuous oscillation] follows acquisition of a Trigger or Gated Input. If not Triggered or Gated, the first portion follows the activation of the definition.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
698	The 'Number of Items' byte specifies the quantity of complete definitions contained in the Command Frame.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
699	If the value is 0, all existing active Complex Output definitions shall be removed.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
700	The transmission of a definition may: a) Install a new active Complex Output definition. b) Remove an existing active Complex Output definition. When a Complex Output definition is removed, the output is set according to the most recently received Set Outputs Command. c) Convert an active output definition from Tracking or Square Wave definition to Complex Output. Conversion removes the existing definition and assigns the Complex Output definition without a transition through the 'output is set according to the most recently received Set Outputs Command' state. The most recent state of the output remains until the new function changes it. d) Redefine an existing Complex Output definition.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
701	If a command frame to be processed by the SIU would result in having more than the maximum number (8) definitions activated, the entire command frame shall be rejected.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
702	[After a command frame has been rejected,] The response V bit shall be set to 1.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
703	The V bit response evaluation takes the currently active definition quantity, adds the projected Enable definitions, subtracts the Remove definitions, ignores invalid Input and Output numbers and compares the result to the maximum number of active Complex definitions allowed.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
704	If the quantity of active definitions would become greater than the maximum number of active Complex Output definitions, or if there are more Remove definitions than existing active Complex Output definitions, the V Bit shall be set in the response.	**4.7.15 Data Communications Protocol**			Performance Test	**Design**
705	While processing an Enable request that requires Triggered or Gated operation, an Out of Range Input number shall preclude processing for that definition.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
706	The Out of Range Output and Input numbers shall not affect the active definition count. No error response is returned.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
707	The rest of the message shall be processed.	**4.7.15 Data Communications Protocol**			Analysis	**Design**

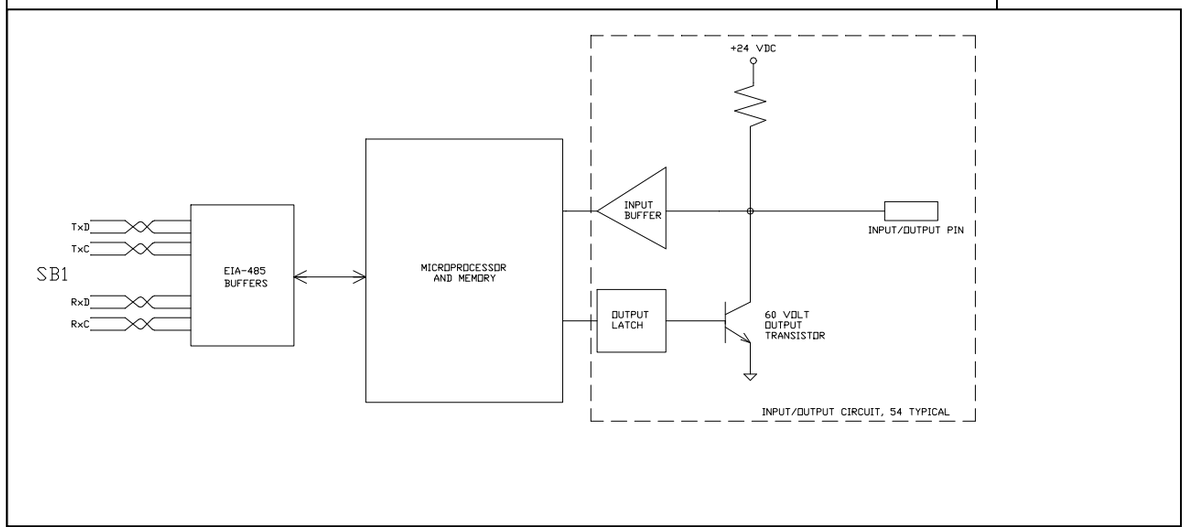
#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
708	The "Number of Items" field is valid from 0 to 16 because the longest message may contain 8 Enable and 8 Remove definitions.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
709	The Input state comes from the Filtered or Raw Input Data source as specified by the Bit F value.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
710	Valid Input and Output Number Ranges: ITS SIU device types: Inputs 0 - 53 & 56 - 59, Outputs 0 – 54	**4.7.15 Data Communications Protocol**			Analysis	**Design**
711	The LINESYNC based clock shall used both the rising and falling edges providing a nominal 8.33 millisecond time tick.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
712	The SIU Identification command frame shall be used to request the SIU Identification value for ITS Cabinet SIUs and CMUs.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
713	Reply message shall use the following addresses: ATC Controller Unit Field I/Os shall respond with address 20.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
714	SIUs respond with their own address ranging from 0-14.	**4.7.15 Data Communications Protocol**			Analysis	**Design**
715	CMUs respond with their own addresses, ranging from 15-18.	**4.7.15 Data Communications Protocol**			Analysis	**Design**

<table>
<tr><th>#</th><th>Requirement (Standard Document Section)</th><th>Document Section</th><th><u>Pass</u>
Fail</th><th>Comments</th><th>Type</th><th>Requirement Type</th></tr>
<tr><td>716</td><td>The command and response frames shall be shown as follows:
I/O Module Identification Command
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number= 60)</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
</table>
I/O Module Identification Response
<table>
<tr><th>Description</th><th>msb</th><th></th><th></th><th></th><th></th><th></th><th></th><th>lsb</th><th>Byte Number</th></tr>
<tr><td>(Type Number= 188)</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Byte 1</td></tr>
<tr><td>SIU I D byte</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Byte 2</td></tr>
</table></td><td>4.7.15 Data Communications Protocol</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>717</td><td>The Address Select input bits shall define the logical position of each SIU.</td><td>4.7.16 Address Select Inputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>718</td><td>No connection shall be logical False, while a connection to Logic Ground shall be a logical True.</td><td>4.7.16 Address Select Inputs</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>719</td><td>There shall be sixteen unique address positions selected with a binary code, using bit 0 as least significant and bit 3 as most significant.</td><td>4.7.16 Address Select Inputs</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>720</td><td>The SIU shall contain one input that shall be read directly by microprocessor.</td><td>4.7.17 SIU/BIU Input</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>721</td><td>When not connected, this input shall be logical False, while a connection to Ground shall be a logical True.</td><td>4.7.17 SIU/BIU Input</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>725</td><td>The Serial Bus 1 indicators shall be sensed on the microprocessor/controller pins.</td><td>4.7.18 Hardware Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>726</td><td>Serial Bus 2 indicators shall be sensed on the Port 4 (EIA-485) signal lines.</td><td>4.7.18 Hardware Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>727</td><td>The SIU Power LED shall indicate that the +24 VDC power supply is within regulation.</td><td>4.7.18 Hardware Requirements</td><td></td><td></td><td>Performance Test</td><td>Design</td></tr>
<tr><td>728</td><td>The SIU Active LED shall be controlled via SIU I/O 55.</td><td>4.7.18 Hardware Requirements</td><td></td><td></td><td>Analysis</td><td>Design</td></tr>
<tr><td>730</td><td>A 9-position subminiature D-type connector shall be mounted on the front panel for Port 3 entry.</td><td>4.7.18 Hardware Requirements</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
<tr><td>731</td><td>The connector pin assignment is Pin 2- RxD, Pin 3- TxD and Pin 5- Signal Ground.</td><td>4.7.18 Hardware Requirements</td><td></td><td></td><td>Inspection</td><td>Design</td></tr>
</table>

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
732	The SIU Input Connection pin assignments shall be as shown in drawing 4-11-8.	**4.7.18 Hardware Requirements**			Analysis	**Design**
733		**4.7.19 SIU Input and Output Assignments**			Analysis	**Design**

SIU	*Set Output Command Type 55*		*Raw Input Data Response Type 180*	
I/O 0	BYTE 2	BIT 0	BYTE 2	BIT 0
I/O 1	BYTE 2	BIT 1	BYTE 2	BIT 1
I/O 2	BYTE 2	BIT 2	BYTE 2	BIT 2
I/O 3	BYTE 2	BIT 3	BYTE 2	BIT 3
I/O 4	BYTE 2	BIT 3	BYTE 2	BIT 4
I/O 5	BYTE 2	BIT 5	BYTE 2	BIT 5
I/O 6	BYTE 2	BIT 6	BYTE 2	BIT 6
I/O 7	BYTE 2	BIT 7	BYTE 2	BIT 7
I/O 8	BYTE 3	BIT 0	BYTE 3	BIT 0
I/O 9	BYTE 3	BIT 1	BYTE 3	BIT 1
I/O 10	BYTE 3	BIT 2	BYTE 3	BIT 2
I/O 11	BYTE 3	BIT 3	BYTE 3	BIT 3
I/O 12	BYTE 3	BIT 4	BYTE 3	BIT 4
I/O 13	BYTE 3	BIT 5	BYTE 3	BIT 5
I/O 14	BYTE 3	BIT 6	BYTE 3	BIT 6
I/O 15	BYTE 3	BIT 7	BYTE 3	BIT 7
I/O 16	BYTE 4	BIT 0	BYTE 4	BIT0
I/O 17	BYTE 4	BIT 1	BYTE 4	BIT1
I/O 18	BYTE 4	BIT 2	BYTE 4	BIT2
I/O 19	BYTE 4	BIT 3	BYTE 4	BIT3
I/O 20	BYTE 4	BIT 4	BYTE 4	BIT4
I/O 21	BYTE 4	BIT 5	BYTE 4	BIT5
I/O 22	BYTE 4	BIT 6	BYTE 4	BIT6
I/O 23	BYTE 4	BIT 7	BYTE 4	BIT7
I/O 24	BYTE 5	BIT0	BYTE 5	BIT 0
I/O 25	BYTE 5	BIT1	BYTE 5	BIT 1
I/O 26	BYTE 5	BIT2	BYTE 5	BIT 2
I/O 27	BYTE 5	BIT3	BYTE 5	BIT 3
I/O 28	BYTE 5	BIT4	BYTE 5	BIT 4
I/O 29	BYTE 5	BIT5	BYTE 5	BIT 5
I/O 30	BYTE 5	BIT6	BYTE 5	BIT 6
I/O 31	BYTE 5	BIT7	BYTE 5	BIT 7

#	Requirement (Standard Document Section)				Document Section	Pass / Fail	Comments	Type	Requirement Type
	I/O 32	BYTE 6	BIT0	BYTE 6 BIT 0					
	I/O 33	BYTE 6	BIT1	BYTE 6 BIT 1					
	I/O 34	BYTE 6	BIT2	BYTE 6 BIT 2					
	I/O 35	BYTE 6	BIT3	BYTE 6 BIT 3					
	I/O 36	BYTE 6	BIT4	BYTE 6 BIT 4					
	I/O 37	BYTE 6	BIT5	BYTE 6 BIT 5					
	I/O 38	BYTE 6	BIT6	BYTE 6 BIT 6					
	I/O 39	BYTE 6	BIT7	BYTE 6 BIT 7					
	I/O 40	BYTE 6	BIT0	BYTE 6 BIT 0					
	I/O 41	BYTE 7	BIT1	BYTE 7 BIT 1					
	I/O 42	BYTE 7	BIT2	BYTE 7 BIT 2					
	I/O 43	BYTE 7	BIT3	BYTE 7 BIT 3					
	I/O 44	BYTE 7	BIT4	BYTE 7 BIT 4					
	I/O 45	BYTE 7	BIT5	BYTE 7 BIT 5					
	I/O 46	BYTE 7	BIT6	BYTE 7 BIT 6					
	I/O 47	BYTE 7	BIT7	BYTE 7 BIT 7					
	I/O 48	BYTE 8	BIT0	BYTE 8 BIT 0					
	I/O 49	BYTE 8	BIT1	BYTE 8 BIT 1					
	I/O 50	BYTE 8	BIT2	BYTE 8 BIT 2					
	I/O 51	BYTE 8	BIT3	BYTE 8 BIT 3					
	I/O 52	BYTE 8	BIT4	BYTE 8 BIT 4					
	I/O 53	BYTE 8	BIT5	BYTE 8 BIT 5					
	Active LED (O54)	BYTE 8	BIT6						
	Opto Input 1 (I56)			BYTE 9 BIT 0					
	Opto Input 2 (I57)			BYTE 9 BIT 1					
	Opto Input 3 (I58)			BYTE 9 BIT 2					
	Opto Input 4 (I59)			BYTE 9 BIT 3					
	A000			BYTE 9 BIT 4					
	A001			BYTE 9 BIT 5					
	A002			BYTE 9 BIT 6					
	A003			BYTE 9 BIT 7					

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
734	Each SIU shall contain 54 Input/Outputs and each shall be connected as follows:  **Exhibit 4-1.** SIU Input/Output Connections	**4.7.20 Block Diagrams**			Analysis	**Design**
735	When the SIU is powered, all outputs shall be initialized OFF and fifty-four inputs shall be available.	**4.7.20 Block Diagrams**			Analysis	**Design**
737	Each output must be able to be read back as an input in order to check integrity.	**4.7.20 Block Diagrams**			Performance Test	**Design**
443	The SIU shall be capable of processing fifty-four Input/Output pins and four Optical Input pins.	**4.7.1 General**	P	Verified via the SIU Input monitoring program running on a laptop.	Inspection	**Performance**
444	When installed in an ITS Input Assembly, it [the SIU] processes twenty-four detector outputs (pins F and W), twenty-four detector status outputs, and provides six detector reset signals (per two slots).	**4.7.1 General**	P	Verified by analysis of the drawing.	Inspection	**Performance**
552	The SIU shall have a minimum of four serial ports, identified as SIU Ports 1-4.	**4.7.14 Inputs and Outputs**	F	The specification is discrepant, since the “ports” are neither properly identified nor labeled on the drawings as shown in the standard.	Inspection	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
553	Serial Ports 1 and 3 are connected to the SIU microprocessor/controller unit, while Serial Ports 2 and 4 provide a buffered communications path from the ATC Controller Unit to the detectors, and are not connected to the microprocessor/controller unit.	**4.7.14 Inputs and Outputs**	F	The words "port" is discrepant as well, as per above.	Inspection	**Performance**
722	The SIU Module shall be physically composed of a printed circuit board, 4.5 inches high by 6.5 inches long, a front panel 2.25 inches wide by 4.5 inches high with a DIN 96-pin connector on the connector end (opposite the front panel).	**4.7.18 Hardware Requirements**	P		Inspection	**Performance**
723	A "U" handle shall be mounted on the front panel for insertion/extraction.	**4.7.18 Hardware Requirements**	P		Inspection	**Performance**
724	Six LED indicators shall be provided on the front panel, as follows: SIU Active SIU Power Serial Bus 1 TxD Serial Bus 2 TxD Serial Bus 1 RxD Serial Bus 2 RxD	**4.7.18 Hardware Requirements**	P	We saw two different implementations of this, because the standard shows two different implementations, one on the drawing and one in this clause of the standard.	Inspection	**Performance**
729	The SIU front panel shall provide a RESET pushbutton that shall provide a hardware RESET to the microprocessor/controller unit.	**4.7.18 Hardware Requirements**	P	Verified during previous tests.	Inspection	**Performance**
736	Without jumpers or firmware changes, the Controller software shall be able to turn ON any of the fifty-four outputs.	**4.7.20 Block Diagrams**	P	Verified via an emulation program running on a remote control. Stepped through all channels available in the Cabinet we had, which only had 14 channels.	Performance Test	**Performance**

B.21 ITS Cabinet Loop Detector General Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
738	The sensor and isolator channels shall be operationally independent from each other.	**5.1 General Requirements**			Analysis	**Design**
739	Each sensor unit or AC isolator channel shall draw no more than 100 milliamperes from the +24 VDC cabinet power supply and shall be insensitive to 700 millivolts RMS ripple on the incoming +24 VDC line.	**5.1 General Requirements**			Performance Test	**Design**
740	The sensor unit or isolator front panel shall be provided with a hand pull to facilitate insertion and removal from the Input Assembly.	**5.1 General Requirements**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
741	All control switches, gain dials and channel indicators shall be mounted on the front panel.	**5.1 General Requirements**			Inspection	**Design**
742	Each sensor unit or isolator channel shall have an indicator to provide visual indication of detector or incoming signal.	**5.1 General Requirements**			Inspection	**Design**
743	Each sensor unit or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 milliamperes at 30 VDC.	**5.1 General Requirements**			Analysis	**Design**
744	The output [of each sensor unit or isolator] shall be compatible with the controller unit inputs.	**5.1 General Requirements**			Inspection	**Design**
745	A valid channel input shall cause a channel Ground True Output to the controller unit of a minimum 100 milliseconds in duration.	**5.1 General Requirements**			Performance Test	**Design**
746	An onboard physical switching mechanism shall be provided to disable this feature when the mechanism is in an OPEN position.	**5.1 General Requirements**			Inspection	**Design**
747	Said [onboard physical] switching mechanism shall eliminate the minimum timing requirement.	**5.1 General Requirements**			Analysis	**Design**
748	The output transistor shall switch from OFF to ON state or ON to OFF state in 20 microseconds or less.	**5.1 General Requirements**			Performance Test	**Design**
749	Onboard protection shall be provided to enable the sensor unit or isolator to comply with ANSI/IEEE C62.41 (100 Kilohertz Ring Wave and the EFT Burst) at voltages and currents specified at “Location Category A1” (i.e. up to 2.0 Kilovolts, 0.07 Kiloampheres for the 100 Kilohertz Ring Wave) and at “Test Severity” level I (i.e. up to 1.0 Kilovolts, open-circuit) for the EFT Burst.	**5.1 General Requirements**			Analysis	**Design**
750	Detector Sensor Units and Isolators shall have a front panel mounted test switch for each channel to simulate valid input.	**5.1 General Requirements**			Inspection	**Design**
751	The test switch shall be a single-pole double-throw, three position CONTROL test switch: The position assignment shall be UP = Constant ON; MIDDLE = Normal Operation; and DOWN = Momentary ON.	**5.1 General Requirements**	P	The text does not reflect the actual look and feel of the standard.	Inspection	**Performance**

B.22 ITS Cabinet Model 222 & 224 Loop Detector Sensor Unit Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
752	The sensor unit channel shall produce an output signal when a vehicle passes over or remains over loop wires embedded in the roadway.	**5.2.1 General Requirements**			Performance Test	**Design**
753	The method of detection shall be based upon a design that renders the output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% minimum decrease in inductance of the circuit measured at the input terminals of the sensor unit.	**5.2.1 General Requirements**		This appears to be a design "suggestion" versus a requirement. Should be re-worded for clarity.	Analysis	**Design**
754	The detector zone shall include, but not be limited to, all configurations listed in section 5.2.3.1.	**5.2.1 General Requirements**			Analysis	**Design**
755	An open loop shall cause the sensor unit channel to output a signal indicating a non-detect situation.	**5.2.1 General Requirements**			Performance Test	**Design**
756	Each sensor unit channel must be capable of detecting all types of AGENCY licensed motor vehicles when connected to the loop configuration/lead-in requirements of section 5.2.3.1	**5.2.1 General Requirements**			Analysis	**Design**
757	The sensor unit shall comply with all performance requirements when connected to an inductance (loop plus lead-in) from 50 to 700 micro Henries with a Q-parameter as low as 5 at the sensor unit operating frequency.	**5.2.1 General Requirements**			Performance Test	**Design**
758	Loop inputs to each channel shall be transformer-isolated.	**5.2.1 General Requirements**			Inspection	**Design**
759	Each individual channel shall have a minimum of four switch-selectable operating frequencies.	**5.2.1 General Requirements**			Inspection	**Design**
760	The sensor unit channel tuning circuits shall be automatic and shall be so designed that drift caused by environmental changes or changes in applied power shall not cause an actuation.	**5.2.1 General Requirements**			Performance Test	**Design**
761	A switch or switch position shall be provided on the front panel to disable each channel output.	**5.2.1 General Requirements**			Inspection	**Design**
762	Each sensor unit channel shall have PULSE and PRESENCE selectable modes.	**5.2.2 Mode Selection Requirements**			Inspection	**Design**
763	In the PULSE MODE, each new vehicle presence within the detection zone shall initiate a sensor unit channel output pulse of 125 milliseconds (+/-25 milliseconds) in duration.	**5.2.2 Mode Selection Requirements**			Performance Test	**Design**
764	Should a vehicle remain in a portion of the detection zone for a period in excess of two seconds, the sensor unit channel shall automatically "tune out" the presence of said vehicle.	**5.2.2 Mode Selection Requirements**			Performance Test	**Design**
765	The sensor unit channel shall then [after "tuning out" the presence of a vehicle] be capable of detecting another vehicle entering the same detection zone.	**5.2.2 Mode Selection Requirements**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
766	The recovery time to full sensitivity between the first vehicle pulse and channel capability to detect another vehicle shall be a maximum of three seconds.	**5.2.2 Mode Selection Requirements**			Performance Test	**Design**
767	In the PRESENCE MODE, the sensor unit channel shall recover to normal sensitivity within one second after termination of vehicle presence in the detection zone regardless of the duration of the presence.	**5.2.2 Mode Selection Requirements**			Performance Test	**Design**
768	The channel sensitivity settings shall provide presence detection of a vehicle in the detection zone for a specified time period and inductance change(s).	**5.2.2 Mode Selection Requirements**			Analysis	**Design**
769	The conditions are as follows: *MINIMUM TIME DURATION IN MINUTES* / *DETECTOR INPUT INDUCTANCE CHANGE* SETTING 6: 3 — 0.02% or more 10 — 0.06% or more SETTING 2: 4 — 1.00% or more	**5.2.2 Mode Selection Requirements**			Analysis	**Design**
770	[The Loop Detector Sensor Units must properly function with] Single Type A, B, Q or Round Loop with a 250 foot lead-in cable.	**5.2.3 Sensitivity**			Performance Test	**Design**
771	[The Loop Detector Sensor Units must properly function with] Single Type A, B, Q or Round Loop with a 1000 foot lead-in cable.	**5.2.3 Sensitivity**			Performance Test	**Design**
772	[The Loop Detector Sensor Units must properly function with] 4 Type A, B, or Q Loops connected in series/parallel with a 250 foot lead-in cable.	**5.2.3 Sensitivity**			Performance Test	**Design**
773	[The Loop Detector Sensor Units must properly function with] 4 Type A, B, Q or Round Loops connected in series with a 1000 foot lead-in cable.	**5.2.3 Sensitivity**			Performance Test	**Design**
774	[The Loop Detector Sensor Units must properly function with] One 50 foot Type C Loop with a 250 foot lead-in cable.	**5.2.3 Sensitivity**			Performance Test	**Design**
775	Each sensor unit channel shall be equipped with seven selectable sensitivity setting(s) in presence and pulse modes to accomplish the following under operational and environmental requirements of this specification:	**5.2.3 Sensitivity**			Inspection	**Design**
776	Each sensor unit channel shall respond while in Setting 2 to a nominal change in inductance between 0.15% to 0.4% (median sensitivity of 0.32%) while connected to the loop configurations described in section 5.2.3.1.	**5.2.3 Sensitivity**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
777	Each sensor unit channel shall respond while in Setting 6 to an inductance of 0.02% while connected to the loop configurations described in section 5.2.3.1.	**5.2.3 Sensitivity**			Performance Test	**Design**
778	All sensitivity settings shall not differ +/-40% from the nominal value chosen.	**5.2.3 Sensitivity**			Performance Test	**Design**
779	Each sensor unit channel shall not detect vehicles, moving or stopped, at distances of three feet or more from any loop perimeter, in all configurations listed in section 5.2.3.1.	**5.2.3 Sensitivity**			Performance Test	**Design**
780	Response time of the sensor unit channel for Sensitivity Setting 2 shall be less than five +/- one milliseconds at an approximate loop frequency of 40 Kilohertz.	**5.2.4 Response Time**			Performance Test	**Design**
781	That is, for any decreased inductive change that exceeds its sensitivity threshold, the channel shall output a ground true logic level within five milliseconds (+/- one millisecond).	**5.2.4 Response Time**			Performance Test	**Design**
782	When such change [any decreased inductive change that exceeds the sensitivity threshold of the loop] is removed, the output shall become an open circuit within five milliseconds (+/- one millisecond).	**5.2.4 Response Time**			Performance Test	**Design**
783	The sensor unit channels shall begin normal operation within two seconds after the application of power or after a reset signal of 30 microseconds.	**5.2.5 Beginning of Normal Operation**			Performance Test	**Design**
784	The sensor unit shall be capable of compensating or tracking for an environmental change up to 0.001% change in inductance per second.	**5.2.6 Tracking Rate**			Performance Test	**Design**
785	The sensor unit shall be capable of normal operation as the input inductance is changed from +/- 5.0% from the quiescent tuning point regardless of internal circuit drift.	**5.2.7 Tracking Range**			Performance Test	**Design**
786	The sensor unit shall be capable of normal operation as the input resistance is changed from +/- 0.5% from the quiescent tuning point regardless of internal circuit drift.	**5.2.7 Tracking Range**			Performance Test	**Design**
787	The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance of the loop caused by environmental changes, with the rate of temperature change not exceeding 1 degree C per 3 minutes.	**5.2.8 Temperature Change**			Performance Test	**Design**
788	The opening or closing of the controller cabinet door with a temperature differential of up to 18 degrees C between the inside and outside air shall not affect the proper operation of the sensor unit.	**5.2.8 Temperature Change**			Performance Test	**Design**

B.23 ITS Cabinet Model 231 Magnetic Detector Sensing Element Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
789	Each sensing element shall be designed for ease of installation, repositioning, and removal.	**5.3.1 Model 231 Magnetic Detector Sensing Element**		What does it mean to be "designed for ease of…" anything? How is this quantified?	Inspection	**Design**
790	The sensing element shall be 2.25 inches maximum in diameter and have no sharp edges along its length.	**5.3.1 Model 231 Magnetic Detector Sensing Element**			Inspection	**Design**
791	The overall length [of the sensing element] shall not exceed 21 inches.	**5.3.1 Model 231 Magnetic Detector Sensing Element**			Inspection	**Design**
792	Each sensing element, including lead-in shall have a DC resistance of less than 3500 ohms.	**5.3.1 Model 231 Magnetic Detector Sensing Element**			Performance Test	**Design**
793	The sensing element shall be constructed of nonferrous material and shall be moisture proof.	**5.3.1 Model 231 Magnetic Detector Sensing Element**		The requirement "moisture proof" has a quantifiable range, and should be specified this way.	Inspection	**Design**
794	The element shall contain no moving parts or active components.	**5.3.1 Model 231 Magnetic Detector Sensing Element**			Inspection	**Design**
795	The element shall have a 50 feet lead-in cable.	**5.3.1 Model 231 Magnetic Detector Sensing Element**			Inspection	**Design**
796	Leakage resistance shall be a minimum of 10 Megohms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a salt-water bath after the device has been entirely immersed in the bath for a period of 24 hours at 20 degrees C (+/-3 degrees C). The salt-water bath concentrate shall be one-fourth ounce of salt per gallon of water.	**5.3.1 Model 231 Magnetic Detector Sensing Element**			Performance Test	**Design**
797	Each sensing element including lead-in shall have a DC resistance of less than 3500 Ohms and an inductance of 20 Henrys (+/-15 %).	**5.3.1 Model 231 Magnetic Detector Sensing Element**			Performance Test	**Design**
798	The Model 232 Two-Channel Magnetic Detector Sensor Unit shall provide two channels of detection.	**5.3.2 Model 232 Two Channel Magnetic Detector Sensing Element**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
799	When resident in an energized cabinet Input Assembly, and each channel connected to its associated Model 231 Magnetic Detector Sensing Element(s), the channel shall produce a continuous output signal to the controller unit when a voltage is induced in the sensing element by a vehicle passing over the sensing element.	**5.3.2 Model 232 Two Channel Magnetic Detector Sensing Element**			Performance Test	**Design**
800	Each channel shall detect vehicles passing within six feet of the Model 231 Sensing Element with 1000 feet of lead-in cable, at all speeds between three and 80 miles per hour.	**5.3.2 Model 232 Two Channel Magnetic Detector Sensing Element**			Performance Test	**Design**
801	A single control knob for adjusting the sensitivity of each channel shall be mounted on the front panel and shall be readily adjustable without the use of tools.	**5.3.2 Model 232 Two Channel Magnetic Detector Sensing Element**			Inspection	**Design**
802	A momentary switch or switch position shall be provided to place a call on each channel, on an individual basis.	**5.3.2 Model 232 Two Channel Magnetic Detector Sensing Element**			Inspection	**Design**

B.24 ITS Cabinet Model 242 Two-Channel DC Isolator Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
803	The Model 242 Two-Channel DC Isolator shall contain two isolation channels which provide isolation between electrical contacts external to the module and the controller unit input.	**5.4.1 General Requirements**			Inspection	**Design**
804	The method of isolation shall be based upon a design which shall provide reliable operation.	**5.4.1 General Requirements**		These words amount to suggestions that cannot be quantified in any way.	**Drop from the standard.**	**Design**
805	The isolator shall have an internal power supply supplying 20 VDC (+/-4 VDC) to the field input side of the isolation channels.	**5.4.1 General Requirements**			Inspection	**Design**
806	The isolator shall not draw more than 2.5 Watts of AC power.	**5.4.1 General Requirements**			Performance Test	**Design**
807	No current shall be drawn from the cabinet power supply.	**5.4.1 General Requirements**			Performance Test	**Design**
808	A channel contact closure input of five milliseconds or less shall not cause an output (ground true) to the controller.	**5.4.1 General Requirements**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
809	An input of 25 milliseconds or greater shall cause an output to the controller.	**5.4.1 General Requirements**			Performance Test	**Design**
810	An input of duration between five and 25 milliseconds may or may not cause an output to the controller.	**5.4.1 General Requirements**		What is the implementer to do with an "either-or" requirement such as this one?	Performance Test	**Design**
811	The channel circuitry shall be able to react to a new input closure within 25 milliseconds of an input opening.	**5.4.1 General Requirements**			Performance Test	**Design**
812	Each isolation channel field input shall be turned ON (TRUE) when a contact closure causes an input voltage of less than 8 VDC, and shall be turned OFF (FALSE) when the contact opening causes the input voltage to exceed 12 VDC.	**5.4.1 General Requirements**			Performance Test	**Design**
813	Each input shall deliver no less than 15 milliamperes, nor more than 40 milliamperes, to an electrical contact closure or short from the power supply.	**5.4.1 General Requirements**			Performance Test	**Design**

B.25 ITS Cabinet Model 242 Two-Channel AC Isolator Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
814	The Model 252 Two-Channel AC Isolator shall contain two isolation channels which provide isolation between external 120 VAC input circuits and the controller unit input circuits.	**5.5.1 General Requirements**			Inspection	**Design**
815	The method of isolation shall be based upon a design that provides reliable operation.	**5.5.1 General Requirements**		These words amount to suggestions that cannot be quantified in any way.	**Drop from the standard.**	**Design**
816	A channel input voltage "Von" of 80 VAC (+/-5 VAC) applied for a minimum duration of 120 milliseconds (+/-10 milliseconds) shall cause an output (Ground True) to the controller unit.	**5.5.1 General Requirements**			Performance Test	**Design**
817	A channel input voltage "Voff" (Von minus 10 VAC) applied for a minimum duration of 120 milliseconds (+/-10 milliseconds) shall cause an output (Ground False) to the controller unit.	**5.5.1 General Requirements**			Performance Test	**Design**
818	A two-post jumper shall be provided to select inverted output states for Von and Voff.	**5.5.1 General Requirements**			Inspection	**Design**
819	When in CLOSED position (Grounded), Von shall cause a Ground False output.	**5.5.1 General Requirements**			Performance Test	**Design**
820	An indicator shall be provided on the front panel labeled 'RR" which shall indicate a Voff input, Ground True output.	**5.5.1 General Requirements**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
821	The input impedance of each channel shall be between 6,000 – 15,000 Ohms at 60 Hertz.	**5.5.1 General Requirements**			Inspection	**Design**
822	The minimum isolation shall be 1000 Megohms between the input and output terminals at 500 AC applied voltage.	**5.5.1 General Requirements**			Inspection	**Design**

B.26 ITS Cabinet Model Serial Bus Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
823	The ATC Controller Unit is serially connected to the Cabinet via two serial synchronous ports located at the Field I/O C12 Connector or the CPU-1B C13 Connector (Serial Bus 1 only).	**6.1.1 General**			Analysis	**Design**
824	These two communication links use EIA-485 Drivers/Receivers and Synchronous Data Link Control (SDLC) Protocol to interface with Serial Bus #1 and #2.	**6.1.1 General**			Inspection	**Design**
825	Serial Bus #1 shall function as a distributed real-time cabinet control and communications bus.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
826	The Bus Commands are generated in the ATC Controller Unit.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
827	They [the Bus Commands] shall be passed to the assembly Model 218 SIU Units and Model 212 CMU Monitor Unit using EIA 485 COMM/SDLC Protocol Frame Address/Message Packets.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
828	The SIU Units shall read the Address Connector for Assembly Address Number.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
829	The CMU shall read the Address Connector of the PDA.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
830	The AMU units shall read address information as part of the Output Assembly address connector.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
831	The following Address Frame numbers shall be assigned to the assemblies and monitor as:	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**

Address	*SYSTEM ASSEMBLY / UNIT*	*ADDRESS*										
		SIU								*AMU*		
		A7	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*	*A0*	*A2*	*A1*	*A0*
0	Reserved									0	0	0
1	14 Pack in position 1	0	0	0	0	0	0	0	1	0	0	1
2	Reserved											
3	14 Pack in position 3	0	0	0	0	0	0	1	1	0	1	1
4	6 Pack in position 4	0	0	0	0	0	1	0	0	1*	0	0
5	6 Pack in position 1	0	0	0	0	0	1	0	1	1*	0	1
6	6 Pack in position 2	0	0	0	0	0	1	1	0	1*	1	0
7	6 Pack in position 3	0	0	0	0	0	1	1	1	1*	1	1
8	Reserved											
9	Input #1	0	0	0	0	1	0	0	1			
10	Input #2	0	0	0	0	1	0	1	0			
11	Input #3	0	0	0	0	1	0	1	1			
11	Input #4	0	0	0	0	1	1	0	0			
13	Input #5	0	0	0	0	1	1	0	1			
14	Reserved											
15	CMU #1	0	0	0	0	1	1	1	1			
16	CMU #2	0	0	0	1	0	0	0	0			
17	CMU #3	0	0	0	1	0	0	0	1			
18	CMU #4	0	0	0	1	0	0	1	0			
19	CPU	0	0	0	1	0	0	1	1			
20	FIO 2A or 8	0	0	0	1	0	1	0	0			
21to 254	Reserved											
255	Broadcast All	1	1	1	1	1	1	1	1			

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
832	If the Command Address Frame matches the Unit, the Unit shall read the message for processing and response.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
833	The Message First Byte shall be the message name.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
834	The Unit shall set the Response Packet First Byte to Command Message plus 128 and the appropriate data.	**6.1.3 Serial Bus # 1 System**			Analysis	**Design**
835	The Cabinet Monitoring System shall use two serial Bus systems for the interface; Serial Bus #1, links the ATC Controller Unit via a Serial Bus Harness to the DC Power/Communications Assembly.	**6.1.5 Cabinet Control/Emergency Override System**			Analysis	**Design**
836	A Serial Bus Harness plugged into the DC Power/Communications Assembly shall connect to the 212 Cabinet Monitor Unit with application serial memory key resident in the PDA ITS.	**6.1.5 Cabinet Control/Emergency Override System**			Analysis	**Design**
837	Serial Bus #3 Harnesses shall provide the interconnection between the Output Assembly's 214 Auxiliary Monitor Units and the CMU.	**6.1.5 Cabinet Control/Emergency Override System**			Inspection	**Design**
838	The Bus Harnesses shall be daisy chained between the Output Assemblies and the PDA ITS.	**6.1.5 Cabinet Control/Emergency Override System**			Inspection	**Design**
839	See sections 4.4 and 4.5 (CMU and AMU) for operations, functions, protocol, Message frames and bit rate.	**6.1.5 Cabinet Control/Emergency Override System**			Analysis	**Design**

B.27 ITS Cabinet Model Housing Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
840	The housing shall be rainproof.	**6.2.2 Housing Construction**		What does "rainproof" mean and how is it quantified?	Analysis	**Design**
843	The aluminum surface shall be either coated with a Mill Finish or Anti-Graffiti Paint.	**6.2.2 Housing Construction**			Inspection	**Design**
846	The spacer supports shall have the option to use 0.059 inch minimum stainless steel sheet.	**6.2.2 Housing Construction**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
847	All exterior seams for enclosure and doors shall be continuously welded and shall be smooth.	**6.2.2 Housing Construction**		Can "smooth" be quantified?	Inspection	**Design**
848	All edges shall be filled to a radius of 0.03125 inch minimum.	**6.2.2 Housing Construction**			Inspection	**Design**
866	The enclosure door frames shall be double-flanged out on all four sides and shall have strikers to hold tension on, and to form a firm seal between, the door gasketing and the frame.	**6.2.2 Housing Construction**			Inspection	**Design**
867	The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 0.156 inch (+/-0.08 inches).	**6.2.2 Housing Construction**			Inspection	**Design**
868	Gasketing shall be provided on all door openings and shall be dust-tight.	**6.2.3 Gasketing**		Is there a performance criterion for "dust tight" that could be used here?	Inspection	**Design**
869	Gaskets shall be 0.25 inches minimum thickness closed cell neoprene or silicone (BOYD R-108480 or equal) and shall be permanently bonded to the metal.	**6.2.3 Gasketing**			Inspection	**Design**
871	Cage mounting supports shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment; side cage supports provided for the bracket cage supports; and bracket cage support attachments.	**6.2.4 Cage Mounting Supports**			Inspection	**Design**
873	Each eye opening shall have a minimum diameter of 0.75 inch.	**6.2.5 Lifting Eyes and Exterior Bolt Heads**			Inspection	**Design**
874	Each eye shall be able to support the weight load of 1000 lbs.	**6.2.5 Lifting Eyes and Exterior Bolt Heads**			Performance Test	**Design**
876	The latching handles shall have provision for padlocking in the closed position.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
877	Each handle shall be 0.75 inch minimum diameter stainless steel with a minimum of 0.50 inch shank.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
878	The padlocking attachment shall be placed at 4 inch from the handle shank center.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
879	An additional 4 inch minimum gripping length shall be provided.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
880	The latching mechanism shall be a three-point draw roller type.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
881	The pushrods shall be turned edgewise at the outward supports and have a cross section of 0.25 inch thick by 0.75 inch wide minimum.	**6.2.6 Door Latches and Locks**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
882	Rollers shall have a minimum diameter of 0.875 inch with nylon wheels and steel ball bearings.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
883	When the door is closed and latched, the door shall be locked.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
884	The lock and lock support shall be rigidly mounted on the door.	**6.2.6 Door Latches and Locks**		Can “rigidly mounted” be quantified?	Inspection	**Design**
885	The lock shall be mounted in the upper quadrant, above the handle when in it’s full open position.	**6.2.6 Door Latches and Locks**		“It’s” is a contraction, but a possessive case is needed here.	Inspection	**Design**
886	The locks shall be Corbin 2 type.	**6.2.6 Door Latches and Locks**		Need to dig up specifications for this “type.”	Inspection	**Design**
887	One key shall be supplied with each lock.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
888	The keys shall be removable in the locked position only.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
889	The locks shall have rectangular, spacing loaded bolts.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
890	The bolt shall have a 0.281 inch throw and shall be 0.75 inch wide by 0.375 inch thick.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
891	Tolerance is 0.035 inch.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
892	A swing away cover shall be placed over the key entrance to protect the lock mechanism.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
893	The center latch cam shall be fabricated of a minimum thickness of 0.188 inch aluminum, or 11 gauge steel.	**6.2.6 Door Latches and Locks**		Manufacturing specification.	Inspection	**Design**
894	The bolt surface shall horizontally cover the cam thickness.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
895	The cam shall be structured to only allow the door to open when the handle is moved toward the center of the door.	**6.2.6 Door Latches and Locks**			Inspection	**Design**
896	The louvered vent depth shall be a maximum of 0.25 inch.	**6.2.7 Housing Ventilation**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
897	A removable and reusable air filter shall be housed behind the door vents.	**6.2.7 Housing Ventilation**			Inspection	**Design**
898	The filter filtration area shall cover the vent opening area.	**6.2.7 Housing Ventilation**			Inspection	**Design**
899	A filter shell shall be provided that fits over the filter providing mechanical support for the filter.	**6.2.7 Housing Ventilation**			Inspection	**Design**
900	This shell shall be louvered to direct the incoming air downward.	**6.2.7 Housing Ventilation**			Inspection	**Design**
901	The shell sides and top shall be bent over a minimum of 0.25 inch to house the filter.	**6.2.7 Housing Ventilation**			Inspection	**Design**
902	The filter resident in its shell shall be held firmly in place with a bottom trough and spring loaded upper clamp.	**6.2.7 Housing Ventilation**			Inspection	**Design**
903	No incoming air shall bypass the filter.	**6.2.7 Housing Ventilation**			Inspection	**Design**
904	The bottom filter trough shall be formed into a waterproof sump with drain holes to the outside housing.	**6.2.7 Housing Ventilation**			Inspection	**Design**
905	The filter shall be 16 inch wide by 12 inch high by 0.875 inch thick.	**6.2.7 Housing Ventilation**			Inspection	**Design**
906	The filter shall be an ECO-AIR Product E35S or equal.	**6.2.7 Housing Ventilation**		Need to dig up this specification.	Inspection	**Design**
907	The intake (including filter with shell) and exhaust areas shall pass a minimum of 60 cubic feet of air per minute for Housing #1; 120 cubic feet of air per minute for Housing #3; and 26 cubic feet of air per minute for Housing #2.	**6.2.7 Housing Ventilation**			Performance Test	**Design**
908	Each electric fan shall be equipped with ball or roller bearings and shall have a minimum capacity of 100 cubic feet of free air delivery per minute.	**6.2.7 Housing Ventilation**			Performance Test	**Design**
909	The fan shall be mounted within the housing and protected with a finger guard.	**6.2.7 Housing Ventilation**			Inspection	**Design**
910	Stainless Steel hinges (two bolts per leaf) shall be provided to bolt the enclosure to the doors.	**6.2.8 Hinges**			Inspection	**Design**
911	Housing #1 & Housing #3 shall have four hinges per door and Housing #2 shall have three hinges per door.	**6.2.8 Hinges**			Inspection	**Design**
912	Each hinge shall be 3.5 inch minimum length and have a fixed pin.	**6.2.8 Hinges**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
913	The pin ends shall be welded to hinge and ground smooth.	**6.2.8 Hinges**			Inspection	**Design**
915	A ground strap between the door and the main cabinet housing shall be required when 120 VAC components are mounted on the door.	**6.2.8 Hinges**			Inspection	**Design**
916	Front and rear doors shall be provided with catches to hold the door open at both 90 and 165 (+/- 10) degrees.	**6.2.9 Door Catches**			Inspection	**Design**
917	The catch minimum diameter shall be 0.375 inch aluminum rods.	**6.2.9 Door Catches**			Inspection	**Design**
918	The catches must be capable of holding the door open at 90 degrees in a 60 mph wind acting at an angle perpendicular to the plane of the door.	**6.2.9 Door Catches**			Performance Test	**Design**
919	A police panel assembly shall be provided to allow limited control access.	**6.2.10 Police Panel**		What does “limited control access” mean exactly?	Inspection	**Design**
921	The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having live voltage are exposed.	**6.2.10 Police Panel**			Inspection	**Design**
923	The drain [in the police panel] shall be channeled to the outside.	**6.2.10 Police Panel**			Inspection	**Design**
924	The series 35X Cabinets shall have one switch provided and labeled “SIGNALS ON – OFF “.	**6.2.10 Police Panel**			Inspection	**Design**
925	The series 34X Cabinets shall have one switch labeled “SIGNALS ON – OFF” and the other “FLASH/AUTO”.	**6.2.10 Police Panel**			Inspection	**Design**
926	The MANUAL CONTROL ENABLE ON-OFF switch and a receptacle for the INTERVAL ADVANCE cord shall be provided.	**6.2.10 Police Panel**			Inspection	**Design**
927	A 12 VAC transformer shall be provided in advance of the INTERVAL ADVANCE receptacle.	**6.2.10 Police Panel**			Inspection	**Design**
928	An INTERVAL ADVANCE cord, six feet in length, shall be provided.	**6.2.10 Police Panel**			Inspection	**Design**
841	It shall have front and rear doors, each equipped with a lock and handle.	**6.2.2 Housing Construction**	P		Inspection	**Performance**
842	The enclosure top shall be crowned to prevent standing water.	**6.2.2 Housing Construction**	P	Does the angle matter?	Inspection	**Performance**
844	The enclosure, doors, lifting eyes, gasket channels, police panel door, spacer supports and all supports welded to the enclosure and doors shall be fabricated of 0.125 inch minimum thickness aluminum sheet.	**6.2.2 Housing Construction**	P	Measured with calipers.	Inspection	**Performance**
845	The filter shell, filter trough, fan support and police panel enclosure shall be fabricated of 0.080 inch minimum thickness aluminum sheet.	**6.2.2 Housing Construction**	P		Inspection	**Performance**
870	A gasket top and side channels shall be provided to support the top gasket on the door to prevent gasket gravitational fatigue.	**6.2.3 Gasketing**	P		Inspection	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
872	The housing shall be provided with 2 lifting eyes for placing the cabinet on its foundation.	**6.2.5 Lifting Eyes and Exterior Bolt Heads**	P		Inspection	**Performance**
875	All bolt heads shall be tamperproof type.	**6.2.5 Lifting Eyes and Exterior Bolt Heads**	P		Inspection	**Performance**
914	The pins and bolts shall be covered by the door edge and not accessible when the door is closed.	**6.2.8 Hinges**	P		Inspection	**Performance**
920	The panel door shall be equipped with a lock and master police key.	**6.2.10 Police Panel**	P		Inspection	**Performance**
922	The panel assembly shall have a drain to prevent water from collecting within the assembly.	**6.2.10 Police Panel**	P		Inspection	**Performance**
849	Exterior cabinet welds shall be done by gas Tungsten arc TIG process only.	**6.2.2 Housing Construction**		Manufacturing process requirement. Is there a performance criterion?	Inspection	**Procurement**
850	ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum.	**6.2.2 Housing Construction**		Manufacturing process requirement. Is there a performance criterion?	Inspection	**Procurement**
851	Procedures, welders and welding operators shall conform to the requirements and practices in AWS B3.0 and C5.6 for aluminum.	**6.2.2 Housing Construction**		Need to dig up this specification.	Inspection	**Procurement**
852	Internal cabinet welds shall be done by gas metal arc MIG or gas Tungsten arc TIG Process.	**6.2.2 Housing Construction**		Manufacturing process requirement. Is there a performance criterion?	Inspection	**Procurement**
853	ALUMINUM SURFACE PROTECTION shall be either MILL FINISH or ANTI-GRAFFITI Paint.	**6.2.2 Housing Construction**		Need to dig up specifications for these designations.	Inspection	**Procurement**
854	The aluminum surface shall be cleaned, etched and rinsed.	**6.2.2 Housing Construction**		Manufacturing description. Is this appropriate for a standard?	Inspection	**Procurement**
855	The cleaning and etching procedure shall be to immerse in inhabited alkaline cleaner at 71 degrees C for five minutes (Oakite 61A, Diversey 909 or equivalent in mix of the 6 to 8 ounces per gallon to distilled water).	**6.2.2 Housing Construction**		Manufacturing process requirement that cannot be assessed after-the-fact.	Inspection	**Procurement**
856	Rinse in cold water.	**6.2.2 Housing Construction**		Manufacturing process requirement that cannot be assessed after-the-fact.	Inspection	**Procurement**
857	Etch in a sodium solution at 66 degrees C for 5 minutes 90.5 ounce sodium fluoride plus 5 ounces of sodium hydroxide mix per gallon to distilled water.	**6.2.2 Housing Construction**		Manufacturing process requirement. Is there a performance criterion?	Inspection	**Procurement**
858	Rinse in cold water.	**6.2.2 Housing Construction**		Manufacturing process requirement that cannot be assessed after-the-fact.	Inspection	**Procurement**
859	Desmut in a 50% by volume nitric acid solution at 20 degrees C for 2 minutes.	**6.2.2 Housing Construction**		Manufacturing process requirement. Is there a performance criterion?	Inspection	**Procurement**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
860	Rinse in cold water.	**6.2.2 Housing Construction**		Manufacturing process requirement that cannot be assessed after-the-fact.	Inspection	**Procurement**
861	Dry surfaces by preheating in an oven for 15 minutes at 400 degrees F.	**6.2.2 Housing Construction**		Manufacturing process requirement that cannot be assessed after-the-fact.	Inspection	**Procurement**
862	Remove and coat the surfaces using TCI Wheel Silver # 9811- 0110 with a minimum film build of not more than 2 mils total thickness.	**6.2.2 Housing Construction**			Inspection	**Procurement**
863	Place back into preheated oven for 10 minutes minimum at 360 degrees F to gel the base coat.	**6.2.2 Housing Construction**		Manufacturing process requirement that cannot be assessed after-the-fact.	Inspection	**Procurement**
864	Remove and coat the surfaces using TCI Anti-graffiti Clear # 9810-0231.	**6.2.2 Housing Construction**			Inspection	**Procurement**
865	Place back into oven and fully cure at 380 degrees F for 40 minutes.	**6.2.2 Housing Construction**		Manufacturing process requirement that cannot be assessed after-the-fact.		**Procurement**

B.28 ITS Cabinet Rack Cage Requirements

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
929	A Standard Rack Cage shall be installed inside the housing for mounting of the ATC Controller Unit and cabinet assemblies.	**6.3 Rack Cage**			Inspection	**Design**
930	The EIA rack portion of the cage shall consist of four continuous, adjustable equipment mounting angles.	**6.3 Rack Cage**			Inspection	**Design**
931	The mounting angle nominal thickness shall be 11-gauge plated steel.	**6.3 Rack Cage**			Inspection	**Design**
932	The mounting angles shall be tapped with 10-32 threads with EIA universal spacing.	**6.3 Rack Cage**			Inspection	**Design**
933	The mounting angle shall comply with standard EIA-310-B and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.	**6.3 Rack Cage**			Inspection	**Design**
934	The mounting angles shall provide holes to mount the “J” panels.	**6.3 Rack Cage**			Inspection	**Design**
935	Clearance between rails for mounting assemblies shall be 17.75 inch.	**6.3.1 Clearance Between Rails**			Inspection	**Design**
936	The cage(s) shall be centered within the cabinet door opening(s).	**6.3.2 Cage Location**			Inspection	**Design**

B.29 ITS Cabinet Assembly Requirements

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
937	The cabinet assemblies shall be completely removable from or installable in the cabinet cage without removing any other equipment and using only a Standard Slotted or Phillips Screwdriver.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
938	All fuses, circuit breakers, switches (except Police Panel Switches and Fan Fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
939	All equipment in the cabinet shall be clearly and permanently labeled.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
940	The marker strips shall be made of material that can be easily and legibly written on using a pencil or ballpoint pen.	**6.4.1 Cabinet Assemblies – General**		This specification is unquantifiable.	Inspection	**Design**
941	Marker strips shall be located immediately below the item they are to identify and must be clearly visible with the items installed.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
942	Suppression shall be provided at all relay sockets (across relay coil), except for the Transfer Relays (TR) in the output assemblies where one suppression device may be common for all.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
943	PDA, Output and Input Assemblies Depth shall include terminal sockets, plug-in units and strain relief bar (Field Wire Support Bracket).	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
946	The assembly housing top and bottom shall be slotted for vertical ventilation.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
949	The aluminum metal surface shall be treated with clear chromate.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
951	Guides (top and bottom) shall be provided for assembly Plug-in units (Power Supply Units guide on bottom only).	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
952	The guides shall begin 0.50 inch from the assembly front panel face.	**6.4.1 Cabinet Assemblies – General**			Inspection	**Design**
953	The “J” Panels shall be mirror images of each other when mounted in the cabinet cage.	**6.4.2 “J” Panel Assemblies**			Inspection	**Design**
954	They [the “J” Panels] shall be bolted to the cage with the matching shelf unit bolted to the panel.	**6.4.2 “J” Panel Assemblies**			Inspection	**Design**
955	Two ten position minimum AC- Raw & Equipment Ground Copper Bus Bars shall be provided on the lower right position of the J Panel when viewed from the rear door for interconnect to the Service Panel and provide the termination of AC- Raw and Equipment Ground wiring within the Cage and Cabinet.	**6.4.2 “J” Panel Assemblies**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
956	An optional Input Termination Panel shall be provided that uses ten twelve-position terminal blocks and 4 copper bus bars.	**6.4.2 "J" Panel Assemblies**			Inspection	**Design**
957	Eight of the twelve position terminal blocks and the four copper bus bars shall be used for termination of field inputs.	**6.4.2 "J" Panel Assemblies**			Inspection	**Design**
958	Two of the twelve position terminal blocks shall be used for termination of the CDC interface.	**6.4.2 "J" Panel Assemblies**			Inspection	**Design**
959	Input transient protection devices may be used for input termination.	**6.4.2 "J" Panel Assemblies**			Inspection	**Design**
960	Terminal blocks one through four provide termination for Input Assembly #1 and terminal blocks five through eight provide termination for Input Assembly #2.	**6.4.2 "J" Panel Assemblies**			Inspection	**Design**
961	A ground lug shall be provided on the panel assembly to terminate an 8 AWG green wire that is attached to the Equipment Ground copper bus bar on the "J" panel assembly.	**6.4.2 "J" Panel Assemblies**			Inspection	**Design**
962	The Input Termination Panel shall be mounted on the left side of the Rack Assembly, when viewing from the rear.	**6.4.2 "J" Panel Assemblies**			Inspection	**Design**
963	A Shelf Assembly shall be provided unless otherwise called out in the contract special provisions. One alternative is a shelf/drawer assembly.	**6.4.3 Cabinet Shelf Assemblies**		It is unclear why an alternative is listed.	Inspection	**Design**
964	A Service Panel Assembly shall be provided.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
965	The assembly shall function as the entry point for AC Power to the cabinet including main and secondary circuit breakers, cabinet transient and voltage surge protection, clean power filtering, and Raw and Clean AC Power Sources.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
966	The assembly shall be located on the lower right J Panel when viewed from the back door.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
967	The terminals of the Block shall be labeled AC+, AC- and EG and shall be covered with a clear insulating material to prevent inadvertent contact.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
968	The Terminating Lugs shall be large enough to accommodate # 2 conductors.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
969	This assembly shall provide two 8 inch #8 gauge wire extensions for AC- Raw and Equipment Ground, for attachment to the AC- and Ground busses mounted on the "J" panel.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
970	The DC Ground and Equipment Ground Bus shall be electrically isolated by 500 Megohms when tested at 250 VDC.	**6.4.4 Service Panel Assembly**			Performance Test	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
971	The AC- copper terminal bus shall not be grounded to the cabinet or connected to logic ground.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
972	Nylon screws with a minimum diameter of 0.25 inch or nylon spacers shall be used for securing the bus to the J Panel.	**6.4.4 Service Panel Assembly**			Inspection	**Design**
973	This Assembly [raw/clean AC power] shall be provided in each cabinet.	**6.4.5 Raw/Clean AC Power Assembly**			Inspection	**Design**
974	It shall provide Six Clean AC Power Receptacles for assemblies and cabinet units; Raw AC Power to the Output Assemblies; and both logic and power to the Fan and Light system, door opening circuitry and logic interface (all via CCIN and CCOUT Connectors).	**6.4.5 Raw/Clean AC Power Assembly**			Inspection	**Design**
975	The Extension shall provide a minimum of five additional NEMA 5-15 receptacles with harness plug connector for plugging into the main assembly.	**6.4.5 Raw/Clean AC Power Assembly**			Inspection	**Design**
976	The extension may be an option in Housing #1, and shall be required in Cage 2 of the Housing #3.	**6.4.5 Raw/Clean AC Power Assembly**			Inspection	**Design**
977	This assembly shall function as the DC Power bus, providing Six VDC BEAU S5404-SB Receptacles and communications interface between the ATC Controller Unit and other assemblies.	**6.4.6 DC Power / Communications Assembly**			Inspection	**Design**
978	This assembly shall interface with ATC Controller Unit Logic Lines (Power Down, NRESET and LINESYNC) and Seven System Serial Bus signals via DB-25S Connectors.	**6.4.6 DC Power / Communications Assembly**			Inspection	**Design**
979	The Extension shall provide additional Serial Bus Connectors and DC Receptacles. The extension may be an option.	**6.4.6 DC Power / Communications Assembly**			Inspection	**Design**
980	A Serial Bus #1 and #2 Terminator Unit shall be provided and plugged into the DC POWER / COMMUNICATIONS ASSEMBLY DB 25S End Connector.	**6.4.6 DC Power / Communications Assembly**			Inspection	**Design**
981	The Terminator Unit shall provide a 150 ohm termination resistor between the RxD+ and RxD-, the TxD+ and TxD-, the RxC+ and RxC-, and the TxC+ and TxC- pairs for both Serial Bus #1 and Serial Bus #2.	**6.4.6 DC Power / Communications Assembly**			Inspection	**Design**
982	The Terminator Unit shall also provide 1K ohm DC bias resistors from +5VDC ISO to the RxD+, the RxC+, the TxD+, and the TxC+ of both Serial Bus #1 and Serial Bus #2.	**6.4.6 DC Power / Communications Assembly**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
983	The Terminator Unit shall provide 1K ohm DC bias resistors from ISO GND to the RxD-, the RxC-, the TxD-, and the TxC- of both Serial Bus #1 and Serial Bus #2.	**6.4.6 DC Power / Communications Assembly**			Inspection	**Design**
984	The Power Distribution Assembly ITS is an EIA-310B rack mounted assembly that provides for the protection and distribution of AC power and DC power. Additionally: • Logic control circuits, including a Main Contactor for control of the load circuits; • Fault sensing field Circuit Breakers, eight for Traffic applications and four for Traffic Management systems; • Production and distribution of DC power, using +12VDC and 24VDC pluggable power supplies; • A resident Cabinet Monitor Unit (CMU); • Maintenance service, consisting of a circuit breaker in line with GFI equipment power receptacles; • Two Model 204 Flasher Units, protected by a ganged two-pole 20A Circuit Breaker when operating in a Traffic Signal application; • A 25-pin D Socket shall be provided for communication with the ATC Controller Unit. This Socket shall be mated with an 18-inch Communications Cable. This Cable shall be attached to the Assembly by slotted 4-40 screws. See Serial Bus Harnesses Detail 6-5-39.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
985	A four-position Address Socket and plug shall be provided to provide addressing to the CMU.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
986	A CDC Connector shall be provided on the rear panel of the Output Assembly for isolated signal outputs from the police panel.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
987	The CDC Socket is a nine-pin “D” connector that contains the Manual Control Enable, Stop Time, Interval Advance, and Manual Flash switch signals.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
988	The Manual Control Enable and Manual Flash switch signals shall be a 120 VAC signal in series with a 27K Ohm resistor.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
989	The Interval Advance and Stop Time switch signals shall be 12 VAC signals from a transformer located in the PDA.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
990	The secondary output of the 12 VAC transformer shall be tied to AC- RAW.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
991	CDC pin 5 Common shall be referenced to AC- RAW. CDC pin 8 shall provide an interface for the external reset signal and CDC pin 9 shall provide an interface for DC Ground.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
992	The PDA shall be provided with eight field load circuit breakers and two Model 204 Flasher Units with ganged circuit beaker protection.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
993	The Load Circuit Breakers located on the PDA that are used to control the Output Assembly Model 200 Switch Pack Units shall have auxiliary switches.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
994	The auxiliary switches shall “open” when the load breaker has tripped and the system will transfer the power from the Main Contactor to the Flash or Blank condition.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
995	The Amperage Rating of breakers shall be shown on the face of the breaker or handle.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
996	Breaker function shall be labeled below the breakers on the front panel.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
997	Ganged Circuit Breakers shall be assembled by the circuit breaker manufacturer and certified that their circuit breakers shall gang trip.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
998	The maintenance equipment circuit shall include a 15-Ampere Circuit Breaker in line with GFCI receptacles on both the front and back of the assembly.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
999	The back receptacle shall be the first with GFCI Protection device as defined in the National Electrical Code.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1000	Circuit interruption shall occur on 6 milliamperes of ground fault-current and shall not occur less than four milliamperes of ground-fault current.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
1001	The front receptacle shall be attached to the load side of the GFCI device.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1002	The AUTO/FLASH Switch when placed in FLASH position shall de-energize the Main Contactor and the Transfer Relays (TR) Coils.	**6.4.7 Power Distribution Assembly ITS**			Performance Test	**Design**
1003	When the switch is placed in the AUTO position shall energize the Main Contactor and the TR Coils.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1004	The switch shall be a SPST Control Switch.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1005	The DC Power shall be brought to the back panel using a BEAU S5404-SB Receptacle.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1006	An 18-inch DC Power (DCP) Harness, with sheath, consisting of four #18 cables, with a BEAU P5404-LAB Connector on each end, shall be provided with the Assembly.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1007	The harness shall be plugged in to an adjacent plug on the DC/COMM Assembly. See drawing 6-5-40.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1008	Three 36-inch minimum length #8 gauge wires, one black for AC+, one white for AC- and one green or green/yellow for Equipment Ground, shall be attached to the rear of the assembly at the AC Raw Power Terminating Block.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1009	The cables shall be routed between the Service Panel Assembly AC+ terminal, the AC-Bus and the Equipment Ground Bus.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1010	The PDA Assembly shall have a resident 18-inch ACP Harness with sheath and strain relief.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1011	The other end shall contain a BEAU P5412-CCE connector.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
1012	This harness shall be plugged into the P1 connector on the Raw/Clean AC Power Assembly.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1013	The ACP harness shall provide Flasher input and AC power to the Switch Packs.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1014	An 18-inch CC Harness shall be provided with sheath and strain relief.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1015	When plugged into the Raw/Clean AC Power Assembly (CC IN) this harness shall provide AC Raw voltage and control logic between the ITS PDA Assembly and the Police Panel control switches.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1016	An 18-inch long ACCP power cord with strain relief and a NEMA 5-15 plug shall provide AC Clean power to the PDA ITS Assembly when plugged into the Raw/Clean Power Assembly.	**6.4.7 Power Distribution Assembly ITS**			Inspection	**Design**
1017	A capacitive load of one microFarad at 400 VAC shall be provided across each Flasher Unit Output.	**6.4.7 Power Distribution Assembly ITS**			Performance Test	**Design**
1018	The Input Assembly shall be an EIA-310B rack mounted assembly providing twelve slots of 22/44 pin PCB sockets.	**6.4.8 Input Assembly**			Inspection	**Design**
1019	A Model 218 Serial Interface Unit (SIU) shall be provided in its location mated to a DIN 96-Pin Connector.	**6.4.8 Input Assembly**			Inspection	**Design**
1020	The SIU shall provide interface and control between the ATC Controller Unit and the input units via System Serial Bus #1 and #2. See Section 26 Model 218 SIU for System Operation and Interface.	**6.4.8 Input Assembly**			Inspection	**Design**
1021	A 25-pin D Socket shall be provided for communication with the ATC Controller Unit.	**6.4.8 Input Assembly**			Inspection	**Design**
1022	This Socket shall be mated with an 18-inch Communications Cable.	**6.4.8 Input Assembly**			Inspection	**Design**
1023	This Cable shall be attached to the Assembly by slotted 4-40 screws. See Serial Bus Harnesses Detail 6-5-39.	**6.4.8 Input Assembly**			Inspection	**Design**
1024	The input assembly shall be wired to accept Model 222 and 224 ILD Sensor Units, Model 232 Magnetic Sensor Unit, Model 242 and 252 Isolator Units and Slot mounted NEMA Detectors.	**6.4.8 Input Assembly**			Inspection	**Design**
1025	Each slot connector is a PCB 22/44 Pin Socket type wired for two and four channel devices.	**6.4.8 Input Assembly**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
1026	The F and W Unit Output pins shall provide the 24 Inputs to the SIU Channel 1 (Serial Bus #1).	**6.4.8 Input Assembly**			Inspection	**Design**
1027	In addition, NEMA Status inputs shall be provided on pins 7 and 20.	**6.4.8 Input Assembly**			Inspection	**Design**
1028	INBUS shall be provided on pin 19 and 21 with four slots address lines matching NEMA pin outs.	**6.4.8 Input Assembly**			Inspection	**Design**
1029	The SIU Unit shall provide six detector RESET Outputs, one for each pair of input slots.	**6.4.8 Input Assembly**			Inspection	**Design**
1030	Should the NEMA Status not be required, a RESTART Output from the SIU to the sensor units as a soft reset per channel shall be provided via pins 7-20. See Input Assembly Wiring Diagram 6-5-37.	**6.4.8 Input Assembly**			Inspection	**Design**
1031	The INBUS shall interface with the SIU Channel 2 to provide communications between "Smart Input Units" and Serial Bus #2.	**6.4.8 Input Assembly**			Inspection	**Design**
1032	The SIU functions as a hardware driver interface only between the ATC Controller Unit and Input Units installed in the Input Assembly. See Type 218 SIU section 4.	**6.4.8 Input Assembly**			Inspection	**Design**
1033	A 25-pin DB Connector shall be provided on the left assembly side (rear panel) to interface the assembly (SIU) to the DC/COMM Assembly Serial Bus #1 and #2.	**6.4.8 Input Assembly**			Inspection	**Design**
1034	A 32-pin DB (Socket) shall be provided for the Test Function. For Test Connector wiring, see Input Wiring Diagrams 6-5-37.	**6.4.8 Input Assembly**			Inspection	**Design**
1035	Four special function Inputs shall be provided via nine-position subminiature D-type connector to the SIU.	**6.4.8 Input Assembly**			Inspection	**Design**
1036	These are electrically isolated and may handle 12V DC/AC inputs and are referenced to a separate isolated ground.	**6.4.8 Input Assembly**			Inspection	**Design**
1037	Note: In the ITS Cabinet interface wiring 120 VAC inputs shall be routed to the Isolated SIU inputs through a 27K Ohm, one watt resistor located in the PDA ITS Assembly.	**6.4.8 Input Assembly**			Inspection	**Design**
1038	The assembly height shall be 5.25 inches (3U).	**6.4.8 Input Assembly**			Inspection	**Design**
1039	An 18-inch harness cable, with strain relief and sheath and terminated with a BEAU S5404-SB connector, shall be supplied for interconnect of +24/+12VDC power.	**6.4.8 Input Assembly**			Inspection	**Design**
1040	Pins D, E, J, K, and L on each PCB Connector slot shall be routed to their associated field terminal, i.e. FT1-12 Additionally, an Equipment Ground Lug shall be provided on the back panel for termination of a #8 AWG conductor.	**6.4.8 Input Assembly**			Inspection	**Design**
1041	Each Input Assembly shall contain a four-bit address code plug and socket.	**6.4.8 Input Assembly**			Inspection	**Design**
1042	The Input Assembly address shall be provided by a plug with jumpers installed to produce a binary code 1, 2, 4, and 8.	**6.4.8 Input Assembly**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
1043	The address receptacle shall be installed on the back panel of the Input Assembly, Ground True Logic shall be used with Ground True equaling Logic "1". See instructions on Input Assembly Connectors detail 6-5-38.	**6.4.8 Input Assembly**			Inspection	**Design**
1044	All connectors mounted on the PCB shall be mechanically secured to the chassis or frame of the unit or assembly.	**6.4.8 Input Assembly**			Inspection	**Design**
1045	The Output Assembly shall be an EIA-310B rack mounted assembly delivered in six Switch Pack or fourteen Switch Pack configurations.	**6.4.9 Output Assembly**			Inspection	**Design**
1046	This assembly may provide 18 load circuits or 42 load circuits. Either configuration is designed to interface with a plug-in Model 200 Switch Pack Unit.	**6.4.9 Output Assembly**			Inspection	**Design**
1047	The SIU shall be provided resident in its connector to provide interface and control.	**6.4.9 Output Assembly**			Inspection	**Design**
1048	In addition, a Model 214 AMU Unit shall be provided in its connector to sense voltage and current for the CMU.	**6.4.9 Output Assembly**			Inspection	**Design**
1051	The Model 205 relay units and Program Blocks shall be provided to select control and color state of the Emergency Override State (red, yellow, or no indication output).	**6.4.9 Output Assembly**			Inspection	**Design**
1052	The programming connectors shall be Molex Type 1375 or equal.	**6.4.9 Output Assembly**			Inspection	**Design**
1053	The relay units and program blocks shall be mounted on the rear of the Output Assembly.	**6.4.9 Output Assembly**			Inspection	**Design**
1054	Program Block Pins shall be crimped and soldered.	**6.4.9 Output Assembly**			Inspection	**Design**
1055	The Model 205 transfer relays shall be accessible on the rear of the Output Assembly without the use of tools.	**6.4.9 Output Assembly**			Inspection	**Design**
1056	An Address Plug and Socket shall be provided on Output Assembly for defining the Serial Bus #1 and #3 addressing. See 4.7.16, 4.5.1.1, and 6/14 Pack Output Assembly Connectors Detail 6-5-33.	**6.4.9 Output Assembly**			Inspection	**Design**
1057	Transformers shall be provided on the incoming AC source for each Switch Pack to measure the load current. See Section 4.5.7 AMU Current Sensing.	**6.4.9 Output Assembly**			Inspection	**Design**
1058	Field Termination shall be provided on the rear panel of the assembly consisting of six-position sockets and plugs.	**6.4.9 Output Assembly**			Inspection	**Design**
1059	Transient suppression shall be provided at the field terminals, for the protection of the Switch Packs, on rear panel of the assembly consisting of three nine-position sockets and plugs for a six Pack Output Assembly.	**6.4.9 Output Assembly**			Inspection	**Design**
1063	A Serial Bus #1 DB25 female connector shall be provided on the upper left rear panel of the Output Assembly for serial interconnection to the DC Power/Communication Assembly.	**6.4.9 Output Assembly**			Inspection	**Design**

#	Requirement (Standard Document Section)	Document Section	Pass / Fail	Comments	Type	Requirement Type
1064	This Socket shall be mated with an 18-inch Communications Cable.	**6.4.9 Output Assembly**			Inspection	**Design**
1065	This Cable [the serial bus connector between the Output Assembly and the DC Power Communication assembly] shall be attached to the Assembly by slotted 4-40 screws. See Serial Bus Harnesses Detail 6-5-39.	**6.4.9 Output Assembly**			Inspection	**Design**
1066	A CDC Connector shall be provided on the rear panel of the Output Assembly for signal interconnection to the unit.	**6.4.9 Output Assembly**			Inspection	**Design**
1067	The CDC Socket is a 9-pin "D" connector.	**6.4.9 Output Assembly**			Inspection	**Design**
1068	These inputs are electrically isolated and may handle 120 VAC signals when wired to the PDA ITS Assembly and 12 VAC inputs that are referenced to a separate isolated ground.	**6.4.9 Output Assembly**			Inspection	**Design**
1069	This Cable [the CDC Connector] shall be attached to the Assembly by slotted 4-40 screws.	**6.4.9 Output Assembly**			Inspection	**Design**
1070	Two RJ-11S Connectors shall be provided on the rear panel of the Output Assembly for signal interconnection of Serial Bus #3.	**6.4.9 Output Assembly**			Inspection	**Design**
1071	An Equipment Ground Lug shall be provided on the rear panel for termination of a #8 green wire.	**6.4.9 Output Assembly**			Inspection	**Design**
1072	The 6-Pack Output Assembly height shall be 5.25 inches (3 U) and the 14-Pack Output Assembly shall be 10.5 inches.	**6.4.9 Output Assembly**			Inspection	**Design**
1073	Cabinet Harnesses are supplied with each cabinet configuration. See Serial Bus and DCP Harness Details.	**6.4.9 Output Assembly**			Inspection	**Design**
944	The Width shall be 17.5 inches maximum including side screws.	**6.4.1 Cabinet Assemblies – General**	P		Inspection	**Performance**
945	The maximum Depth, including connectors, shall not exceed 14.0 inches.	**6.4.1 Cabinet Assemblies – General**	P		Inspection	**Performance**
947	Assembly Thickness - Side ends shall be fabricated of 0.080 inch minimum thickness aluminum sheet.	**6.4.1 Cabinet Assemblies – General**	P	No maximum is specified here. Should there be?	Inspection	**Performance**
948	All other surfaces [other than side sheets] shall be fabricated of 0.0625 inch minimum thickness aluminum sheet.	**6.4.1 Cabinet Assemblies – General**	P		Inspection	**Performance**
950	Flasher and Switch Pack Unit sockets shall be mounted with their front face 7.50 inch from the assembly front panel.	**6.4.1 Cabinet Assemblies – General**	F	The dimension is correct, but the wording is inverted. The verbiage should say, "7.50 from the back panel to the front plate of the unit.	Inspection	**Performance**
1049	A 25-pin D Socket shall be provided for communication with the ATC Controller Unit.	**6.4.9 Output Assembly**	P		Inspection	**Performance**

#	Requirement (Standard Document Section)	Document Section	Pass Fail	Comments	Type	Requirement Type
1050	This Socket shall be mated with an 18-inch Communications Cable. This Cable shall be attached to the Assembly by slotted 4-40 screws. See Serial Bus Harnesses Detail 6-5-39.	**6.4.9 Output Assembly**	P		Inspection	**Performance**
1060	A 14 Pack Output Assembly requires seven nine-position sockets and plugs.	**6.4.9 Output Assembly**	P		Inspection	**Performance**
1061	Each socket shall provide protection for two Switch Packs.	**6.4.9 Output Assembly**	P		Inspection	**Performance**
1062	Protection devices shall be terminated to Equipment Ground.	**6.4.9 Output Assembly**	P		Inspection	**Performance**

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FHWA-JPO-09-042