REFERENCE USE ONLY

REPORT NO. DOT - TSC - NASA - 71 - 9

METALLIZATION FAILURES

ROSEMARY BEATTY
TRANSPORTATION SYSTEMS CENTER
55 BROADWAY
CAMBRIDGE, MA. 02142

MAY 1971
TECHNICAL REPORT

AVAILABILITY IS UNLIMITED. DOCUMENT MAY BE RELEASED TO THE NATIONAL TECHNICAL INFORMATION SERVICE, SPRINGFIELD, VIRGINIA 22151, FOR SALE TO THE PUBLIC.

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
WASHINGTON, D.C. 20590

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.

4. Title and Subtitle	5. Report Date
Metallization Failures	May 1971
	6. Performing Organization Code TRE
7. Author(s) Rosemary Beatty	8. Performing Organization Report No. DOT-TSC-NASA-71-9
9. Performing Organization Name and Address Transportation Systems Center 55 Broadway Cambridge, Mass. 02142	10. Work Unit No. R-1130
	11. Contract or Grant No.
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D.C. 20590	13. Type of Report and Period Covered Technical Report
	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract Metallization-related failure mechanisms are a major cause of integrated circuit failures under accelerated stress and field operation conditions. Industry's approach has been, (1) a better understanding of the aluminum system, now the most widely used material, and (2) evaluation of alternative metal systems.

The newer and more complex multilevel metallization systems require low temperature deposition techniques and critical etching-through methods due to smaller geometry and closer spacing.

Aluminum metallization offers many advantages, but also has limitations. Alternative materials are being considered for large scale integrated arrays. This survey defines the merits and restrictions of metallization systems in current usage and those under development. Although no specific recommendations are made references can be drawn from the data presented. The advanced state of beam lead technology is apparent.

17. Key Words	18. Distribution Statement
Metallization Failures Integrated Circuit Failures Metallization Material Multilevel Metallization Integrated Circuit Design Beam Lead Technology	Unclassified - Unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	116	

TABLE OF CONTENTS

	Page
SUMMARY	ix
INTRODUCTION	1
METALLIZATION FAILURES	3
Electromigration	6
Etch Pits	15
Aluminum-Silicon Reaction	15
Metal-Metal Interaction	18
Metal-Oxide Interaction	19
Thermal Stresses	19
Peeling in Layered Systems	20
Diffusion Effects in Barrier Layer Systems	20
Electrolytic Migration	20
Scratches in Metallization Stripes	21
METALLIZATION SYSTEMS	21
Requirements	22
Fabrication Processes	25
Single Metal Systems	25
High Current Density Tests	27
Composite Layered Metallization Systems	34
Resistance Change and Au-Si Alloying	45
CONTACT RESISTANCE	47
TEMPERATURE STABILITY	49
CURRENT DENSITY	51
Chromium-Gold	51
Chromium-Silver-Gold	51
Titanium-Gold	51
Titanium-Platinum-Gold	53
Molybdenum-Gold	57
Summary of Current Density Tests	62
MULTILAYER METALLIZATIONS	64
MULTILAYER TEST VEHICLES	70
FINE LINE PATTERNING	74
SPUTTER ETCHED SEMICONDUCTOR CONTACTS	78
BEAM LEAD TECHNOLOGY	82
METALLIZATION	99
CONCLUSIONS	102
REFERENCES	103

LIST OF ILLUSTRATIONS

		Page
1.	Schematic of Single Metal, Multilayer, and Multilevel Metallization	2
2.	Scanning Electron Microscope Micrograph of Shadowing Effect	4
3.	Mean-Time-To-Failure as a Function of Current Density and Film Temperature: Aluminum Films Evaporated from Tungsten onto Cold Substrate	7
4.	Mean-Time-To-Failure as a Function of Current Density and Film Temperature: Aluminum Films Evaporated from Tungsten Filaments Condensed onto Hot (400°C) Substrates	8
5.	Mean-Time-To-Failure as a Function of Current Density and Film Temperature: 1.46 mil Wide by 12,200 Å Thick, Well Ordered Aluminum Coated with 6000 Å Thick Glass Film	9
6.	Experimentally Determined vs Calculated Mean-Time-to-Failure for Large-Grained Aluminum Films of Variable Line Width	10
7.	Experimentally Determined vs Calculated Mean-Time-to-Failure for Large Grained Aluminum Film Conductors of Variable Thickness	12
8.	Aluminum Film Resistivity Normalized to Bulk Resistivity as a Function of Film Thickness	13
9.	Mean-Time-to-Failure for Aluminum Film Conductors as a Function of Current Density, Temperature and Cross-sectional Dimensions	13
10.	Small Crystallite Aluminum Film Lifetime of Conductors with $10^{-7}cm^2$ Cross-sectional Area	14
11.	Large Crystallite Aluminum Film Lifetime of Conductors with $10^{-7}cm^2$ Cross-sectional Area	14
12.	Glassed Large Crystallite Aluminum Film Lifetime for Conductors with a Cross-section of $10^{-7}cm^2$	15
13.	Penetration of Aluminum into Thermally Grown SiO_2 as a Function of Time and Temperature	16
14.	Penetration Rate of Aluminum Reaction into Thermally Grown SiO_2 as a Function of Temperature	17
15.	Penetration of Aluminum into SiO_2 Extrapolated to Lower Temperatures	17
16.	Photomicrographs of Aluminum Lines	31

LIST OF ILLUSTRATIONS (CONTD)

		Page
37.	5° Angle Cross Section of Multilayer Molybdenum-Gold-Glass-Molybdenum-Gold	71
38.	Schematic Representation of Molybdenum-Gold Multilayer Test Vehicle	71
39.	5° Angle Cross Section of Multilayer Molybdenum-Gold-Molybdenum-Glass-Molybdenum-Gold-Glass	72
40.	Molybdenum-Gold-SiO_2 Glass-Molybdenum-Gold Multilayers after 1 Hour at $450^{o}C$ in Air	73
41.	Molybdenum-Gold Multilayer SiO_2 Structure after 18 Hours at $450^{o}C$ in Air	73
42.	Interconnect Metal Mask	74
43.	5° Angle Cross Section of Multilayer Molybdenum-Gold-Molybdenum-Glass-Molybdenum-Gold-Glass	76
44.	5° Angle Cross Section of Multilyaer Molybdenum-Gold-Molybdenum-Glass-Molybdenum-Gold-Glass	77
45.	Photomicrograph of Scratched Molybdenum-Gold Metallization- Line 2 mils Wide	77
46.	Photomicrograph of Poorly Etched 3-micron Aluminum Film Line 2 mils Wide	77
47.	Diagram of Diode RF Sputtering System	79
48.	Photomicrographs of Sputter-Etched Ti-Pt-Au; Smallest Line 0.2 mil, Au 8000 Å, Pt 2000 Å, Ti 2000 Å	80
49.	Cross Section of Sputter-Etched Ti-Pt-Au	81
50.	Aluminum Beam Lead System with Separately Deposited Beams	91
51.	Cross Section of Beam Lead Device with Glassivated Aluminum Interconnections	92
52.	Cross Section of Dielectric and Air Gap Isolated Crossover	93
53.	Shelving in Oxide-Nitride Dielectrics	97
54.	Etch Rates of Silicon Nitride vs Oxygen Content	98

LIST OF TABLES

		Page
1.	Reasons for Opens or Localized Reduced Cross-Sectional Area in Multilevel Metallization	3
2.	Test Data for Small Crystallite Aluminum Films	7
3.	Test Data for Large Crystal Aluminum Films	8
4.	Glassed Large Crystal Aluminum Performance	9
5.	Glassed Large Crystal Aluminum Predicted Performance	9
6.	Test Data for Large Crystal Aluminum Film Conductors of Variable Line Widths	10
7.	Test Data for Large Crystal Aluminum Film Conductors of Variable Thickness	11
8.	Rate of Aluminum Penetration into SiO_2	16
9.	Resistive Properties of Various Metals	23
10.	Aluminum High Current Test Data	28
11.	Mean Time to Failure for Aluminum Metallization as a Function of Resistivity and Current Density	29
12.	Deposition Data and Properties of W and Mo	33
13.	Resistance of Various Metal(s) after Air Bakes, 1- x 54-mil Conductors, Alloy Tests are on 20-mil^2 Contacts	35
14.	ΔR of Pt-Au Films with 450°C Air Bakes	39
15.	Resistivity of Pt-Au After 30 Minutes at 1000°C	40
16.	ΔR of Ti-Pt and Ti-Pt-Au at 450°C	40
17.	Cr-Ag-Au and Ti-Ag-Au Resistance Changes	42
18.	Ti-Ag and Cr-Ag Resistance Changes (1 mil x 54 mil)	42
19.	Resistance Change	44
20.	Summary, Resistance Change and Au-Si Alloying	45
21.	Metal Silicon Contact Resistance, in ohms, Area = 10^{-4} cm^2	48
22.	Temperature Stability, Contact Resistance in ohms	50
23.	Chromium-Gold High Current Test Data	52
24.	Titanium-Gold High Current Test Data	53
25.	Titanium-Platinum-Gold High Current Data	54
26.	Molybdenum-Gold High Current Test Data	56

SUMMARY

Metallization-related failure mechanisms have been shown to be a major cause of integrated circuit failures under accelerated stress conditions, as well as in actual use under field operation. The integrated circuit industry is aware of the problem and is attempting to solve it in one of two ways: (1) better understanding of the aluminum system, which is the most widely used metallization material for silicon integrated circuits both as a single level and multilevel metallization, or (2) evaluating alternative metal systems.

As integrated circuit structures become more complex, additional processing steps are required to obtain multilevel metallization. Low temperature deposition of dielectrics is essential, and etching through to interconnect the levels of metallization is critical. In addition, smaller geometry and closer spacings are required.

Aluminum metallization offers many advantages, but also has limitations particularly at elevated temperatures and high current densities. As an alternative, multilayer systems of the general form, silicon device-metal-inorganic insulator-metal, are being considered to produce large scale integrated arrays. This survey defines the merits and restrictions of metallization systems in current usage and systems under development. To offer any specific recommendations would be presumptuous without detailed knowledge of the device structure, applications, environmental conditions and manufacturers capability. In cases where aluminum metallization can be used the preference is obvious; since it is a single metal system, well-investigated and lends itself to production techniques. If field conditions and specific applications rule out aluminum, then titanium-platinum-gold or titanium-palladium-gold would be advisable. In either case beam lead technology appears to be well enough advanced technically to warrant specification.

INTRODUCTION

Metallization-related failure mechanisms have been shown to be a major cause of integrated circuit failures under accelerated stress conditions as well as in actual use under field conditions (ref. 1). This survey will concentrate on inherent limitations in material combinations, and methods of detecting these, to provide guide lines for characterization and selection of metallization systems for silicon integrated circuits.

This section presents detailed technical information on processing steps for the fabrication of large-scale integrated circuits, subsequent to diffusion, and the effects of such steps on metallization reliability. The critical steps in integrated circuit fabrication are discussed, and properties of the metallization reliability are examined, particularly in terms of their impact on long term reliability. Desired properties of the metal films are considered relative to the rather extensive body of available information on metallization related failure mechanisms in integrated circuits, both of conventional complexity and LSI arrays.

Metallization characterization tests are determined by: (1) properties of metal thin films, (2) metallization requirements, (3) integrated circuit processing, and (4) long term stress.

Both single and multilayer metallization systems will be discussed as such, and as to their applicability to multilevel integrated circuit fabrication. Figure 1 shows a schematic of single metal, multilayer, and multilevel metallization.

A definition of terms used in figure 1 is as follows:

1. Silicon device-- a semiconductor made of silicon, and including metal contact, may be a bipolar transistor, a field effect transistor, a metal-silicon diode or an integrated circuit.
2. Metallization system-- the interconnecting metal pattern on a silicon device; the metal may be a single material (e.g. Al) or a composite sandwich structure, (e.g. Ti-Pt-Au). See figure 1 top.
3. Multilayer or multilevel metallization system-- two or more metal layers separated by dielectric layers and connected in such a manner as to optimize silicon device performance. Commonly used in large scale integration (LSI- see figure 1 middle and bottom)

METALLIZATION FAILURES

Before discussing specific metallization requirements and comparing various metal systems presently in use, we should be cognizant of the potential causes of metallization failures. It has been found that in some cases trends in integrated circuit design and processing technology may in fact increase the relative susceptibility of monolithic circuits to failure due to metallization-related mechanisms.

Metallization related failures observed to date are occasionally due to shorting, for example, reaction of metal with the substrate, under-etching or metal-metal shorts between layers in multilevel metallized arrays. However, the largest number of metallization related failures are due to *opens*. Table 1 enumerates the various causes of *opens* or localized reduced cross-sectional area in metallization. Quite often more than one cause or mechanism contributes to a given failure. For example, shadowing at steps can cause the localized cross-sectional area to be reduced, which in effect can produce excessively high current density and *opens* by electromigration. Figure 2 is a Scanning Electron Microscope micrograph of the shadowing effect.

TABLE 1.- REASONS FOR OPENS OR LOCALIZED REDUCED CROSS-SECTIONAL AREA IN MULTILEVEL METALLIZATION

1. Electromigration
2. Localized melting of metal due to excessive joule heating
3. Metallization scratches
4. Notches in the metal edge at steps
5. Microcracks at steps
6. Filamentation of metallization at steps
7. Tunnels under metallization at steps
8. Shadowing at steps
9. Fatigue effects
10. Stress cracking
11. Loss of adhesion
12. Over etching of metallization due to poor photoresist adhesion at a step
13. Photolithographic defects
14. Over etching of contact areas enhanced by electrolytic action
15. Inadequately opened contact windows
16. Residual oxide at metal-metal contact interface
17. Inadequate contact alloying
18. Overalloying (excess Al-Si interface penetration in the case of aluminum metallization)
19. Al-Si eutectic formation (applying to aluminum metallization)
20. Kirkendall effect
21. Corrosion effects

In considering maximum current densities for cross-sectional areas, important factors which should be taken into account are film thickness, line width, current crowding at corners, and various factors which influence the cross-sectional area of metal films in localized regions, including scratches, notches, micro-cracks and tunnels at steps produced during metal etch-back.

Other reliability factors unique to each metallization system include ability to form ohmic contacts to silicon, susceptibility to peeling and corrosion, temperature cycling effects, and bondability.

Many failures are a result of specific process conditions, rather than the inherent limitations of the materials involved. For example, in the case of Mo-Au layered structures, excellent high temperature reliability (300°C) and relatively low susceptibility to electromigration have been observed on some samples. Other samples have had problems with peeling, Au-Si interaction, undercutting and other effects.

Metal-dielectric interaction can be an important factor in the reliability of integrated circuits. The most commonly used dielectric is thermally grown SiO_2, but it must be realized that the extent of the interaction is determined by the exact nature of the oxide, prior processes it has been subjected to, and the presence of a borosilicate or phosphosilicate surface layer arising from the diffusion processes. Also, various deposited dielectrics including silicon nitride, aluminum oxide, and phosphosilicate glass are appearing in large-scale arrays.

In multilevel structures, procedures have been developed for insuring that the angle at the edge of a photolithographically defined cut in the oxide is not excessively steep. One technique described in the literature (ref. 2) uses a combination of r-f sputtered SiO_2 and chemically-vapor-plated SiO_2. The faster etching SiO_2 on top results in a less steep angle into the contact cut than would be obtained with a homogeneous SiO_2 film. Another procedure uses a single deposited dielectric layer in which the composition of the film is changed as deposition of the film progresses. The net result is a film in which the initially deposited layers have a lower etch rate than subsequently deposited portions of the layers. An example of a system which can be applied for this type of structure is vapor-plated phosphosilicate (the etch rate of phosphosilicate containing 3 to 4 percent by weight phosphorus in buffered hydrofluoric (HF) is approximately twice that of chemically-vapor-plated SiO_2 containing no phosphorus). Generally the metallization on such devices is aluminum. Among available developmental multilevel arrays, aluminum has most frequently been used for both first and second-level metallization. The molybdenum-gold system, modified to moly-gold-moly in each layer, has been used for multilevel metallized applications.

TABLE 2.- TEST DATA FOR SMALL CRYSTALLITE ALUMINUM FILMS

Film No.	Thickness (Å)	$J \times 10^{-6}$ (A/cm^2)	T (°C)	$\frac{10^3}{T^\circ K}$	MTF (Hours)	$\frac{10^{14}}{MTF\ J^2}$
AD	7400	0.5	177	2.22	480	0.83
BD	7060	1.21	186	2.18	47	1.45
CD	7000	1.5	195	2.135	19.5	2.28
DD	6800	2.82	238	1.96	3.5	3.70
AB	7400	0.5	192	2.15	250	1.60
BB	7060	1.22	200	2.11	38	1.80
CB	7000	1.5	212	2.06	8	5.55
DB	6800	2.88	260	1.87	1.5	8.03
BA	7060	0.987	109	2.62	850	0.121
CA	7000	1.46	121	2.54	268	0.175
DA	6800	2.05	134	2.48	183	0.130

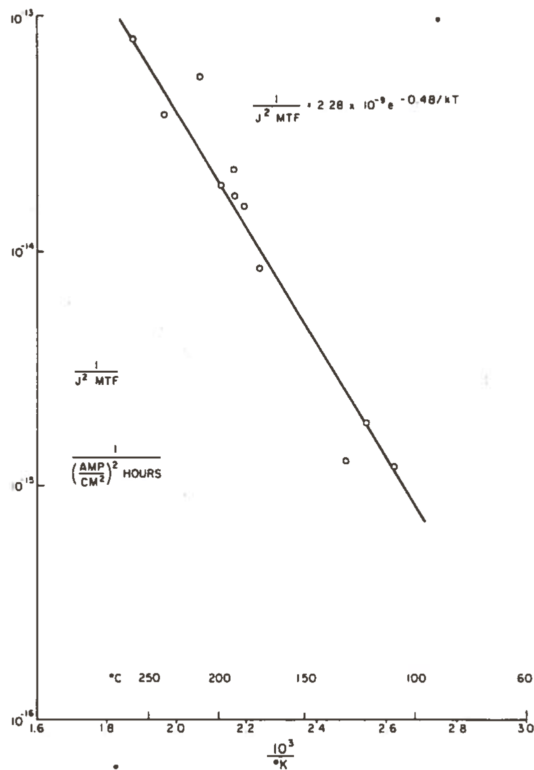


Figure 3.- Mean-Time-To-Failure as a Function of Current Density and Film Temperature: Aluminum Films Evaporated from Tungsten onto Cold Substrate

TABLE 4.- GLASSED LARGE CRYSTAL ALUMINUM PERFORMANCE

Film Thickness (Å)	Film Width (mils)	$J \times 10^{-6}$ A/cm^2	MTF Hours	$\frac{10^{15}}{J^2\ MTF}$	Film Temp.	$\frac{10^3}{K}$
12,200	1.46	0.908	1700	0.713	212	2.06
12,200	1.46	0.860	1060	1.28	221	2.02
12,200	1.43	0.870	395	3.33	246	1.93

TABLE 5.- GLASSED LARGE CRYSTAL ALUMINUM PREDICTED PERFORMANCE

Film Thick-ness (Å)	Film Width (mils)	$Jx10^{-6}$ (A/cm^{2}p)	Esti-mated MTF Hours	$\frac{10^{15}}{J^2MTF}$	Film Temp. ^oC	$\frac{10^3}{^oK}$	Sample Size	No.of Fail-ures	Hours on Test
12,200	1.46	0.777	5,400	0.306	203	2.10	15	7	3900
12,200	1.46	0.702	12,000	0.170	189	1.16	13	2	2590
12,200	1.46	0.460	16,000	0.295	200	2.11	13	1	2333

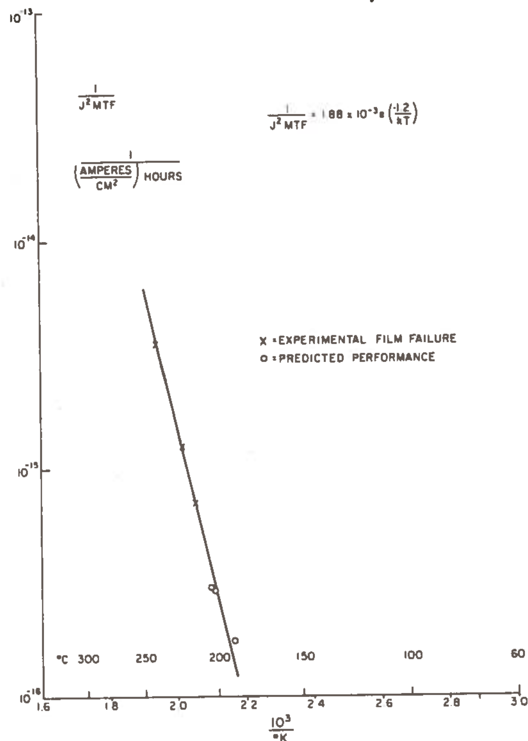


Figure 5.- Mean-Time-To-Failure as a Function of Current Density and Film Temperature: 1.46 Mil Wide by 12,200 A Thick, Well Ordered Aluminum Coated with 6000 A Thick Glass Film

TABLE 7.- TEST DATA FOR LARGE CRYSTAL ALUMINUM FILM CONDUCTORS OF VARIABLE THICKNESS

Film Thickness (Å)	Film Width	Film Cross-sectional area ($cm^2 \times 10^8$)	$J \times 10^{-6}$ (A/cm^2)	T (^oC)	$\frac{10^3}{T(^oK)}$	Experimental MTF	Calculated MTF	Volume Resistivity ohm-cm $\times 10^6$
2017	.63	3.22	2.010	204	2.100	24	21	6.02
2068	.66	3.46	1.780	204	2.10	35	16	7.05
2440	.57	3.53	2.07	200	2.115	36	14	4.82
3320	.52	4.38	1.560	192	2.15	33	45	3.53
3840	.58	5.66	2.175	206	2.09	11	17	3.42
8838	.51	11.42	1.477	202	2.10	80	80	3.05
9455	.43	10.32	1.457	200	2.115	62	86	3.06
10500	.39	10.40	1.460	200	2.115	100	87	3.04
12540	.42	13.38	1.655	222	2.02	38	35	3.11

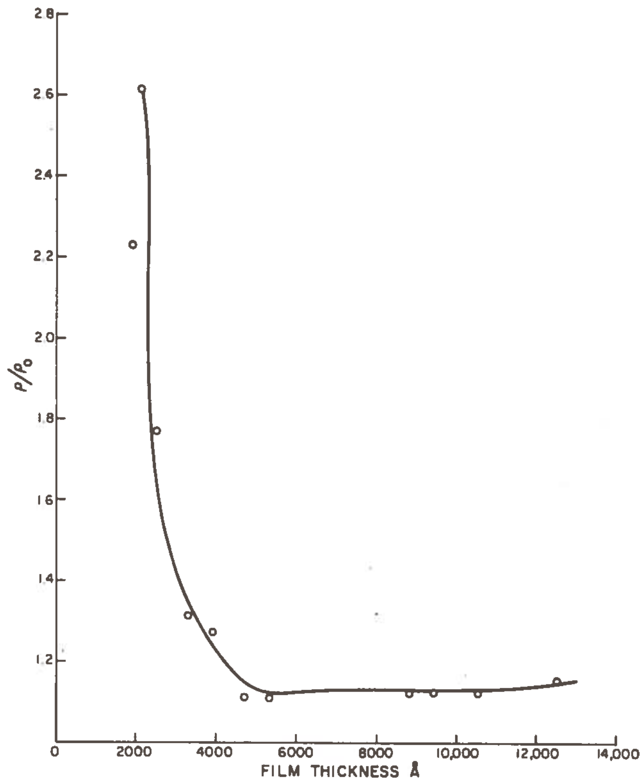


Figure 8.- Aluminum Film Resistivity Normalized to Bulk Resistivity as a Function of Film Thickness

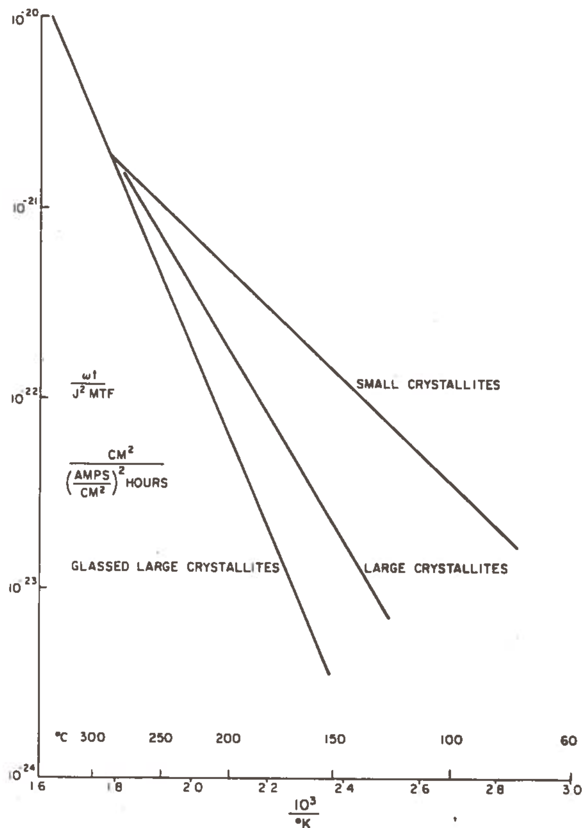


Figure 9.- Mean-Time-To-Failure for Aluminum Film Conductors as a Function of Current Density, Temperature and Cross-sectional Dimensions

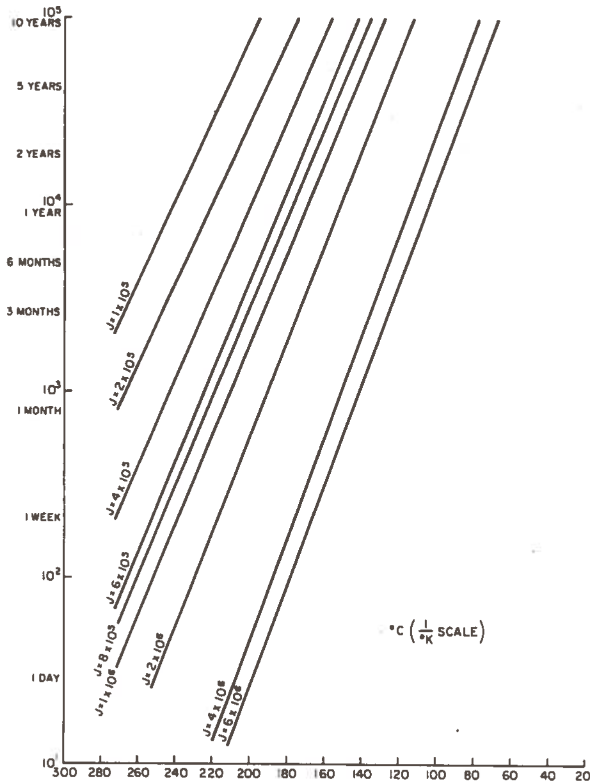


Figure 12.- Glassed Large Crystallite Aluminum Film Lifetime for Conductors with a Cross-section of 10^{-7} cm^2

Etch Pits

A failure mode common in aluminum silicon contacts is the growth of etch pits into the silicon at the positive terminals (ref. 5) under high current density and temperature stress. The pit formation may not be obvious prior to removal of the aluminum. The formation is believed to be due to the dissolution of silicon into aluminum to saturation and the transport of the dissolved silicon by momentum exchange, enabling further dissolution of aluminum. At 235°C about 0.003 weight percent of silicon can exist in solid solution with aluminum. Because silicon will preferentially enter aluminum at crystalline dislocations, rather than uniformly over the interface, the process results in the formation of etch pits. The process can continue until the junction beneath the aluminum-silicon contact is electrically shorted.

Aluminum-Silicon Reaction

Another failure mode is the reaction between aluminum and silicon dioxide. The reaction is initially important in device fabrication to effect good ohmic contact; but this reaction may play in the degradation of the reliability of devices under stress and at elevated temperatures. Figure 13 presents a plot of the

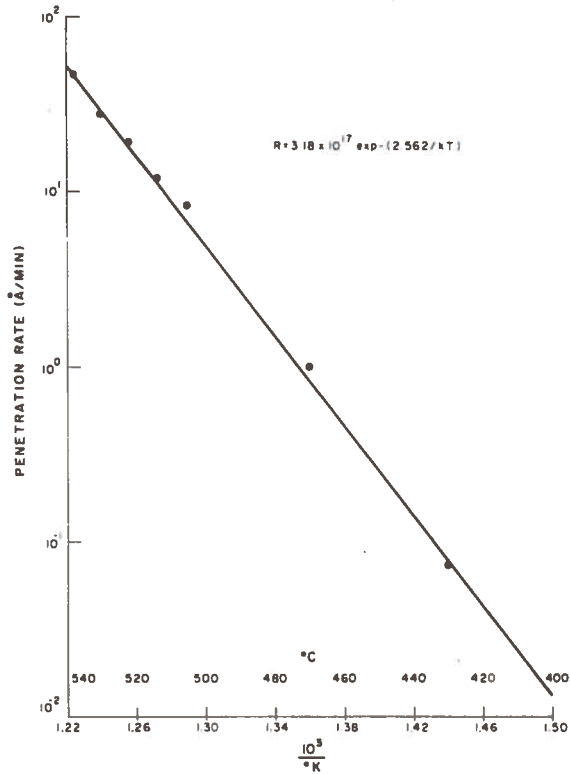


Figure 14.- Penetration Rate of Aluminum Reaction into Thermally Grown SiO_2 as a Function of Temperature

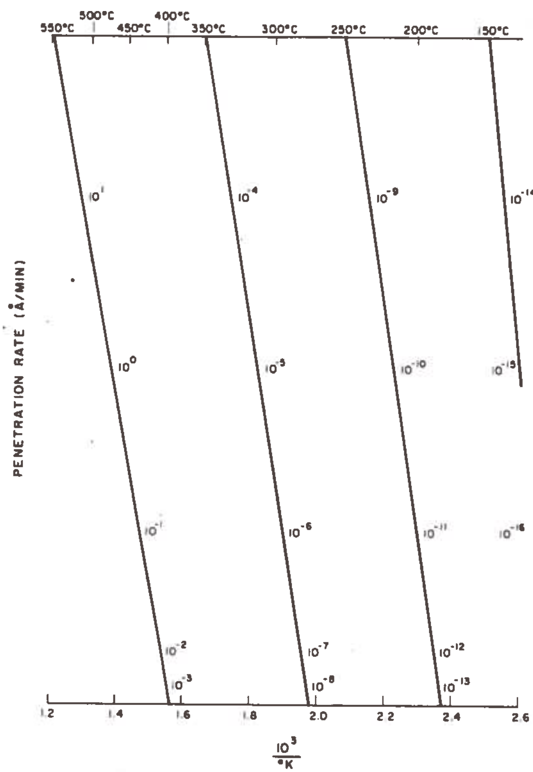


Figure 15.- Penetration of Aluminum into SiO_2 Extrapolated to Lower Temperature

Even in systems which do not form compounds, diffusion of one metal into another can result in contact resistance increasing by orders of magnitude. This failure mode is more serious than generally realized and this type of deterioration is usually not recognized during the early stages of device design and manufacture. Diffusion can occur through any of several processes, including vacancy, interstitial dislocation, and grain boundary mechanisms. The predominant diffusion mechanism depends on the type, temperature, structure and geometry of the metallurgical system.

Diffusions have been observed to occur in Ag-Pb, Au-Cr, Au-Ti, Cr-Ni, Cu (NiCr), Cu (Pb-Sn), Ti-Al-Si and Ti-(PtSi). Compounds have been observed to form in Al-Ni, Al-Ta, Au-Ti, Au-(NiCr), Au-(Sb-Sn), and Ti-Al-Si (ref. 8).

Metal-Oxide Interaction

Metals are known to interact with oxides as a result of solid-state reactions at elevated temperatures, and this type of interaction has been shown to occur with aluminum on SiO_2 and on phosphosilicate glasses. Adverse effects can result from this interaction on any type of circuit, but circuits with thin oxide regions are particularly susceptible. For example, the oxide over gate regions of MOS transistors is typically 0.1 to 0.15 microns thick. Accordingly, an important attribute of a metallization system for MOS integrated circuits is the ability to adhere well to oxide but not to react extensively with the thin SiO_2 layer under the gate metal region. There is also a similar requirement for capacitors in bipolar circuits, where such capacitors frequently have 0.1 micron thick oxide, prepared either by anodization or by thermal oxidation. Electrical shorts in MOS structures have been attributed to a solid-state reaction between the electrode metal and SiO_2. The details of oxide preparation can also be a major factor in determining the incidence of such electrical shorts at temperatures of 500°C.

Dielectrics other than SiO_2 are also used at times in integrated circuits. In particular, silicon nitride has been used in a number of types of integrated circuits, and aluminum oxide has been used in MOS circuits. Aluminum adheres well to both of these dielectrics, and has less tendency to react with silicon nitride at elevated temperatures than with SiO_2.

Thermal Stresses

Any metallization system used for integrated circuits must form continuous conducting lines which go up and down steps resulting from topography in the integrated circuits. In bipolar circuits, steps arise at contact cuts to the emitter regions, collector regions, and base regions, as well as between different

Scratches in Metallization Stripes

Aluminum and gold, being soft, are quite susceptible to the possibility of scratch formation during device fabrication. Scratches typically would form during the steps of scribing, breaking, and handling the chips to mount them on headers. Harder metals such as molybdenum and chromium are considerably less susceptible to scratches during handling. On the other hand, their lower ductility can result in problems if relatively thick layers are used and are processed through temperature cycles. The problem of scratches in the aluminum metallization can to a very large extent be solved by the process of depositing a dielectric layer over the aluminum prior to scribing. The additional steps required to accomplish this include vapor plating the oxide, typically at 400°C, and using photolithographic techniques to open up areas of the contact pads prior to bonding. The deposited dielectric in this case causes significant improvements in yield through the process and also considerably less susceptibility to reliability problems as a result of scratches and smears of the metallization. Glassing also has the merit of protecting the patterns of closely spaced, adjacent current carrying stripes from corrosion effects, either electrolytic or chemical, and imparting additional freedom from the possibility of shorts due to particles which might bridge between conducting metal stripes. With glassed circuits the only exposed metal is in the area of bonding pads. The spacing between such areas is considerably greater than that between lines in the circuits. Since SiO_2 adheres to aluminum, a wide range of thicknesses of glass can be used.

Deposited dielectrics generally have poor adhesion to gold. Thus wafers in which the top layer in the metallization system is gold are difficult to protect with deposited dielectric unless thick glass layers are used or an additional layer such as chromium or molybdenum is put on top of the gold.

METALLIZATION SYSTEMS

The metallization systems in use today for fabrication of integrated circuits in production can be divided into those used with single-level metallized circuits and those used for multilevel systems containing two or more levels of metallization. The most common metal used in single-level metallization systems is aluminum, and the most common metals used in the layered composite systems are molybdenum-gold and titanium-platinum-gold. All three systems are used in the fabrication of commercially available bipolar integrated circuits. The titanium-platinum-gold system is used in beam-lead fabrication. The systems Al-Si (homogenous) and Ti-Al (layered) are also in use. For MOS integrated circuits, a number of metallization systems are currently in use.

Table 9 shows the theoretical bulk value resistivity for the better electrical conductors and the ohms per square for a film of this geometry. The total resistance of such a conductor running 10 mils in length is also given. It should be remembered that metals, in general, when deposited as films, exhibit volume resistivities greater than the theoretical bulk resistivities making the table somewhat optimistic.

TABLE 9.- RESISTIVE PROPERTIES OF VARIOUS METALS

Metal	Theoretical Volume Resistivity in Micro-ohm-cm	Ohms/Square for 6000 Å Thick Film	Resistance of a 10 mil Long Conductor, 2 Microns Wide X 6000 Å Thick (ohms)
Ag	1.61	2.7×10^{-2}	3.4
Al	2.74	4.6×10^{-2}	5.8
Au	2.44	4.1	5.2
Cu	1.70	2.8	3.5
Be	3.25	5.42	6.9
Mg	4.3	7.2	9.1
Mo	5.3	8.8	11.2
Rh	4.7	7.8	9.9
Ni	7.8	13.0	16.5
W	5.3	8.8	11.2

Chemically, the metallization must resist deterioration in oxygen at 500°C to survive the post metallization processing steps. Therefore, a metal which produces a thin continuous protective oxide inhibiting further reaction is desirable. Such metals generally are those in which the oxide is less dense than the parent metal. The oxide must also possess a low vapor pressure and must not deteriorate under humid conditions.

The first layer of metallization must act as a reducing agent for silicon dioxide to reproducibly make ohmic contact through the thin oxide layer that readily forms on silicon. When considering the use of multilevel metallization, it is desirable that the metal does not react sufficiently with the dielectric to form conductive electrical paths between the metal layers at the crossover points. It is therefore necessary that the metal be only slightly a reducing agent and that the temperature at which the reduction takes place be reached rapidly and only once to form

Fabrication Processes

It is very important in the selection of a metallization system to consider the processing steps required in the fabrication of an integrated circuit. These steps are:

1. Deposition of metallization (silicon containing p-n junctions and dielectrics is heated to 200-500°C prior to vacuum deposition and deposition times range from 10-20 minutes for each metal)
2. Heat treatments (5-15 minutes at 300-500°C to insure good ohmic contacts)
3. Glass deposition (200-500°C for 10-20 minutes)
4. Application of solder or eutective bonding material on back of silicon wafer (5 minutes at 200-500°C)
5. Bonding chip to header or package (5 minutes at 400-500°C)
6. Lead bonding (room temperature to 350°C)
7. Sealing package (5-30 minutes at 200-500°C)
8. Operational life stress tests at elevated temperatures (300°C for 1000 or more hours.)

Single Metal Systems

Aluminum is the predominant metallization system used in the fabrication of silicon integrated circuits for the following reasons: (ref. 10)

1. Aluminum can be used in a single-metal system which provides considerable simplicity compared to multimetal systems
2. Aluminum is a low-cost source material
3. Aluminum films have a high electrical conductivity, close to that of the bulk material
4. Aluminum evaporation by a resistance heated tungsten coil is simple
5. Aluminum adheres well to oxides
6. Aluminum layers delineate well by photolithographic techniques
7. Aluminum is easily etched without dissolving SiO_2 or silicon
8. Aluminum reacts with residual SiO_2 in contact areas
9. Aluminum forms low-resistance contacts to n^+ silicon and p-type silicon
10. The solid solubility of silicon in aluminum is such that Al-Si alloys can be used to adjust the amount of penetration at alloying and reduce the amount of penetration as compared to that of pure aluminum
11. There are no compounds in the Al-Si system; thus brittle compounds are not possible, and void formation (Kirkendall effect) has not been a problem at Al-Si interfaces

6. Aluminum recrystallizes at fairly low temperatures causing hillocks of metal which could break through a dielectric or be difficult to cover
7. Reaction of aluminum and SiO_2 can be significant at temperatures of about 500°C
8. Aluminum forms compounds with gold which tend to be brittle and result in decreased electrical conductivity
9. Gold wire bonded to aluminum results in reliability problems due to the Kirkendall effect
10. Aluminum is soft and easily scratched
11. Silicon dissolved during contact alloying may precipitate at grain boundaries in aluminum and cause reliability problems
12. Aluminum is typically under stress as deposited
13. The thermal coefficient of expansion of aluminum is greater than that of silicon which results in considerable stress in aluminum during temperature cycling
14. In multilevel metallization structures, the problem of making good aluminum-aluminum contacts has not been completely solved
15. Aluminum is electronegative and corrodes in electrolytes
16. Aluminum is not directly solderable by conventional soldering techniques
17. Aluminum has a higher work function than some metals, and thus results in higher threshold voltages in MOS devices
18. Aluminum dissolves to a small extent in solutions used to etch contacts in deposited dielectrics in multilevel-metallized structures.

High Current Density Tests

High current density tests on aluminum metallization as conducted at 100°C, 150°C, and 175°C and current levels (1-2 x $10^6 A/cm^2$ yielded results shown in Table 10.)

Table 11 presents Mean-Time-To-Failure for aluminum metallization as a function of resistivity and current density.

Examination of the failures showed a single dominating failure mode, i.e. a random opening of the interconnection, occurring in a porous rough-textured metal. During the processing, the aluminum is subjected to 450°C for perhaps 30 minutes, and changes from a smooth, nonporous film, beginning to develop a characteristic roughness. This roughness and porosity can be increased by subsequent thermal treatments. The intentional addition of moisture to the dry air furnace has no significant effect. The same rough texture is reported to appear in high current density tests in dry nitrogen sealed To-5 cans. The proposed failure mechanism is that a thermal reaction causes a porosity and reduced cross-sectional area, with a localized increased current density.

TABLE 11.- MEAN TIME TO FAILURE FOR ALUMINUM METALLIZATION AS A FUNCTION OF RESISTIVITY AND CURRENT DENSITY

$J = 10^6$ A/cm^2	0.5	1.0	1.2	1.5	2.0	2.8
= 2.6 - cm*	---	1500 hours		--	69	--
= 4.0 < cm	---	470	--	--	25	--
= 6.0 - cm	---	130	--	--	13	--
All available data	480	560	17	20	30	4

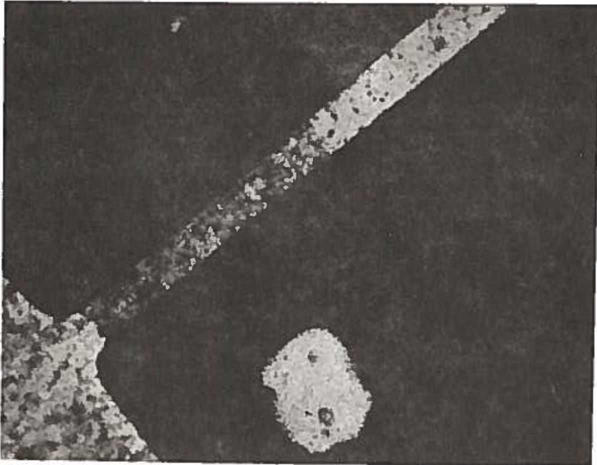
*Resistivity varied by deposition rate

This causes localized hot spots and accelerated reaction at these sites. Failure occurs when the voids form continuous breaks across the strip. This is illustrated in figure 16. The 1/2 mil strip was heated 48 hours at 450°C in wet air.

Additional experiments demonstrated the thermal nature of the reaction. Devices with 1/2 mil lines were tested at 2×10^6 A/cm^2 and an oven temperature of 175°C. These units had normal processing, i.e. gold backing, bonding, and To-5 packaging. The mean time to failure was 25 hours. A second group was prebaked at 450°C for 2 hours prior to the high current tests. These units had a mean time to failure of 24 hours. A third group was prebaked 8 hours at 450°C before the high current tests. The mean time to failure was reduced to 15 hours. The aluminum metallization included vacuum evaporated metal using tungsten filaments, tantalum filaments, and electron beam heating. Both normal (10^{-6} torr) vacuum and high (10^{-8} torr) vacuum samples were included. The films were approximately 6000 Å thick, and were generally deposited from 1-10 minutes. All the aluminum tested showed the thermal changes described.

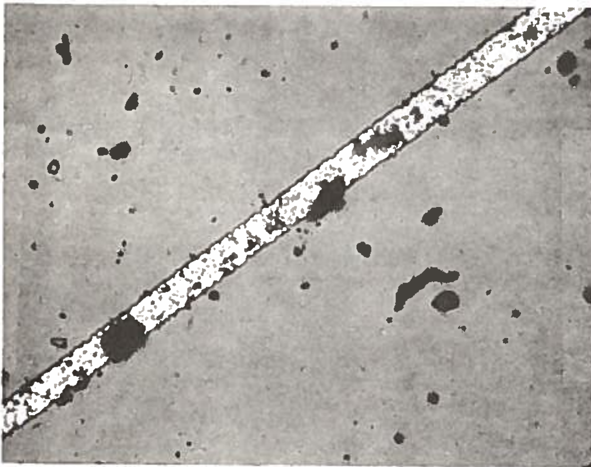
Current induced metal migration is the problem resulting from induced high current density stress. The failure depends on the structure of the film, but lifetime is generally related to the current density by some form of the equation:

$$L = AJ^{-2} \exp. \Phi/KT$$



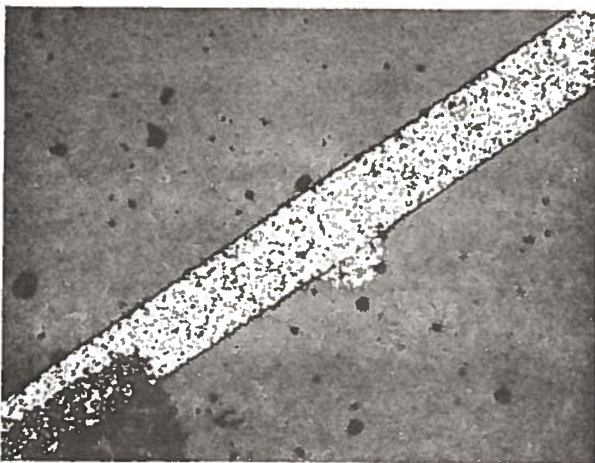
800X

0.5-Mil Line After 48 hrs
450°C



800X

0.5-Mil Line 10^6 A/cm^2
1150 hrs Film Temperature
~180°C



800X

1-Mil Line - No Current

Figure 16.- Photomicrographs of Aluminum Lines

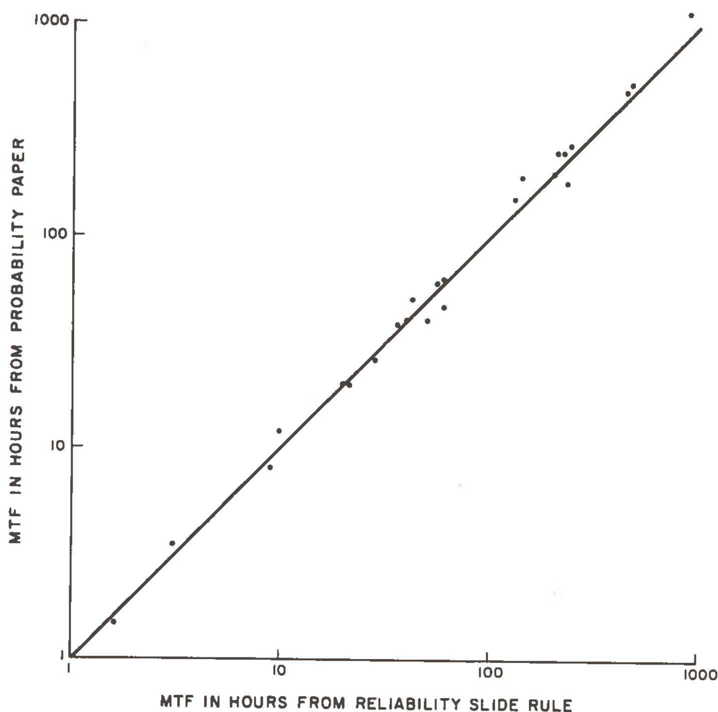


Figure 18.- Correlation Plot Comparing Mean-Time-To-Failure from Distribution Plots and from Reliability Slide Rule

TABLE 12.- DEPOSITION DATA AND PROPERTIES OF W AND Mo

	RF Sputtered		Electron-Gun
	Mo	W	Mo
Deposition Rate	250 Å/min	100 Å/min	10-20 Å/sec
Substrate Temperature	200°C	200°C	200°C
Deposition Pressure	5 microns	5 microns	10^{-6} to 10^{-5} torr
Film Resistivity	15 micro-ohm-cm	25 micro-ohm-cm	30-40 micro-ohm-cm
Adherence	Fair	Fair	Marginal
Ohmic Contact (Si)	Fair, but difficult to reproduce		

Poor adherence to SiO_2 eliminates the high conductivity metals, e.g. Au, Ag and Cu, as single layer systems. It therefore appears that no single layer system will replace aluminum.

TABLE 13.- RESISTANCE OF VARIOUS METAL(S) AFTER AIR BAKES, 1- x 54-MIL CONDUCTORS, ALLOY TESTS ARE ON 20-MIL^2 CONTACTS

Metals and Thickness (First Layer ↓, Total Film ↓)	Resistance, 1-mil x 54-mil conductor, after							
	450°C				650°C			
	Int.R	2 Hrs.	4 Hrs.	Au-Si Alloy	Int.R	2 Hrs.	4 Hrs.	Au-Si Alloy
Al 7000Å	2.7	2.6	2.7					
Cr-Au 2000, 6500Å	5.8	17.4	19.0	100% at 1 Hr.				
Ti-Au 2000, 6500Å	5.4	12	18	100% at 1 Hr.				
V-Au 800-9900 Å 1600-6600 Å	1.7 Ω 3.5	3.6 Ω 7.1	3.6 Ω 5.9	300/400 after 1 Hr.	1.7 Ω 3.6	6.6 Ω 8.3	5.6 Ω 9.5	100% after 30 min.
(Ti-Pt)-Au 3000, 9000Å	2.9	4.0	4.3	0/120 at 4 Hrs.				
Mo-Au 2100, 10000Å 2700, 7200Å	3.2 3.1	2.5 2.8	2.5 2.8	1/400 at 4 Hrs.	2.7 3.2	2.3 2.7	2.3 2.8	12/400 at 4 Hrs.
W-Au 1400-6600 -7200	2.6 3.4	2.6 2.8	2.5 2.7	2/400 at 4 Hrs.	2.5 3.3	2.5 2.7	2.4 2.74	6/400 at 4 Hrs.
Ti-Mo-Au 500, 1500Å 5500Å	5.6	5.7	5.7		5.3	4.8	5.0	
W-Au-Ti -300Å (Ti)	4.9	3.4	3.2		4.7	2.7	2.6	

The as-deposited resistivity of the Cr-Au composite films ranged from 6-15 micro-ohm-cm due probably to the relative amount of Cr and Au in the composite film. Increases in resistance after 450°C air bake are shown in figure 19. It is interesting to note that the resistances of films with Cr thicker than 1000 Å increases 200-600 percent within an hour at 450°C and then tapers off. The films with heaviest interface blending (second metal deposition started before the first metal is completely deposited), tend to increase more. Recent studies of Cr-Au (ref. 1) have noted resistance increases as large as 170 percent after 50 hours at 350°C in nitrogen ambients. The results found on sputtered Cr-Au are similar, and the magnitude of the resistance increase is too large to be a simple oxidation of Cr from under the Au. The more plausible explanation lies in the solid state diffusion of Au into the Cr (or Cr into the Au), which results in the formation of a higher resistance intermetallic compound.

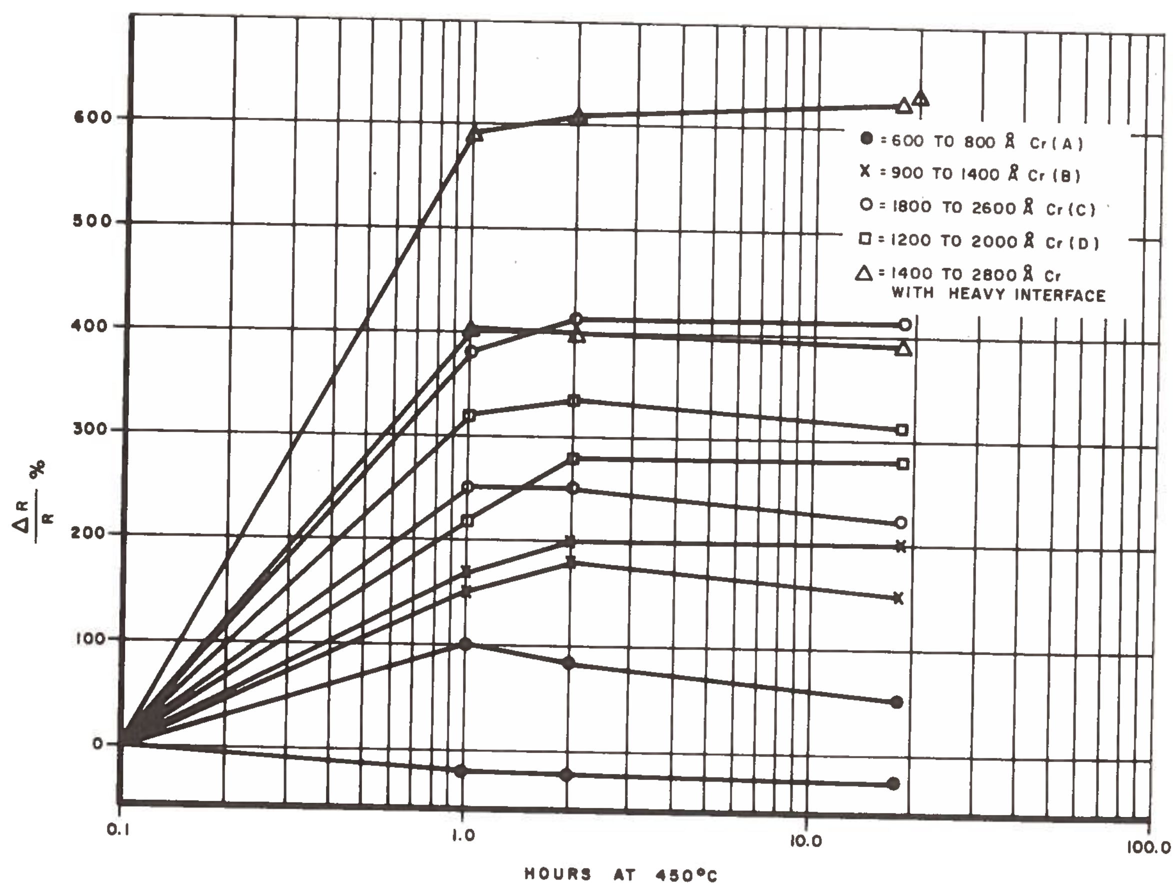


Figure 19.- Resistance Change in Cr-Au Films, Au Thickness 5000 Å

1 mil wide and 54 mils long, the remaining Ti was removed by chemical etching in a dilute H_2SO_4 solution. The wafers containing the etched patterns were then scribed into three pieces. Measurements were taken, samples were baked at 450°C in air, and remeasured at one hour intervals for 24 hours. The resistance of Pt-Au composite films increased with time at 450°C. The changes shown in Table 14 are scattered, but there is a trend indicating that films containing both small and large amounts of Pt have less of an increase than an intermediate composition film.

TABLE 14.- ΔR OF Pt-Au FILMS WITH 450°C AIR BAKES

Platinum, Percent of Film	Initial ρ Micro-ohm-cm	+ΔR After 2 Hours Percent	ΔR After 4 Hours Percent	T_{Au} (Å)	T_{Pt} (Å)
23	3.7	75	90	11,000	3,300
25	3.6	120	150	6,700	2,300
25	3.6	110	135	6,700	2,300
27	4.6	150	160	4,350	1,650
31	4.5	120	150	5,600	2,500
32	4.6	150	150	4,100	2,000
35	4.6	125	143	6,000	3,300
50	7.6	115	120	1,650	1,650
70	9	125	130	1,100	2,500

The Pt-Au films, after 24 hours at 450°C, were heated to 1000°C for 30 minutes in forming gas to permit them to proceed to a more complete reaction and the final resistance was measured at room temperature. Table 15 compares the experimental resistivity data on Pt-Au after the 1000°C bake with various literature values (refs. 21 and 22) and shows fair agreement. These results indicate that the layered Pt-Au film resistivity can increase by a factor of 10 if complete alloying occurs. The results also show that the resistance change of Pt-Au composite films will be smallest for Pt concentrations less than 35 atomic percent. Hence, the Pt thickness in Pt-Ti-Au should be as thin as possible consistent with retaining the barrier between the Au and the underlying silicon.

The Ti-Pt system likewise undergoes a resistance increase upon thermal treatment at 450°C. As presently used in Ti-Pt-Au systems, the Ti is about 2000 Å and the Pt is 2000 Å. The resistivity of the sputtered Ti is 200 micro-ohm-cm and the sputtered Pt is about 25 micro-ohm-cm. The resistance of a

The previous discussion indicated that for a minimum change in resistance the volume ratio of Au-Pt should be large or the Pt should be as thin as possible, consistent with preventing the Au from reaching the Ti. This minimum Pt thickness was sought in a series of Au-Si alloying tests in which the Pt thickness ranged from 450-2100 Å. The contacts, consisting of Ti (1500 Å)-Pt-Au (7000 Å) on 20 mil^2 and 100 mil^2 areas of silicon, were baked at 450°C for times ranging from 15 minutes to 4 hours. The test results are summarized as follows:

1. After 4 hours with 450 Å Pt, 10 out of 120 large areas and 5 out of 120 small areas alloyed
2. With 2100 Å Pt, 1 out of 120 large areas and none out of 120 small areas alloyed after 4 hours
3. No well defined minimum Pt thickness existed which would prevent Au-Si alloying
4. Larger areas alloyed first for a given Pt thickness.

The area dependence indicated that pinholes in the Pt were more important than solid-solid diffusion. Assuming that pinholes are the major problem,then the Pt should be as thick as possible to reduce the probability of pinholes, and the Au made correspondingly thicker to reduce thermally induced resistance changes.

Summarizing, the Ti-Pt-Au system can increase in resistance in 450°C bake cycles. This resistance increase is caused by interdiffusion of the Au and Pt. Still,the system can be extremely useful at temperatures of 450°C by making the volume ratio of Au/Pt greater than approximately 3/1. 1500 Å to 2000 Å of Pt is effective in preventing Au-Si or Au-Ti reactions at 450°C.

<u>Cr-Ag-Au and Ti-Ag-Au</u>.- In these systems the Ag and Au behave similarly to the Pt-Au in that the Au and Ag form a continuous series of solid solutions and the resistivity increases drastically during heat treatment. This is in agreement with published values for Ag-Au alloys. For example, Mott and Jones (ref. 21) show the resistivity of a 50 atomic percent alloy to be 24 micro-ohm-cm compared to 1.61 for pure silver and 2.44 for pure gold.

In general, experimental data on Cr-Ag-Au as compared to Ti-Pt-Au, show that the Cr-Ag-Au resistivity after several minutes of 450°C bakes is higher, and that Ag-Au interdiffusion can occur as low as 350°C in a relatively short time. The initial values of resistance in the Cr-Ag-Au system are higher than expected from known individual film resistivities indicating a reaction has already taken place during deposition and subsequent processing. Table 17 shows typical resistance changes obtained on Cr-Ag-Au and Ti-Ag-Au. In both systems the Ag is effective in preventing the Au-Si eutectic formation.

Mo-Au and W-Au.- As additional composite metal systems, Mo-Au and W-Au systems have been considered. In the Mo-Au system as with the other refractory metal-gold systems the thickness of the molybdenum film is considered critical. In one set of experiments to investigate the thermal stability of the Mo-Au system, the molybdenum thickness was varied from 500 Å to 8200 Å. No resistance increases were found after four hours at 450°C, provided the ratio of Au/Mo was greater than about 3/1 and no interface mixing of the Mo and Au was used during deposition. In films which had blended interfaces during deposition and thin Au (1500 Å Au/2000 Å Mo), the resistance increased 20-50 percent after four hours at 450°C. Using relatively good vacuum of 10^{-6} to 10^{-5} torr and sequential deposition of the Mo and Au in the same pump down, the Au to Mo adherence is excellent and no interfacial blending is necessary to promote adherence. It has been reported in the literature (ref. 23) that the thermal behavior of sputtered and electron-gun Mo covered with filament-evaporated or low pressure triode sputtered Au are similar in that no increases in resistance are observed. However, it was noted that the low pressure triode sputtered Au had 2-3 times the resistivity of the evaporated Au (ref. 23). The high Au resistivity is attributed to scattering at grain boundaries. The gold films contain extremely small crystallites due to a large number of nucleation sites which are enhanced by the sputtering mode of deposition. Using 2100 Å of Mo prevents Au-Si alloying at 450°C.

The Mo-Au and W-Au systems behave similarly in thermal stability tests even after 4 hours at 625°C. Any resistance change was less than 5 percent and it usually decreased, indicating an annealing effect. Tungsten is as effective as molybdenum as a barrier metal.

Unfortunately, the adherence of both Mo and W to SiO_2 is marginal, so an additional adherent layer is sometimes used. Titanium has worked as an excellent "glue" for these materials. Even with the titanium, the thermal stability of Ti (500 Å)-Mo or W (2000 Å) and Au films is satisfactory. Data on typical films are summarized in Table 19.

Ni-Au or Co-Au.- The behavior of these films is not similar to any of the others discussed. A slight reaction between the metals occurs; but tests show that after one hour at 450°C the surface of the Au becomes discolored and the film is hard and rough. This could make wire bonding difficult. In the case of Ni-Au the nickel did not prevent Au-Si alloying.

Resistance Change and Au-Si Alloying

Some fairly comprehensive data are summarized in Table 20. Combining results from tests along with adherence properties and fabrication difficulties indicates that no one system will meet all requirements listed in the previous section.

TABLE 20.- SUMMARY, RESISTANCE CHANGE AND Au-Si ALLOYING

Metals Examined	+ ΔR at $450^{\circ}C$ 2 Hours	Au-Si (1 hour at $450^{\circ}C$) Alloying
Al	0	
Ti-Pt	0	
Ti-Rh	0	
Ti-Pt-Au	<50 percent	No
Ti-Ag-Au	>100 percent	No
Ti-Mo-Au	0	No
Ti-Ag	5-10 percent	
Cr-Ag-Au	>100 percent	No
W-Au	0	No
Zr-Au	<50 percent	Yes
Nb-Au	<100 percent	No
Ni-Au	<100 percent	Some
Co-Au	<50 percent	Some
V-Au	>100 percent	Yes
Ta-Au	<50 percent	Some
Cr-Au	>100 percent	Yes
Ti-Au	>100 percent	Yes
Mo-Au	0	No
Hf-Au	<50 percent	Some

In general, the systems which most nearly meet these requirements may be separated into two groups:

1. Those destined for low temperature applications, e.g. beam leads or plastic encapsulation
2. Metallization for systems requiring relatively high temperature long processing schedules, LSI multilayer systems.

CONTACT RESISTANCE

The amount of contact resistance and linearity of resistance introduced by a metallization process is an important problem in the successful fabrication of integrated circuits. This section summarizes the results of contact measurements using metal layers of Al, Cr, Mo, Ni and Ti; with and without a platinum silicide layer on both N and P type silicon. The PtSi process used here is similar to the process described in reference 20.

Experiments were conducted on N and P type silicon samples with approximately 5000 Å thermal oxide, photomasked and 4 x 5 mil contact areas spaced approximately 4 mils apart etched through the glass down to the silicon. The various metals were deposited by a filament evaporation, electron beam evaporation, or low pressure dc sputtering.

The measurement technique included probing four adjacent metallized pads, two with the DVM leads and two with the constant current leads. The contact resistance as measured included the effects of spreading resistance (ref. 24). To check for non-linearity, measurements were made at 10 and 100 mA. and visually monitored on a transistor curve tracer. These results are shown in Table 21 and represent the average from several runs. Generally, values were reproducible to better than ± 25 percent.

The data of Table 21 shows that various metals have low ohmic contact resistance on low resistivity n and p type silicon. As the silicon resistivity increases, the contact resistance increases, as does the nonlinearity. All of the metals exhibited rectifying contacts on n type silicon above about 0.01 ohm-cm. Although the contact resistance increases, the Al p-type silicon contacts are ohmic at least up to 1 ohm-cm particularly after a mild bake, ($450^{\circ}C$ - 10 minutes). It is of interest to note that this same heat treatment increases the contact resistance of aluminum on n type silicon (0.1 ohm-cm).

The use of Pt-Si is known to lower the contact resistance regardless of the metal used, especially on mid-resistivity n type silicon, where an order of magnitude reduction is obtained. The resistance values for the various metals on PtSi-Si is almost independent of the metal used, suggesting that the potential barrier is in the PtSi-Si region. An independent measurement of the resistivity of PtSi shows that it is approximately 100 micro-ohm-cm (bulk Pt = 10 micro-ohm-cm). For the areas of the contacts used, this yields a figure of 10^{-5} ohms and therefore would not be detected in these measurements.

In addition to lowering the contact resistance, the PtSi yields ohmic contacts to higher silicon resistivity. For example,

the Al-N-Si contacts rectify at 0.01 ohm-cm. This figure is increased to approximately 0.05 ohm-cm for Al-PtSi-N-Si.

In the early use of platinum contacts it became obvious that the silicon must be as free as possible of oxide and contaminants if the platinum is to form the silicide. The platinum silicide process used includes:

1. the deposition of platinum after a pre-ohmic etch, with either an electron gun or sputtering.
2. Sintering at 600-700°C to form the silicide.
3. Chemically removing the excess platinum from the SiO_2 masked surface.

Since platinum will not reduce the silicon oxide it is imperative that silicon in contact areas be oxide free. If this is not the case then the PtSi will not form.

TEMPERATURE STABILITY

Air bakes at 450°C for 15 minutes generally lower the contact resistance (but rarely more than 50 percent) if the surface is clean and proper shielding of the substrate is used during the initial evaporation or pre-sputter. An exception to this was aluminum on n-type silicon, where the resistance increased 25-50 percent during the bakes. In general, the changes were less on PtSi units. Evidence of the stability of metal PtSi contacts is shown in Table 22. These data compare the contact resistance obtained on AlSi and Al-PtSi-Si contacts with heat-treatment, and indicate the stability of the PtSi at elevated temperatures. Other tests conducted, with MoAu on PtSi-Si contacts, also showed extremely stable behavior on long term storage at 250°C.

CURRENT DENSITY

In this section various metal systems in use will be discussed as to current density capabilities and high temperature operation reliability. In each case the results will be compared to relative data on aluminum metallization.

Chromium-Gold

Some chromium-gold test results are given in Table 23. Related groups are averaged to increase the sample sizes. The mechanism of the chromium-gold failures was discussed previously in reference to the thermally induced resistance rise. The observed doubling of the conductor resistance in 500 hours at about 220°C is in agreement with the self-diffusion energy for gold, or about 1.8eV. Although the resistance rise occurred in all samples, including those not carrying current, many of the samples continued to conduct for many hours, although with increased power dissipation. Eventually, burnout occurs. Glassing of the chromium-gold system did not improve the life at the lower current levels, but merely accelerated the resistance rise mechanism by the elevated temperature processing.

Chromium-Silver-Gold

As indicated in the thermal testing section, the addition of silver to the chromium-gold metallization improves the thermal stability. Samples under discussion were prepared with 22 percent silver by volume of the gold. The films were patterned and glassed. The resistivity rose to 15 micro-ohm-cm for the encapsulated units. Current density tests at $2x10^6$ A/cm^2 and 222°C gave a mean-time-to-failure of 600 hours. A sample at $1x10^6$A/cm^2 and 195°C gave an estimated mean-time-to-failure of 6700 hours. These failures are both of the catastrophic open and the resistance increase type. Since these samples have high resistivities, and were glassed, a direct comparison with the chromium-gold binary system is difficult. However, it appears that there is a significant improvement in the lifetime over the chromium-gold system, although the mechanism of failure is similar.

Titanium-Gold

The titanium-gold metallization results have been promising at current levels greater than $2x10^6$A/cm^2. A study of the titanium-gold metallization system and its thermal stability was presented previously. This revealed a potential failure mechanism for the titanium-gold system as a resistance increase, followed by a burnout in a localized area. This failure mode appears similar to that seen in about 500 hours with the chromium-gold system and about 7000 hours with the molybdenum-gold system.

The titanium-gold data is given in Table 24. There appears to be a strong dependence on initial resistivity, and therefore on the titanium thickness. Films with approximately 6.5 micro-ohm-cm resistivity are characterized by about 1000Å of titanium and good high current performance. Lifetimes of 19,000 hours at $1x10^5$ A/cm^2 and 7,500 hours at $2x10^6$ A/cm^2 are indicated. At higher current densities, the lifetimes are greatly reduced. The distribution of the failure times are shown in figure 20. From these results, the titanium-gold system on SiO_2 continues to show promise as a low temperature system, if the titanium thickness is less than 1000Å. However, these thin titanium layers are inadequate to prevent alloying of the gold with exposed silicon, if elevated temperatures (>370°C) are involved. This limitation of the titanium-gold system was discussed earlier.

TABLE 24.- TITANIUM-GOLD HIGH CURRENT TEST DATA

Sample	Resis-tivity (micro-ohm-cm)	$J \times 10^6$	T(°C)	Fraction Failed	Total Test (Hrs.)	50% MTF
1-5	6.5	0.98	179	4/10	91,300	20,000
1-4-2	8.5	1.56	153	4/7	20,240	5,300
2-4-2	8.5	1.58	176	9/9	7,650	760
1-10	6.5	1.88	193	8/10	68,680	7,800
1-4-1	8.5	2.9	186	10/10	19	1.7
2-4-1	8.5	2.91	243	10/10	21-1/2	2.0

Titanium-Platinum-Gold

The initial thermal and high current density tests of the titanium-platinum-gold films have indicated a need to study the thickness effects in this system more completely. A sample of etched titanium-platinum (3500Å) was coated with evaporated gold to a total thickness of 8000Å. The titanium thickness was estimated to be 2000Å. Initially, the resistivity was 4.4 micro-ohm-cm. However, after gold backing and mounting, and encapsulation, the resistance had risen such that the resistivity was 4.8 micro-ohm-cm. In order to gather information, titanium-platinum-gold samples were placed on test at current densities even higher than normal. Also samples were sputter-etched from a film of 3500Å titanium-platinum, with a gold layer of 2,220Å. The initial resistivity was 6 micro-ohm-cm, but after processing and encapsulation, the resistivity had risen to 8.9 micro-ohm-cm. The ambient temperature for these high current tests was 125°C. The results are shown in Table 25. The $1.8x10^6$ A/cm^2 and higher current density samples showed primarily a resistance rise prior to failure.

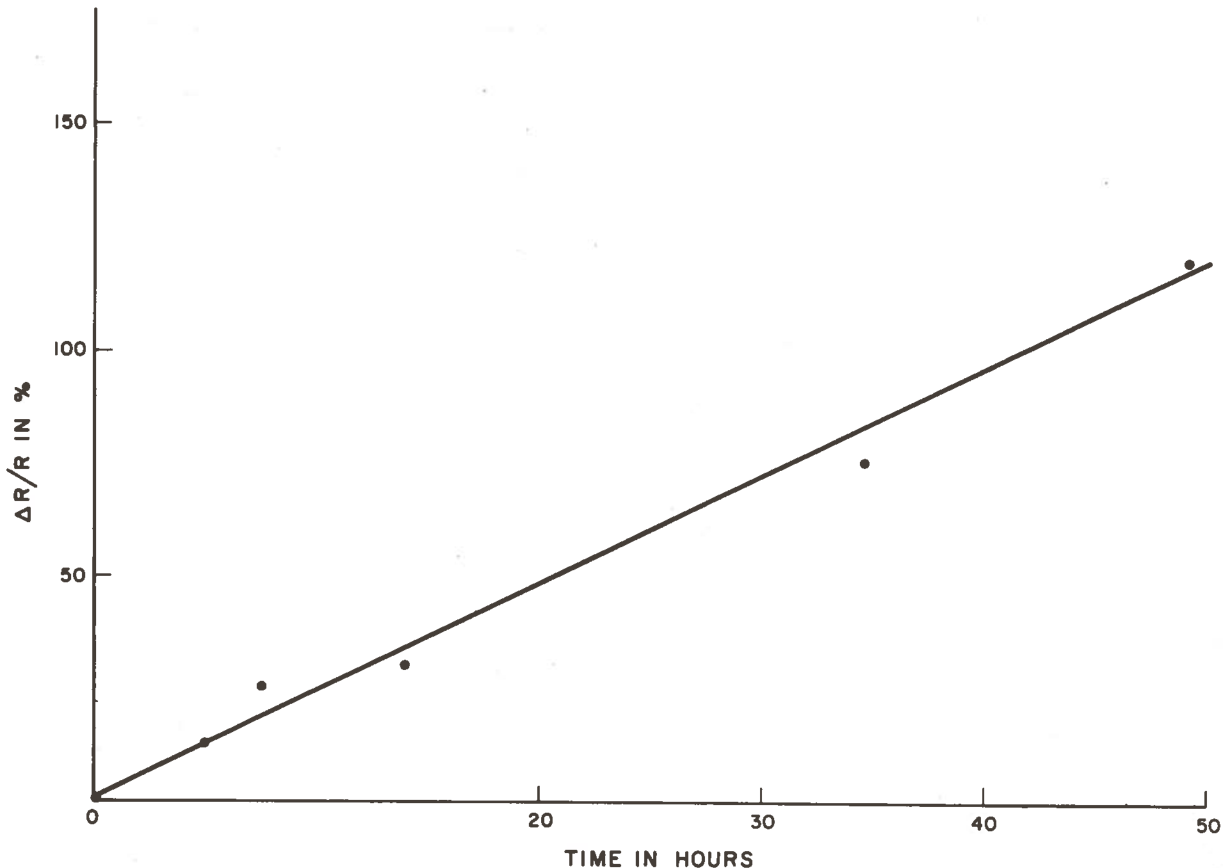


Figure 21.- Ti-Pt-Au Total Thickness (9000Å) Normalized Resistance as a Function of Time on Test at $3.5 \times 10^6 A/cm^2$ and 225°C

film consisted of about 3500Å of titanium-platinum and 4500Å of gold. The adjacent 1-mil conductor (no current) showed no significant change in resistance. In a $6.3 \times 10^6 A/cm^2$ test, where the film temperature was 500°C, the adjacent conductor (no current) showed a 4.5 percent increase in resistance, although the test was less than 1/2 hour in duration. Examination of the ohmic failure at $3.5 \times 10^6 A/cm^2$ showed a very roughened surface. The edge around the gold pattern is the titanium-platinum layer, which was left slightly wider than the evaporated gold. This sample showed an ohmic increase as would be predicted by the 450°C thermal tests.

Although these tests were not as complete as those of the other metallizations, they indicate a resistance mode of failure may be induced in Ti-Pt-Au at elevated temperatures and/or high current densities.

Molybdenum-Gold

Considerable data on the molybdenum-gold system is shown in Table 26. This metallization appears to be the most promising to date. The results show that good reliability is obtained at 175°C ambient temperature and current levels up to 2 x 10^6 A/cm^2. At higher current levels, the lifetime is higher than for the other metallizations. The glassing does not appear to significantly increase the lifetime on the high current tests. The failure mechanism appears in the long life samples as a resistance increase. Opens have occurred within the first 200 or so hours of operation of samples at low temperatures (185°C), and low current densities. At higher temperatures (>185°C), the characteristic failure mode is characterized by a doubling of resistance in about 7,000 hours. Analysis of the five long life groups gives a sample of 50, with 2 opens occurring at 28 and 200 hours. The rest of the failures have been ohmic (resistance doubling). The distribution of these failures is shown in figure 22. A typical resistance failure is shown in figure 23.

Each sample consisted of a chip mounted in a TO-5 can with both a 1/2 and a 1 mil wide conducting strip wired to the pins. The first tests were on the 1/2 mil lines. Following the failure of the 1/2 mil conductor, the resistance of the 1 mil conductor was verified. Following the verification of the 1 mil lines, the samples are often returned to the test sockets, using the 1 mil conductor. The applied voltage and external load resistors were the same as used for the 1/2 mil test, so the current through each test conductor was about the same as before, but the current density is about half the first test value. The load resistors were generally at least ten times the resistance of the test conductor, to minimize the current density variation due to sample resistance changes. Each test was started after a 24-hour preheat before applying current to the samples. The current was increased slowly over a several minute period to the desired value.

One sample of evaporated molybdenum-gold in the tests at 150°C oven temperature showed an early increase in resistance. This molybdenum-gold conductor, 1 mil wide x 54 mil long initially showed a higher than normal resistance (7.35 ohms vs 5.91 ohms). This sample showed an increasing resistance during the early portion of the test, and doubled its resistance in about 28 hours. The other eight samples of this group did not show this change. However, the average temperature for the group was 247°C, while this particular device operated initially at 260°C, due to its higher resistance. As the resistance increases, the current falls slightly, and the temperature rises. The resistance and the calculated temperatures of this sample during the first 60 hours of

test are shown in figure 24. When this device was opened for inspection, it was discovered that the die was bonded poorly to the header, which would reduce the thermal transfer to the header, raising the sample temperature considerably above the estimated values based on a good thermal transfer. The 1/2 mil strip showed a normal gold burnout failure occurring under the silicate glass (figure 25). The 1 mil strip showed a large area of missing or spotty gold under the cracked glass. Some of the

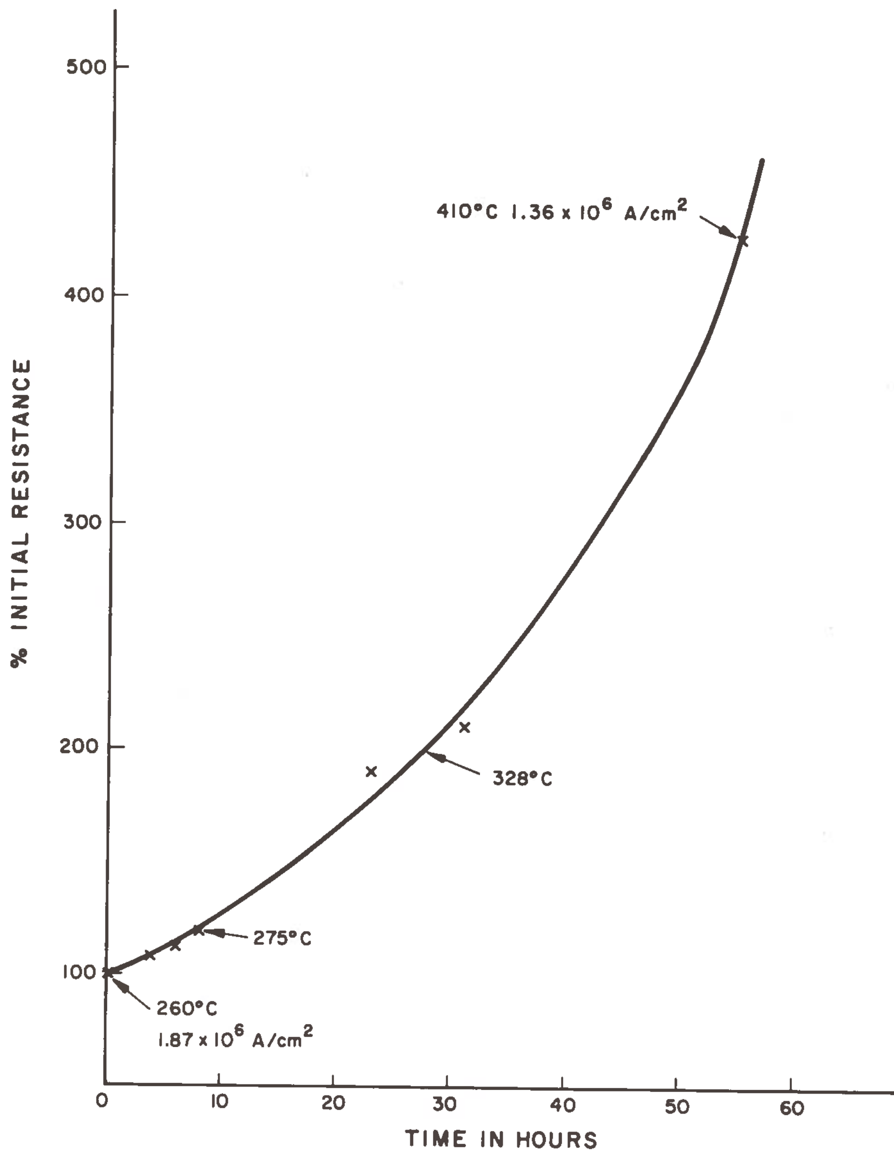


Figure 24.- DC Resistance of Moly-Gold 1-mil Strip (#2-81) as a Function of Time at 1.96×10^6 A/cm^2 - Estimated Film Temperature 247°C (average)

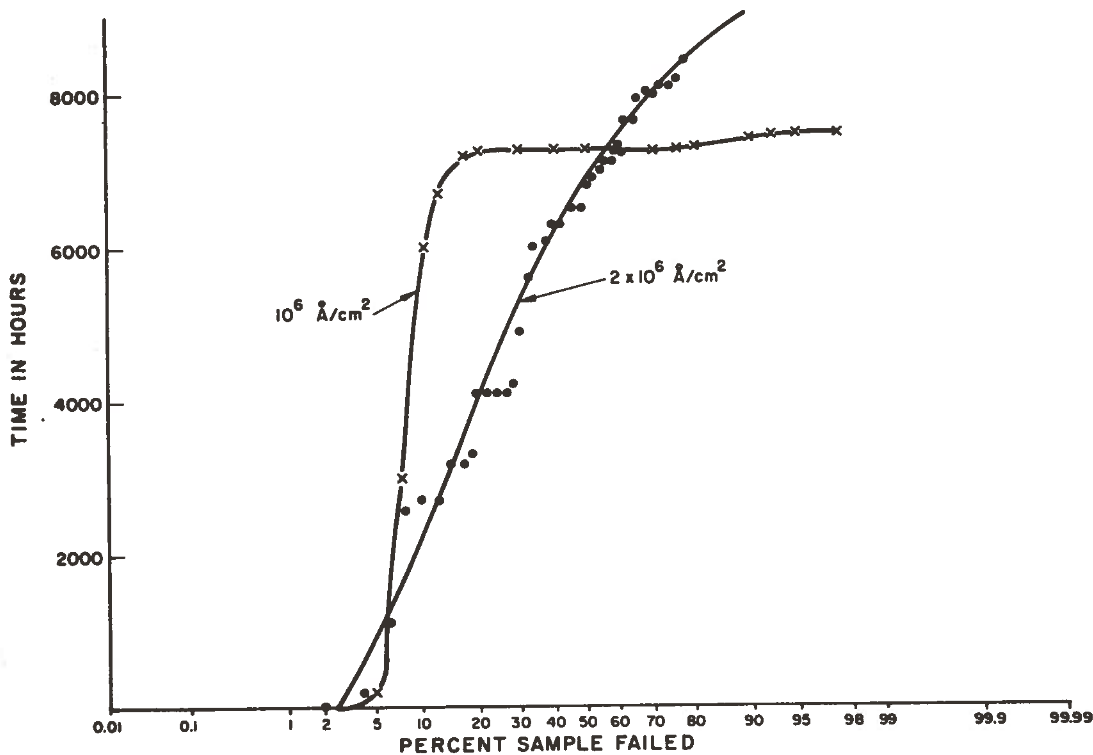


Figure 27.- Distribution Plot of Molybdenum-Gold Failures at 175°C and 1 or 2 x 10^6 Å/cm^2

(1040X)

Figure 28.- Sample 1-15. Molybdenum-Gold Failure ~7000 hours 175°C 1 x 10^6 A/cm^2

TABLE 27.- CURRENT DENSITY TEST RESULTS

	Current Density J 10^6 A/cm^2	Resis-tivity (micro-ohm-cm)	Average Temperature	50% MTF (hours)
Al	1.0	4.7	167°C	780
	2.0	4.4	185°C	19
Cr-Au	1.0	7.8	195°C	13,500
	2.0	7.6	219°C	1,500
Ti-Pt-Au	0.98	6.5	179°C	20,000
	1.88	6.5	193°C	7,800
Mo-Au	1.0	4.2	177°C	6,700
	2.0	4.4	194°C	5,250
Ti-Pt-Au	0.9	8.9	180°C	4,600
	1.8	8.9	190°C	2,500

higher resistivity samples have a reduced lifetime. At 2 x 10^6 3 x 10^6 A/cm^2 and 210°C the life was only 1.9 hours.

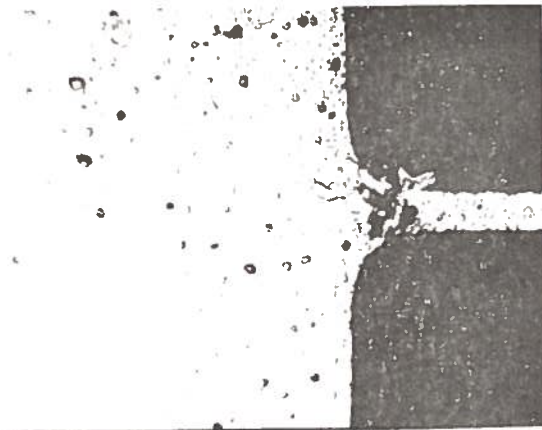
The Ti-Pt-Au samples were from a lot which had only 2,000 Å gold deposited over 1,500 Å Pt. From the thermal tests discussed in a previous section, this combination of thickness in Au-Pt is expected to exhibit a thermally induced resistance increase. Even though the current density samples were not of optimized thickness, the lifetime was longer than 2,500 hours at 1.8 x 10^6 A/cm^2.

The extended lifetime of the Au based systems is further exemplified by the data on the MoAu samples. Even at 2 x 10^6 A/cm^2, the lifetime of the MoAu samples exceeded 6,000 hours.

The current density studies reported here on the Au based systems were not designed to be as intensive as those reported on aluminum (ref. 3). Consequently, the results do not necessarily indicate that Au migration is a predominant failure mode in the metal Au systems tested. The intended result of qualitative comparison in lifetime was accomplished, and shows that the Au based systems are capable of lifetimes of 10 to 100 times longer than aluminum at a very high current density.

with most glass combinations. The sputtered film showed a high resistivity and earlier tests showed cases of severe "nuggeting".

Therefore, the tantalum filament evaporated aluminum was chosen as a reference metallization. This material showed deterioration when unprotected, but was greatly improved by the use of any of the glass combinations. (See figures 29 and 30).



(1000X)

Figure 29.- Aluminum (Tantalum Filament Evaporation) after 18 Hours at 450°C in Air

(1000X)

Figure 30.- Aluminum (Tantalum Filament Evaporation) and SiO_2 after 18 Hours at 450°C in Air

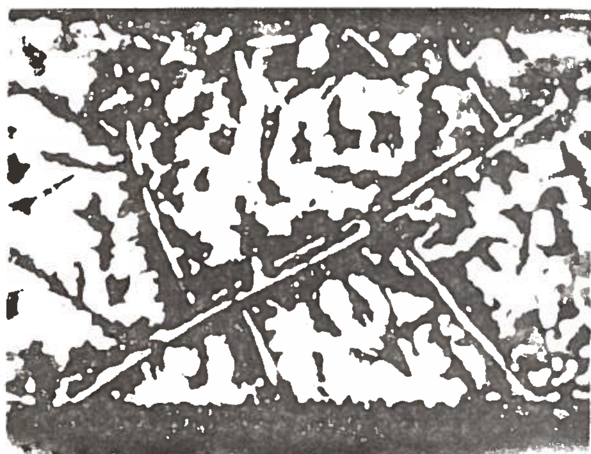
The higher temperature SiO_2 operation caused some mild deterioration of the metallization, which was reduced when an initial thin layer of sputtered quartz or low temperature glass was applied prior to the SiO_2 operation. All the glasses adhered to the aluminum metallizations and no cracking, or loss of glass was noted.

Molybdenum-gold and molybdenum-gold-molybdenum films were prepared using 2000 Å of molybdenum, 4000 Å of gold, and, in some cases, 200 Å of molybdenum as a top layer. The compatibility of the metallization with various glassing processes was checked by depositing a layer of glass over the patterned metallization before the thermal tests. The evaporated molybdenum-gold and molybdenum-gold-molybdenum films, sputtered molybdenum-gold, the referenced metal aluminum and a titanium-gold film were rated for compatibility with the various glasses in Table 28. There were cases of cracked glass and poor adherence, as indicated in the table.

The unprotected films varied in performance. The aluminum showed mild deterioration starting in 1/2 hour at 450°C. The deterioration of the molybdenum-gold films was varied.

Molybdenum films showed good stability after 18 hours baking at 450°C in air. These films were not protected by a glass overcoat and were deposited by sputtering onto a thermally oxidized substrate. Dark edges are observed along the molybdenum-gold films due to oxidation of the molybdenum out from beneath the top gold layer, a frequently observed mode of deterioration unless a glass passivation overcoat is used. If the top gold is thin and a heavy interface is used, the deterioration becomes quite severe even though a glass passivation is used. (See figure 31.)

Cracking of the glass layer was seen with the gold top layers and sputtered quartz, sputtered quartz plus low temperature glass, sputtered quartz plus SiO_2 and the low temperature glass. The only glass adhering to the gold (either evaporated or sputtered) was the SiO_2 (even in this case adherence to larger areas of gold was marginal). The films with the SiO_2 showed little or no deterioration in 18 hours at 450°C. The deterioration noted in the cracked samples originated around the exposed metal area further suggesting that the diffusion of oxygen through the gold or glass is a probable mechanism.



(1520X)

Figure 31.- Sputtered molybdenum-Gold Film and Low Temperature Glass After 18 Hours at 450°C in Air (Thin Gold Layer)

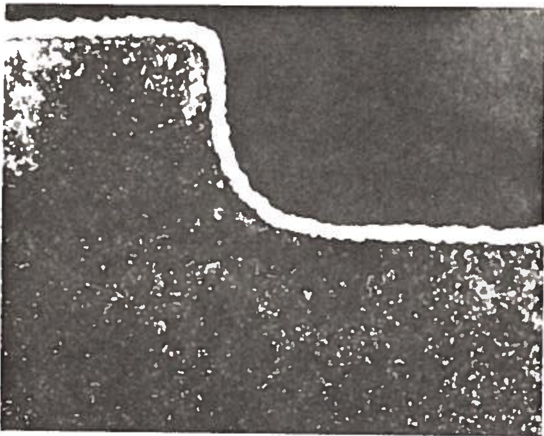
The above action is not surprising. Gold when deposited upon glass substrates does not adhere well, and glass deposited upon gold should behave similarly. The adhesion in this case will be enhanced by the surface roughness or texture of the gold film. The SiO_2 adhesion, however, is improved because this passivation is deposited by vapor or gas plating. In this method, corrosive constituents are reacted at an elevated temperature at the surface of the substrate. No doubt a certain amount of reaction between the gold and one or more materials in the vapors does occur before the actual glass layers start to form, resulting in an improved metal-to-glass bond.

The molybdenum-gold-molybdenum film showed interesting properties. If the film is heated at 450°C with the top molybdenum layer exposed to air, the sample deteriorates as expected. This deterioration carries through to the intermediate gold layer. If the top molybdenum film is removed before the baking, the results

Note: The term SiO_2 refers to gas vapor deposited material.

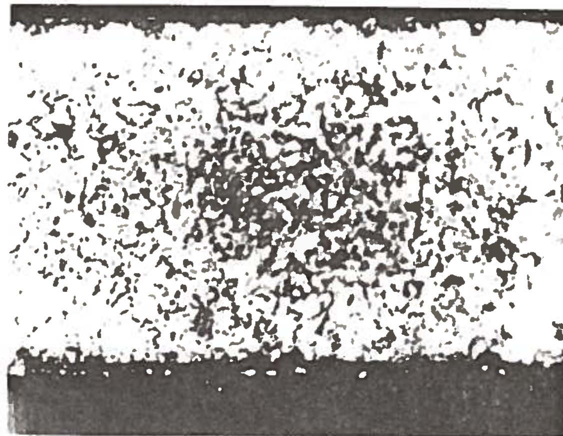
film deteriorated rapidly and completely in the air bake at 450°C. The edges of the film showed little or no deterioration. The edge was apparently an intact gold film which was undercut during the titanium etch (see figure 33).

Both the sputtered quartz and the low temperature glass showed cracking on this metallization, with severe deterioration of the exposed metal, and mild deterioration of the protected areas. The SiO_2 film did not crack and the protected metal showed little or no deterioration in three hours and mild deterioration in 18 hours (see figure 34).



(1520X)

Figure 33.- Titanium-Gold Film after 18 Hours at 450°C in Air



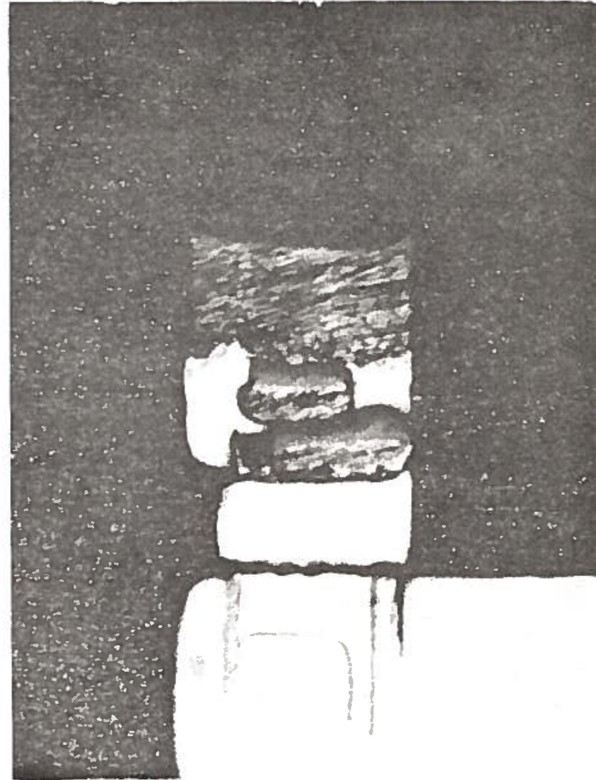
(1520X)

Figure 34.- Titanium-Gold Film and SiO_2 after 18 Hours at 450°C in Air

The titanium-gold film had an initial resistivity of 3.4 micro-ohm-cm with no significant increase on baking. This is surprising, in view of the obvious visible deterioration of the film in many cases. However, the average measured resistance of the 1/2 mil x 54 mil line before glassing was 18.8 micro-ohm-cm and, after glassing and baking, 1 1/2 hours at 450°C, the value was 19.2 micro-ohm-cm.

1500X

Figure 36.- Normal Cross Section of Multilayer Molybdenum-Gold-Glass-Molybdenum-Gold-Glass



1200X

Figure 37.- 5° Angle Cross Section of Multilayer Molybdenum-Gold-Glass Molybdenum-Gold

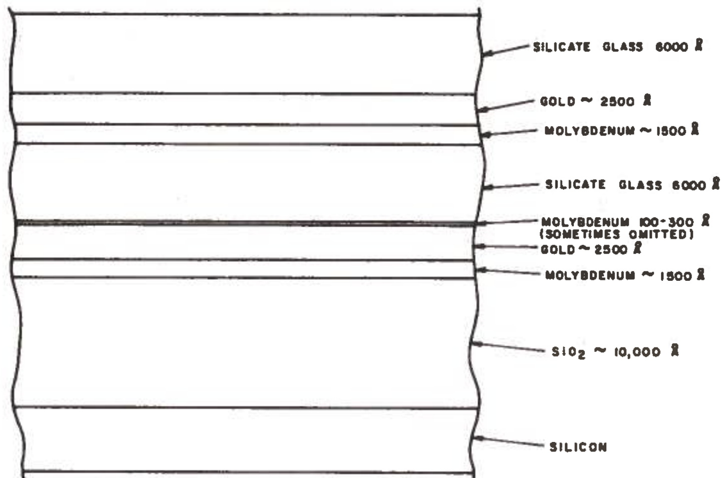
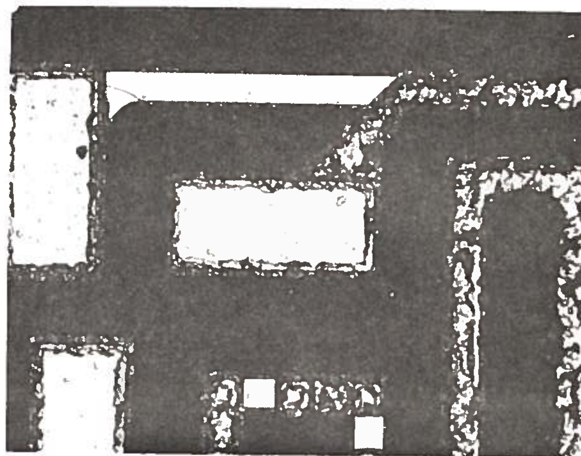


Figure 38.- Schematic Representation of of Molybdenum-Gold Multilayer Test Vehicle

(375X)

Figure 40.- Molybdenum-Gold-SiO_2-Glass-Molybdenum-Gold Multilayers after 1 Hour at 450°C in Air



(375X)

Figure 41.- Molybdenum-Gold Multilayer SiO_2 Structure After 18 Hours at 450°C in Air

generally gave more problems than those that were evaporated. Even in the most difficult cases, the 3 micron lines were always retained. Many of the 1 micron lines were etched successfully, but were lost in subsequent cleaning and removal of the resist. The problem is minimized by substitution of a gentle TCE rinse for the normal TCE spray cleaning.

The normal photoresist retains the exposed portions, and the unexposed area is removed in the development. In some processes, it is convenient to use the Shipley AZ 1350 Resist, in which the exposed portion is removed by the development step. Using Shipley AZ 1350 Resist the fine-line pattern has been consistently reproduced.

With the increased complexity and fine-line geometry of the test patterns being used, the difficulties of consistently patterning a complex metallization became more apparent. Specifically, the use of the present multilayer test pattern has disclosed photoresist problems. The difficulty, generally, is seen with the use of a vigorous etching solution, usually heated, and appears in the form of lifting photoresist toward the end of the etching process. While no definite conclusions have been possible, several tendencies have been noted. First, the final bake time and temperature are critical for these complex patterns. Inadequate postbake, after development, commonly causes poor adherence. There has also been a tendency for more adherence problems with the molybdenum top coated metallizations, especially where the molybdenum is thicker than a few hundred angstroms. This problem is probably due to the undercutting of the resist during the etching of the thicker bottom molybdenum layer. However, the use of controlled etching conditions has, to a large degree, eliminated any serious problems. A common cause of difficulty is the use of molybdenum etch at too low a temperature, resulting in an excessive etching time. The etching step for the bottom 2000 Å of molybdenum should not be much greater than 15 seconds, and never longer than 30 seconds. After etching, a rapid and complete rinsing in deionized water is necessary. With an adequate postbake (30 minutes at 180°C for the resist used in this experiment), there has been little adherence problems. However, it has occasionally proved difficult to completely remove the resist from the water. The use of an acetone rinse, 15 seconds in hot J-100 (photoresist remover), followed by a second acetone rinse, and another 15 seconds in hot J-100 has proven satisfactory in even the most difficult cases. The wafer is then cleaned by an acetone rinse, and TCE sprayed.

Before any further processing, the wafer is rinsed at least 30 minutes in deionized water. Before metallization steps, a 5 second dip in very dilute (40-1) buffered HF etch, followed by a deionized water rinse is performed. This produced wafers which

width of the patterned line. The etching of these thick films may be avoided in the gold systems by etching only a thin layer, then plating additional gold on the patterned wafer.

Figure 44.- 5° Angle Cross Section of Multilayer Molybdenum-Gold-Molybdenum-Glass Molybdenum-Gold-Glass

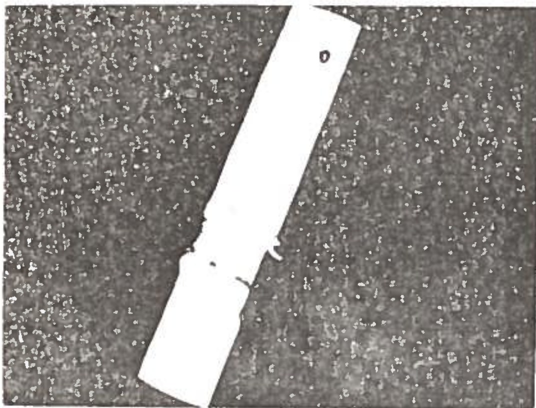


Figure 45.- Photomicrograph of Scratched Molybdenum-Gold Metallization - Line 2 mils Wide

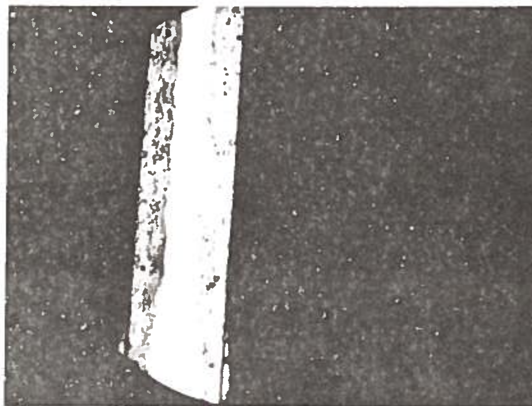


Figure 46.- Photomicrograph of Poorly Etched 3-micron Aluminum Film - Line 2 mils Wide

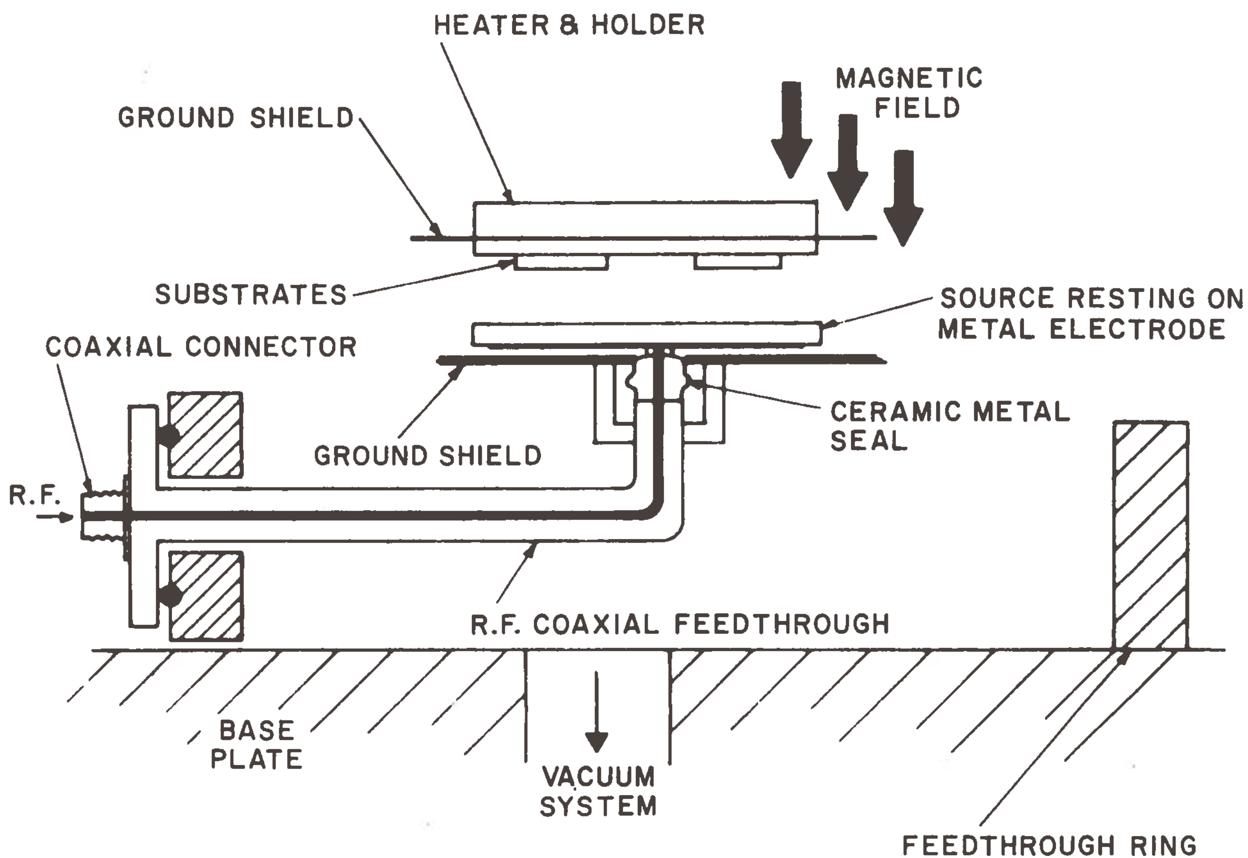


Figure 47.- Diagram of Diode RF Sputtering System

temperature and the reactive gases in the vacuum system. The removal rate increases with wafer temperature and can be decreased by a factor of two simply by water cooling the source target.

A second masking process has been used in beam lead work (ref. 20). In this use only the Pt is sputter etched and the thicker gold plated beams serve as the etch mask. After deposition of the Ti-Pt, the gold is plated to 2 microns or greater on the beams. The thick gold then serves as a mask and only approximately 3000 Å of the gold is removed in sputter etching the 2000 Å Pt film.

Figure 48 contains photomicrographs of a portion of the first layer metallization in a multilayer test pattern. This pattern was photo masked with 9000 Å of KMER (poise 0.15) and the Au and Pt were RF sputter etched. The Au thickness is approximately 8000 Å and the Pt is 1500 Å. Figure 48 (b) is a blown-up view of a portion of the pattern in figure 48 (a). The

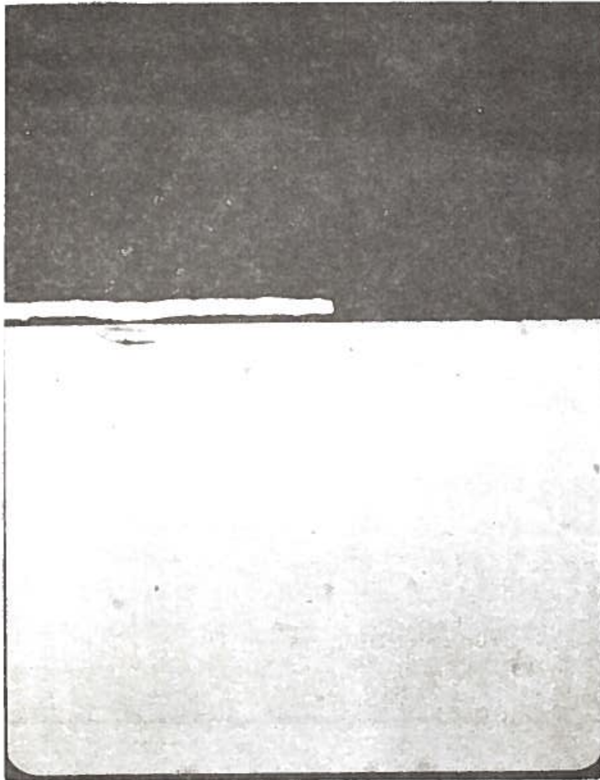


Figure 49.- Cross Section of Sputter-Etched Ti-Pt-Au

The Cr and Mo metals were being bombarded for a full five minutes after the gold cleared while waiting for the thicker Au and Pt metals to complete etching. There was no indication of undercutting on any of the wafers and a continuous film of Cr, Mo or Ti remained on all wafers. Therefore the process is easily controlled and is only limited by the resolution of the masking material and the relative sputtering rates of the materials.

Sputter etching of the Pt for beam lead work which is the Ti-Pt-Au system, has also been demonstrated. The Pt is sputter etched using either photoresist as a mask or the gold plating. In using the gold mask, the Pt is not etched until after the gold plating of the beams is completed. The thick gold (2 microns to 0.5 mil) then serves as a mask for sputter etching the Pt. The sputtering rate for the gold is only slightly faster than the Pt and approximately 3000 Å of plated gold is removed while sputter etching the Pt. The technique actually reduces the number of resist steps in the beam lead fabrication process by at least one from the required steps had chemical etching been used.

These results indicate the feasibility of the sputter etch technique in delineating semiconductor contacts. The practicality and adaptability of this technique for a production process obviously depends on the metal system to be etched. Clearly, its use in etching aluminum is limited. Even though excellent definition is obtained in aluminum, the extremely slow etch rate makes this technique impractical. However, for a system such as Ti-Pt-Au the sputter etching technique is practical and amendable to a production process.

An early application of beam leads was 2 DCTL gates with 3 and 4 inputs of high frequency transistors, and nine beam-leaded boron-diffused silicon resistors. Several circuits wired as 3-stage ring oscillators with a fan-in of 3-4, and fan out of 1, yielded measured propagation delay of 4.2 ns.

A specific application of beam leads to monolithic integrated circuits was investigated by Waggerer (ref. 29). As a consequence of etching away the unwanted silicon from under the beam leads, isolated pads of silicon may be attained, interconnected by beam leads. The only capacitive coupling in these small metal-over-oxide overlays is typically 0.05 pf.

The processing was developed to survive 350°C oxidizing ambients (air or steam) continuously for 1000 hours without degradation. The metallurgical system is Pt_5Si_2-Ti-Pt-Au. Platinum silicide is used as the ohmic contact material for it is the most stable of the silicon compounds, has extreme corrosion resistance and is a solid phase at 980°C (ref. 30). It has an optical reflectivity different from either silicon or platinum and forms ohmic contact to heavily doped silicon.

In this particular reference the platinum is sputtered and heated to 700°C in an inert atmosphere. The platinum reacts with silicon to form Pt_5Si_2 which is a solid phase and will not ball up or creep beyond the edges of the contact holes as a eutectic would do. Platinum over the oxide is removed, leaving silicide inside the contact holes. Then titanium is deposited which has a high oxygen activity, refractory in nature, an ability to absorb almost half its weight in reaction products interstitially and the natural oxide that it does form is completely self-passivating at temperatures of about 400°C.

Table 29 lists some common metals and free energies of formation of their oxides in order of activity (ref. 31). This may be used as a guide for surface-bonding strengths. Titanium is the first active metal after silicon and in addition to having great bonding strength, titanium may be used to penetrate a thin SiO_2 layer (gettering). Gold is used as beam lead material because of its corrosion resistance, ease of bonding, low yield point, high elongation and suitability with high resolution electroforming. However, gold is a very reactive metal and reacts with titanium chemically at relatively low temperatures for form compounds which are undesirable. So platinum is used in a sandwich structure for it has a low diffusion coefficient with gold (D is less than 10^{-10} cm^2/sec. at 900°C) (ref. 32).

Metal films are normally deposited by evaporation but in this case, since there is a need for extreme adherence of titanium to silicon dioxide, the sputtering technique is used. Since sputtered metals have many times the energy of thermally

8. Introduces a minimum amount of damage or surface instability while being deposited
9. Compatible with multilevel processing
10. Beams must be ductile and easily bonded

Since the properties of a metal demanded by each function vary markedly, it is difficult to find a simple metallurgical system that will satisfy all the requirements. With the exception of the all-aluminum beam lead metallurgy (refs. 33 and 34) all other metallurgical systems reported are composed of three or more metals; the contact metal, the bond metal, the diffusion barrier metal, and the beam metal. This section will discuss beam lead materials, processing and reliability of beam lead technology now in use or to be used in the immediate future.

The first level metallization must have high conductivity, low contact resistance, must not degrade at high temperatures or current densities and be amenable to production techniques. Of the more commonly used metals: aluminum, chromium, titanium, molybdenum, platinum, palladium, cobalt and nickel; each appear to have advantages and disadvantages. In some cases these characteristics have been discussed in previous sections; but bear repeating.

Aluminum has high conductivity and low contact resistance but will dissolve the silicon substrate at elevated temperatures and/or high current densities. Chromium is an excellent contact metal as well as a good bond metal but forms rectifying contacts on P-type silicon over 0.02 ohm-cm. Nickel also makes rectifying contact on high-resistivity P-type silicon and suffers from degrading intermetallic compounds at high temperatures. Molybdenum is a good contact material and has good temperature stability but does form rectifying contacts on high-resistivity N-and P-type silicon (above 0.01 ohm-cm). Platinum comes the closest to the ideal contact material. It does, however, have one property that limits its use. Due to its very high melting point, it must be evaporated by electron beam or sputtered so that xrays are present during the deposition which can cause damage to MOS devices. Recently, palladium has been suggested (ref. 35) as a replacement for platinum on MOS devices since it can be evaporated from a tungsten filament, thus eliminating any possibility of xray damage. Since palladium has similar characteristics to platinum and can usually be etched*, the consensus of opinion is that palladium will replace platinum in beam lead technology. In the case of either palladium or platinum, a silicide is formed and markedly reduces contact resistance. See Table 30 (same as Table 21 in a previous section).

Metal silicide-Si contacts are prepared as follows. Silicide films of about 1000 Å in thickness are deposited onto oxidized

*Palladium can be etched in concentrated sulphuric acid at 60°C

silicon wafers with contact holes by vacuum evaporation. The source silicides are prepared by melting the stoichiometric amounts of their constituent materials with the use of an hf generator in an argon atmosphere. In order to prevent oxidation of the silicide layer, the Pt layer of about 2000 Å in thickness is successively deposited onto the silicide layer. Evaporated platinum and silicide layers are chemically etched to form expanded contacts using photo resist techniques. These specimens are then heat-treated for 10 minutes at a proper temperature between 300°C and 700°C in an argon atmosphere. After heat treatment, a gold outer layer is deposited in order to make easy bonding of the lead wire for the electrical measurements. The I-V characteristics of the silicide-silicon contacts have been observed using a diode curve tracer and the measurements of the contact resistances carried out by the ordinary dc four-probe method. The shear adherence of the silicide layer to the SiO_2 surface is determined by the scribing technique (ref. 36).

The results of x-ray analysis show that as-deposited, silicides are amorphous but when silicide-silicon contacts are heat treated at temperatures above 400°C for 10 minutes the diffraction pattern corresponding to the silicides appears in addition to those of platinum and silicon. In the case of CoSi-Si contacts, the diffraction pattern corresponding to CoSi is observed for heat treatment at 400°C and those corresponding to CoSi and $CoSi_2$ at 500°C. In the case of PtSi-Si contacts, only diffraction patterns corresponding to PtSi is observed for heat treatment above 400°C. From the features of the I-V characteristics it has been found that the silicides such as CoSi, $CoSi_2$ and PtSi provide good ohmic contacts to n-type silicon having the resistivities less than 0.005 ohm-cm and to p-type silicon less than 0.01 ohm-cm.

The results of the measurements of the specific contact resistance, Rc for CoSi-Si and PtSi-Si contacts are given in Table 30 along with those of Al-Si (ref. 37). All the measured values are the average of at least four measurements. The values of Rc are reproducible to ±20 percent. It should be noted that all of the silicides studied yield low resistance ohmic contacts to heavily doped silicon and Rc is strongly dependent on the resistivity of silicon, regardless of the particular silicide contact. The effects of heat treatment on Rc are remarkable when the resistivity of silicon is relatively high.

The shear adherence of silicides to SiO_2 is presented in Table 31 in comparison with those of some familiar metals. Shearing forces are calculated from the indentation hardnfess of SiO_2 and the critical loads at which the silicide films are stripped from SiO_2 leaving a clear channel (ref. 38). The results are rather qualitative because measurements of the

considered as bond metals because of their adhesive qualities. Aluminum, in fact, has been used by itself to form a complete beam lead system (ref. 38). This system, however, is limited to low current (10^5 amps/cm^2) and low temperatures (400°C). Since all of these beam metals are very active, they are subject to corrosive undercutting during defining; therefore, they must be deposited in very thin layers.

As gold is most often used as the beam lead material, a diffusion barrier layer metal is used to prevent gold diffusion. Molybdenum is a good diffusion barrier and has the added advantage of being inexpensive and readily defined by chemical etching in the presence of the gold beam, eliminating several costly fabricating steps. Tests have shown molybdenum-gold metallization to be severely corroded in 85°C, 85 percent relative humidity ambients in 48 hours, where platinum-gold metallizations have exceeded 1000 hours in the same atmosphere (ref. 39). Since the beam is the contact medium between chip and substrate, special consideration must be given to its compatibility with the substrate metallurgy as well as the chip metallurgy. In general, a beam metal must have the following characteristics:

1. Good mechanical strength
2. Easily deposited in thick layers (>50,000 Å)
3. Easily defined by controlled deposition or etching
4. High corrosion resistance
5. Low yield point
6. Coefficient of expansion near to that of silicon or high elongation to overcome mismatch
7. High conductivity
8. Easily bonded.

Gold, aluminum, nickel (ref. 40) and copper (ref. 38) are most often suggested as potential beam metals that could be used in conjunction with a variety of bond and barrier metals. Unfortunately, many of these metal systems deteriorate rapidly in corrosive environments which are accelerated if the metals are under electrical bias. Table 33 shows the effect of electrical bias on some of these metal systems while submerged in a boiling 1 percent solution of ammonium hydroxide in deionized water. The vehicles used for testing the metals listed were silicon dice upon which has been patterned parallel "dogbone" conductors to which suitable bonded connections were made. A potential of 10 volts was applied to pairs of the strips while chips were submerged in the electrolyte.

Although the all-aluminum beam lead system has too many restrictions for general use, it does offer a simple, inexpensive metallurgy for low current applications. A typical all-aluminum system (ref. 34) consists of a conventional integrated circuit on which a layer of silane glass is deposited and windows are

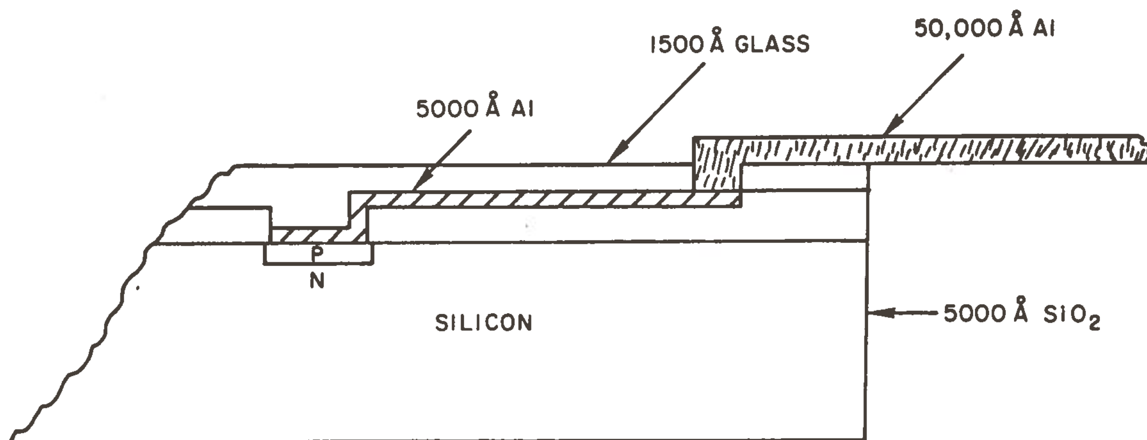


Figure 50.- Aluminum Beam Lead System with Separately Deposited Beams

2000 Å sputtered and 6000 A pyrolythic quartz, the pinhole density dropped to a minimum. Ninety seven percent of the circuits were free of pinholes. For the connection to the beam leads, feed-through windows are cut in the deposited oxide and layers of titanium (1000 Å), platinum (3000 Å) and gold (2000Å) are sequentially sputtered onto the entire wafer. The beams are then electroplated to the proper height. The sputtered gold and platinum is removed from the unwanted areas by sputter etching and the titanium is chemically etched. See figures 51 and 52. Despite the fact that pure metal layers were deposited, all devices with aluminum interconnections and Ti-Pt-Au beams showed high contact resistance (up to 1000 ohms). The electrical behavior of these contacts strongly indicated the existence of an aluminum oxide between the aluminum interconnections and the titanium. Therefore, it was necessary to introduce a sputter etching step prior to the deposition of the titanium. With this method and the sequential deposition of pure Ti-Pt-Au, excellent contacts were obtained.

A copper system (ref. 38) was also developed with the purpose to increase the radiation resistance of integrated beam lead devices. Again silicon nitride is used as passivation on top of the thermally grown oxide. Platinum silicide provides the semiconductor-metal contact (ref. 41). Titanium (1000 Å) platinum (3000 Å) and copper (2000 Å) is then sputtered sequentially and the interconnections and beams electroformed to the desirable height. Sputter etching is again used to remove the sputtered copper and platinum from unwanted areas. The titanium bottom layer is etched away chemically. Along with the work referenced above, two multilayer interconnection systems for integrated circuits have been developed. In both systems, platinum silicide provides the necessary semiconductor-metal contacts. The first layer interconnections consist of titanium,

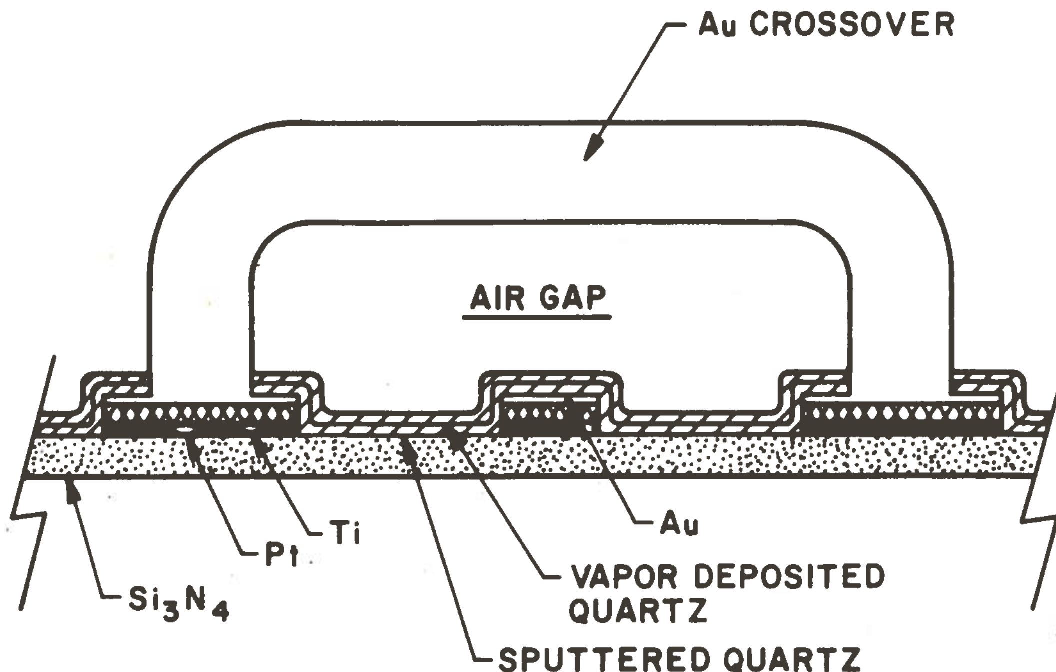


Figure 52.- Cross Section of Dielectric and Air Gap Isolated Crossover

Platinum and palladium have not been evaluated as beam metals but they have potential in this application for high-reliability devices which are subjected to very severe corrosive environments. The cost would be higher and the bonding would be more difficult but the thermal expansion mismatch would be less and the corrosion resistance would be far superior to any other metal system.

For most applications gold beams are almost the unanimous choice due to ease of bonding and fabrication. In addition, gold has a relatively high corrosion resistance. While gold on titanium and platinum is the technique most widely used, there are recent reports on gold beams on aluminum (ref. 34) and molybdenum-aluminum (ref. 44).

This survey was intended to cover only metallization; but one might say that a metallization system is only as good as the dielectric under or on top of it. Currently three dielectrics are used; silicon dioxide, silicon nitride and aluminum oxide.

contaminate the oxide layer composite it covers and will act as a barrier to impurities if it is free of pinholes. The quality of the oxide is extremely critical in MOS structures as the conventional oxide remains and the silicon nitride is deposited over this oxide. In the contact windows the silicon dioxide is regrown prior to silicon nitride deposition producing a more uniform stress-free film and minimizing pitting of the highly phosphorus doped silicon during the nitride etch.

TABLE 34.- SUMMARY OF PHYSICAL PROPERTIES (ref. 46)

	SiO_2 Amorph.	Si_3N_4 Cryst.	Si_3N_4 Amorph.	$Si\text{-}O_xN_y$ Amorph.
Melting Point (°C)	~1600	~1900	--	--
Density g cm^{-3}	2.2	3.4	3.1	--
Index of Refraction	1.46	2.1	2.05	1.60-1.88
Dielectric Constant	3.8-3.9	9.4	7.5	4.77-6.12
Dielectric Strength V cm^{-1}	~5 x 10^6	--	~1 x 10^7	~5 x 10^6
Infrared Absorption Band μm	9.3	10.6	11.5-12.0	9.3-12.0
Energy Gap (e.v.)	8	3.9-4.0	~5.0	--
Thermal Expansion Coeff./°C	5.6x10^{-7}	3.0-3.5 x10^{-6}	--	--
Thermal Conductivity cal cm^{-1} sec^{-1} $°C^{-1}$	0.0032	0.067	--	--
dc Resistivity ohm-cm				
at 25°C	10^{14}-10^{16}	10^{15}	~10^{14}	
at 250°C	--	--	--	
at 300°C	--	--	--	
at 350°C	--	~10^{13}	~2 x 10^{13}	
Etch Rate in Å/min in 10:1 NH_4:HF	1000	<0.1	5-10	33-400

(Thermal Expansion Coefficient of Silicon: 3.2 x 10^{-6}/°C.)

which etches silicon nitride much faster than silicon dioxide. Typical etch rates with this solution would be 150 Å/min for silicon nitride and 20 Å/min for silicon dioxide. Silicon nitride etched contact windows are well defined and do not have the slope of an oxide window. This causes difficulty with stress and shadowing of deposited metal contacts. Generally, the silicon nitride is deposited over a thin silicon dioxide film in the contact windows. The etching of the oxide is accomplished using the silicon nitride as a mask. This procedure in many cases causes "shelving" (see figure 53) of the silicon nitride at the oxide interface due to lateral etching of the oxide. This can cause shadowing of the metal deposit, stress and cracking under thermal cycling. The so-called "shelving" causes the oxide step under the nitride to have a lateral etched shelf, possibly causing:

1. Discontinuity in metal film contact
2. Stress in deposited metal film
3. Variation in thickness of deposited metal films
4. Alloying at elevated temperature (400^oC) due to cracking or shadowing in barrier metal (Pt, Pd).

The scanning electron microscope is a valuable tool for determining the extent of this problem, and for determining process control improvements needed to minimize the effect in etching this composite film.

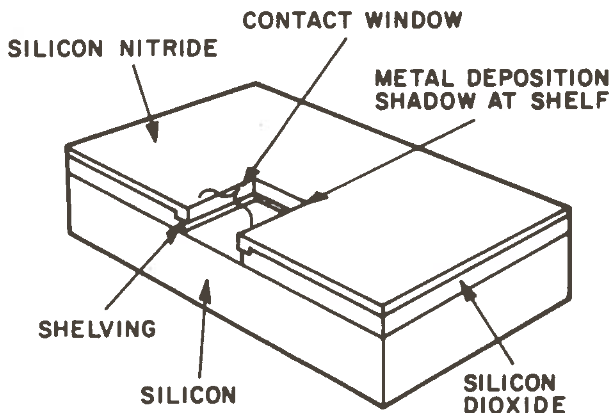


Figure 53.- Shelving in Oxide-Nitride Dielectrics

The barrier capability of silicon nitride can be monitored using the same MOS capacitor C-V measurement used on silicon dioxide. In this case, films of silicon nitride-silicon dioxide composite can be intentionally contaminated. It has been found that the etch rate of silicon nitride in buffered HF (25^oC) is a very good measure of film density and quality. Etch rates greater than 25 Å/min are an indication of films which will fail to mask the diffusion of sodium ions and water vapor. A graph of etch versus density, computed from oxygen content for Si_3N_4 films is presented in figure 54.

Exposure of oxidized silicon surfaces to ionizing radiation brings about permanent changes in the motion of a positive space charge in the insulation, and an increase in density of fast

METALIZATION

Metallization on an oxide-free surface is very important. A thin oxide or organics will prevent the formation of a uniform contact area. The following procedure has been used which has consistently yielded excellent results. Removal of organics takes place in an oxygen glow discharge (asher) for 30 minutes followed by a two minute etch (600 HO, 15 HF, $7HNO_3$) immediately preceding evaporation. Sputter etching for precleaning (refs. 58 and 59), is used; but generally not preferred since it heats the silicon wafer and can reoxidize the surface if a sufficient amount of oxygen is present. Various metals have been investigated and evaluated as ohmic contacts to silicon; however, only platinum has seen extensive use in beam lead technology. Electron beam evaporation and dc and r-f sputtering of platinum are being used but the best results are obtained with r-f sputtering. The sputtering system consists of a sputtering electrode for each metal and one backsputtering electrode with four water-cooled platens for slice holding. After an initial pumpdown to 10^{-6} torr, the chamber is backfilled with ultrahigh purity argon to slightly higher pressure (25 to 100 microns) while pumping against a restriction (e.g. partially opened high vacuum valve). This facilitates plasma initiation after which the electrode is presputtered for five minutes with the shutter in place. 500-800 Å of platinum is then deposited in six minutes using conditions outlined in Table 36.

TABLE 36.- SPUTTERING CONDITIONS

Source to substrate distance	1-1/4 inches
Chamber pressure	25 microns
Atmosphere	Ultra high purity argon
RF power	100 watts
Platen diameter	7 inches

Formation of platinum silicide takes place at temperatures from 550-700°C. It can be formed inside the vacuum chamber or preferably in a tube-type furnace. Heating in the vacuum system requires jigging which, when heated, adds considerably to the pumping time and makes frequent maintenance necessary. In order to prevent the silicon surface from oxidizing through the thin platinum layer, the wafers are loaded immediately after deposition onto a cool boat in a vertical position parallel to the gas flow. After a five-minute flush, the boat is positioned in the tube outside the furnace end before heating for 20 minutes at 640°C. The boat is cooled at the tube end for 10 minutes. Before heating, the platinum surface is uniformly colored and afterwards is gray in the contact windows. If a change in color is not observed, then silicide is not formed. The excess platinum over the oxide is removed using room temperature aqua-regia which does

of 100 Å/min to a total thickness of 900 Å. Platinum is deposited at a rate of 200 Å/min to a thickness of 2000 Å preceded by another five-minute presputtering step. Either of two processing procedures are used: the platinum properly masked with photoresist covering the metallization pattern, is etched in $HCL/HNO_3/H_2O$ at 80°C. Thus, the titanium becomes the conductive metal for gold plating. The second procedure requires gold plating directly on the platinum using titanium and platinum as the conductive metals for gold plating.

Gold beams are electroformed in two steps using separate photoresist techniques (ref. 61). A positive type resist is used for the interconnecting metal since fine line geometries are needed. In the second plate, where fine geometries are not needed, a negative resist is preferred becuase of better durability for the longer plating times required. Acid type gold baths (refs. 61 and 62) having a gold content of 0.7-1.5 troy ounces per gallon, a density of 14° to 16° baume, and operating at a temperature of 45°C are used. In addition to adhesion, thickness and ductility are of prime concern. Thicknesses are checked optically during plating. A microhardness test after plating is used as a measure of ductility. Interconnecting metal is plated to 0.1 mil and the beam buildup requires a total thickness of 0.5 mil. The gold plating is baked in a nitrogen atmosphere at 350°C to improve beam adherence. The titanium is etched from between the beams, the gold beams themselves acting as the etch mask. Over etching can be a problem which results in a weakening of the beam adhesion. An alternative sputter-etch technique involves the removal of platinum using gold beams as the mask. Uniform removal from areas having a width of <0.2 mil are practical without undercutting the larger areas, which is sometimes a drawback for chemical etching. Either of two procedures can be followed for effective platinum removal. One is the use of argon as the ionizing gas; the bombardment continues into the titanium layer requiring a thicker titanium layer. In the second procedure, oxygen in argon is the ionizing gas. In this case the titanium forms an oxide which protects the titanium film from attack. This thin oxide is subsequently removed by sputter-etching. In the case of titanium-molybdenum-gold, each metal is removed selectively using chemical etches.

REFERENCES

1. Schnable, G.L. and Keen, R.S.: Metallization and Bonds- A Review of Failure Mechanisms. Reliability Physics Symposium, 1969.

2. Vossen, J.L. and O'Neill, J.J., Jr.: Evaporation of Aluminum with rf-Induced Substrate Bias. RCA Review, Volume 31, No. 2 June 1970.

3. Black, James R.: Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons. Sixth Annual Reliability Physics Symposium, Los Angeles, Calif., Nov. 1967.

4. Schnable, G.L. and Schlegel, Earl S.: Study of Failure Modes of Multilevel Large Scale Integrated Circuits. Contract NAS 12-544, Philco-Ford Corporation, Microelectronics Division.

5. Black, James R.: Metallization Failures in Integrated Circuits: Technical Report No. REDC-TR-68-243, October 1968.

6. Washburn, E.W., Ed. in Ch.: International Critical Tables of Numerical Data, Physics, Chemistry and Technology. McGraw-Hill, Inc., 1929, Vol. VI, pp 160-165 and 202-205.

7. Hartman, T.E. and Blair, J.C.: Electromigration in Thin Gold Films. IEEE Transactions on Electron Devices, ED-16, No. 4, 407-410, April 1969.

8. Schnable, G.L., Keen, R.S. and Loewenstern, L.R.: Study of Contact Failures in Integrated Circuits, RADC-TR-331, Final Report, Prepared by Philco-Ford, Microelectronics Division. Contract No. AF30(602)-4034, 1967.

9. Schnable, G.L. and Keen, R.S.: Study of Contact Failures in Semiconductor Devices. Final Report, RADC-TR-66-165, prepared by Philco-Ford, Microelectronics Division. Contract No. AF30(602)-3610, 1966.

10. Schnable, G.L. and Keen, R.S.: Aluminum Metallization-Advantages and Limitations for Integrated Circuit Applications. Proceedings of the IEEE Vol. 57, No. 9, 1570-1580, 1969.

11. Sarace, J.C., et al.: Metal-Nitride-Oxide-Silicon Field-Effect Transistors, With Self-Aligned Gates. Solid-State Electronics, Vol. 11, 653-660, 1968.

12. Vadaz, L.L., et al.: Silicon-Gate Technology. IEEE Spectrum, 28-35, October 1969.

REFERENCES (CONTD)

26. Davidse, P.D.: RF Sputter Etching. A Universal Etch. American Vacuum Society, 13th, p 51, 1966.

27. Tsue, R.T.D.: Ion Etch Technique and Its Applications. 2nd Symposium on Thin Films by Sputter, Consolidated Vacuum Corp., 53, 1967.

28. Lepselter, M.P., Waggener, H.A., Davis, R.E.: Beam-Leaded and Intraconnected Integrated Circuits. 1964 Electron Device Meeting, Washington, D.C.

29. Murphy, B.T., Waggener, H.A., Iwerson, J.E.: 1965 IEEE Solid States Circuit Conference. Philadelphia, Pa.

30. Hansen, Constit. Binary Alloys.

31. Coughlin, J.: Contribution of the Data on Theoretical Metallurgy XII, Heats and Free Energy of Formation of Inorganic Oxides, U.S. Gov. Printing Office Washington, 1954.

32. Matano, C.: Japan Journal of Physics (Trans) 8, 109, 1933.

33. Neuhuys, T.M.: Integrated Aluminum Connections. Proceedings of the Electronic Components Conference, 1969, pp. 46-51.

34. Mai, C.: Private Communication.

35. Dudley, R.H., Labude, E. F.: A Reliable Contact for Insulated Gate Effect Integrated Circuits. Paper presented at PGED Conference, Washington, D.C., 1969.

36. Benjamin, P., Weaver, C.: Proc. Royal Soc., London, 254A (1960), 163; 261A (1961) 516.

37. Hooper, R.C., et al.: Solid-State Electronics 8, (1965), 831.

38. Legat, W. H., Tiefert, K.H., Rosvold, W.C.: Electrochemical Society Meeting Detroit, Michigan. 1969.

39. Beatty, R.P.: Metallization Systems for Integrated Circuits. NASA TN D-5866.

40. Eaton, K.H.: Beam Leads for Complex Integrated Circuit Arrays. (AD-824-402) General Instrument Corp., Adv. Microelectronic Res. & Dev. Center. 1967.

41. Wilson, R.W., Terry, L.E.: Integrated Circuit Metallization: A Comparison. Electronic Packaging and Production, sec. 2., Oct. 1970, pp. MC29-MC40.

REFERENCES (CONTD)

56. Salama, C.A.T.: Rf Sputtered Aluminum Oxide Films on Silicon. J. Electro. Society, vol. 117, 1970.

57. Ribner, A.: Preparation and Prospects of Aluminum Oxide Films for MIS Transistors. Tech. Report 70-355.1, GTE Laboratories, 1970.

58. Luke, P.G.: The application of Sputtering to Beam Lead Technology. Microelectronics, June 1970.

59. Legat, W.H.: Contact and Interconnection Technology. J. of Vacuum Science and Technology, vol. 7, 1970.

60. Shamash, M.B. Filp-Chip/Beam-Lead Microbonding Techniques. Proceedings of the 2nd INTER/NEPCON 1969.

61. Hodgson, R.W.: IC Pattern Generation- A Resist Process. Elect. Packaging and Production, vol. 10. 1970.

62. Hodgson, R.W. and Scudlapski, A.H.: Gold Plating in the Manufacture of Solid State Electron Devices. Conference Record of Second Plating in the Electronics Industry Symposium, 1969.