ORT NO. HS-801-736

NONDESTRUCTIVE TESTING SYSTEM FOR RETREADS

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NOVEMBER 1975
FINAL REPORT

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
NATIONAL HIGHWAY TRAFFIC SAFETY ADMINISTRATION
Research and Development, Office of Vehicle Safety Research
Crash Avoidance Research Division
Washington DC 20590

Technical Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
HS-801-736	TSC-NHTSA-75-4	

4. Title and Subtitle
NONDESTRUCTIVE TESTING SYSTEM FOR RETREADS

5. Report Date
November 1975

6. Performing Organization Code

7. Author(s) Henry H. Bessler, Stephen N. Bobo, Manuel J. Lourenco, William R. Wade

8. Performing Organization Report No.
DOT-TSC-NHTSA-75-4

9. Performing Organization Name and Address
U.S. Department of Transportation
Transportation Systems Center
Kendall Square
Cambridge MA 02142

10. Work Unit No. (TRAIS)
HS603/R6407

11. Contract or Grant No.

12. Sponsoring Agency Name and Address
U.S. Department of Transportation
National Highway Traffic Safety Administration
Research and Development, Off. of Veh. Safety Research
Crash Avoidance Research Division
Washington DC 20590

13. Type of Report and Period Covered
Final Report
July 1974 - October 1975

14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

An important problem in retreading tires is the assurance of a satisfactory casing. Since 1972 the National Highway Traffic Safety Administration has had under development an air-coupled through-transmission ultrasonic inspection system for finding anomalies in casings. This report describes the results of this development in sufficient detail to permit its reproduction by a reasonably competent electronics manufacturer. The reader is cautioned that the equipment described will not find all anomalies in every casing, and that system cost effectiveness depends heavily on the way the equipment is used, the tires it inspects, and the types of anomalies considered to be detrimental to retreading.

17. Key Words
- Retread Inspection
- Nondestructive Retread Inspection
- Tire Testing

18. Distribution Statement
DOCUMENT IS AVAILABLE TO THE PUBLIC THROUGH THE NATIONAL TECHNICAL INFORMATION SERVICE, SPRINGFIELD, VIRGINIA 22161

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	94	

Form DOT F 1700.7 (8-72) Reproduction of completed page authorized

PREFACE

The work covered in this report was accomplished in support of the Nondestructive Tire Testing Project for the National Highway Traffic Safety Administration, Mr. Manuel J. Lourenco, Program Coordinator.

The authors are indebted to the Crash Avoidance Research Division for its assistance and support in this project.

Valuable industry assistance came from the Tire Retreaders Institute, Mr. A. Janarelli, Director of Research; The American Retreaders Association, Mr. Ed J. Wagner, Managing Director; and from Teknekron Corporation, Berkeley, California, the manufacturer of the electronic equipment.

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1. GENERAL DISCUSSION

1.1 PURPOSE AND SCOPE

1.1.1 Purpose

The National Highway Traffic Safety Administration (NHTSA) has sponsored a nondestructive tire testing program whose objective is to find means of reliably and economically detecting safety-related anomalies in tires. In keeping with this objective, the Transportation Systems Center (TSC) of Cambridge, Massachusetts, has developed an air-coupled ultrasonic inspection system for inspecting retread tires. This report describes that system.

1.1.2 Scope

System characteristics and constraints and the potential for its duplication are listed below:

a. The system developed by NHTSA/TSC can detect a majority of the separations found in worn casings prior to retreading.

b. The system's ability to detect separations and the sizes of these detectable separations depend on uncontrollable variations such as the residual tread on a casing and the condition of that tread.

c. The system does not relate anomalies in tire casings to their ability to survive retreading.

d. This document contains sufficient design and technical information which, with minor development to fulfill specific requirements, will permit manufacture of an ultrasonic casing inspection system.

1.2 MAJOR COMPONENTS OF THE TEST EQUIPMENT

The tire testing equipment (figure 1-1) consists of three major components:

a. A rugged mechanical framework which contains the means for securing the tire to a rotating shaft and its rotation by a

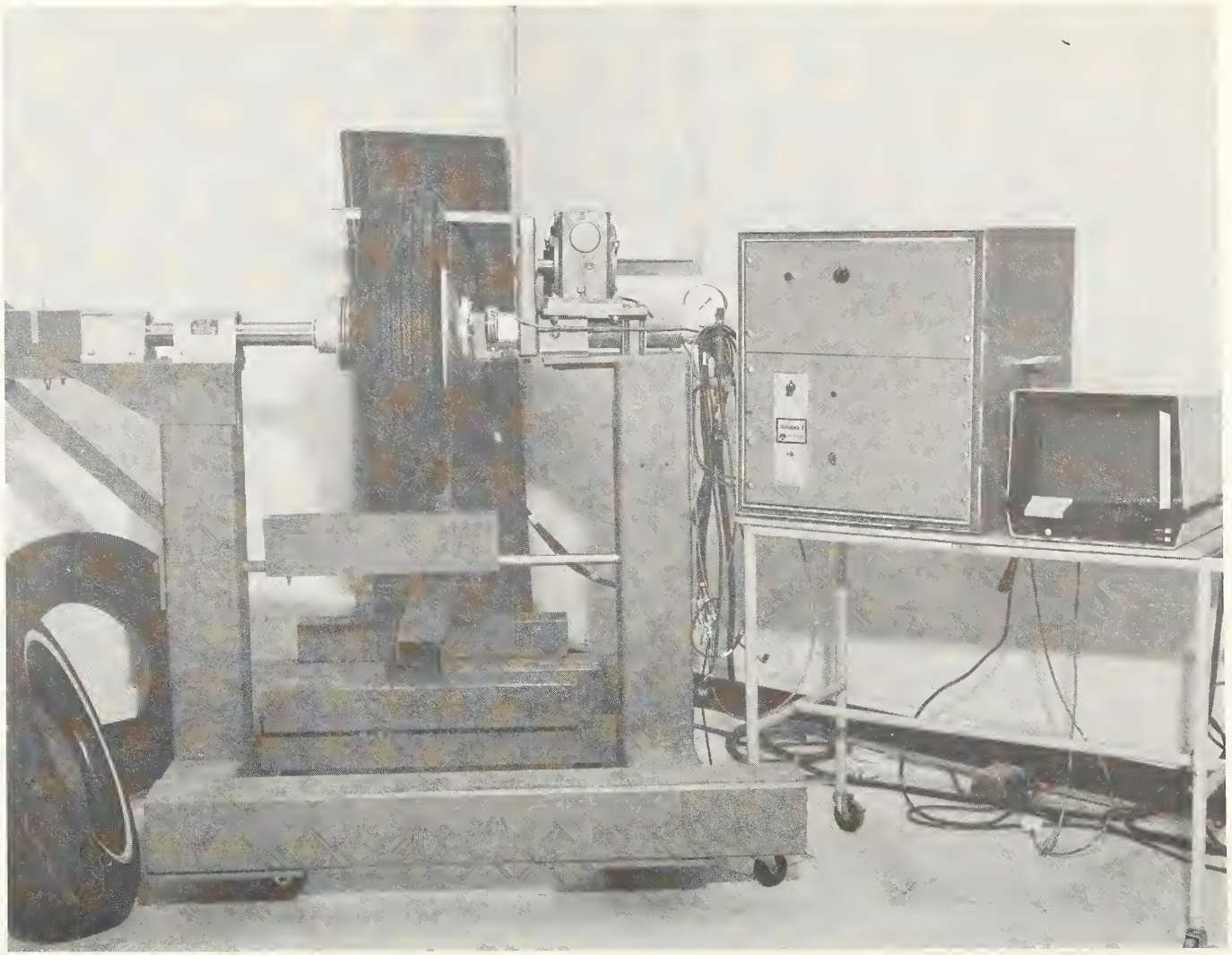


Figure 1-1. Nondestructive Testing System

drive motor. The mechanical system must retain the original geometry of the tire and present it to the sensors with a minimum of runout. To do this the mechanical fixture must hold the beads at measuring rim spacing, and the tire must be inflated to a low pressure (2 to 4 psi). These requirements are in addition to such requirements as easy interchange and quick mount and dismount.

b. A cabinet which houses the electronic circuits with visual display, and other electrical controls.

c. A storage scope display device. This instrument provides visual indications of waveforms whose interpretation qualifies the condition of the tire casing.

1.3 BRIEF DESCRIPTION OF THE TEST EQUIPMENT OVERALL FUNCTION

The test concept as applied consists of exposing the tire surface to ultrasonic energy and observing its effects by means of visual waveform interpretations. The concept is implemented by excitation of piezoelectric transducers to convert sound transmission first to electrical, and ultimately, after processing, to visual responses.

The tire is first mounted between the rims (figure 1-2), and a suitable air pressure is applied to the tire. A motor, mounted on the mechanical framework and geared to the main shaft, causes rotation of the tire.

In addition to the rims, which press against the tire, figure 1-2 also shows the transducers, which are involved in the sound reception referred to above. The center transducer is known as the transmitter transducer, and the peripheral ones (twelve are actually used in the NHTSA/TSC prototype) as receiver transducers. The positioning of the transducers as shown in figure 1-2 permits the tire to be situated between transmitter and receiver transducers, as shown in figure 1-3. The transmitter and receiver transducers are in line, so that received sonic energy is modified by conditions within the tire.

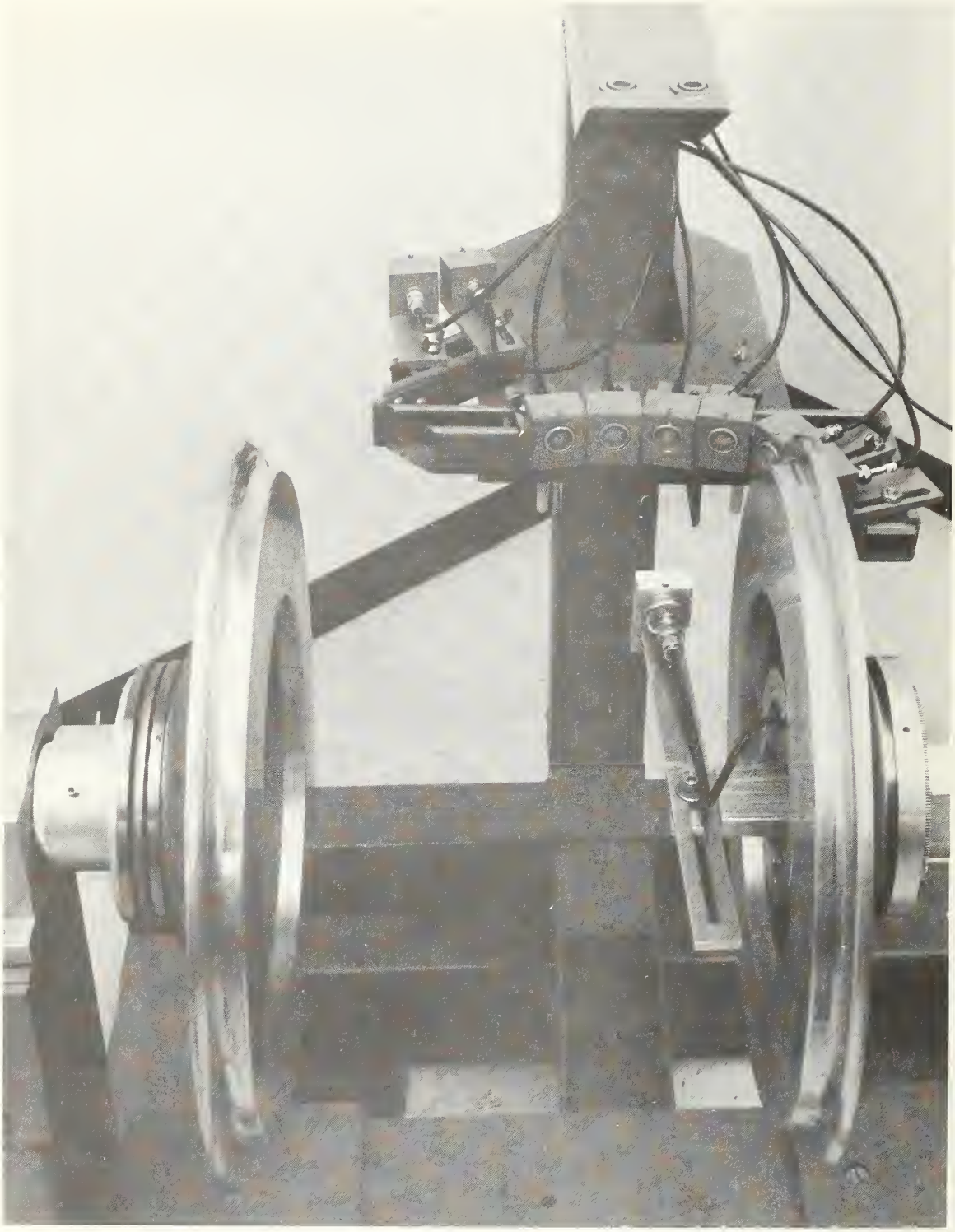


Figure 1-2. Rims and Transducers Locations

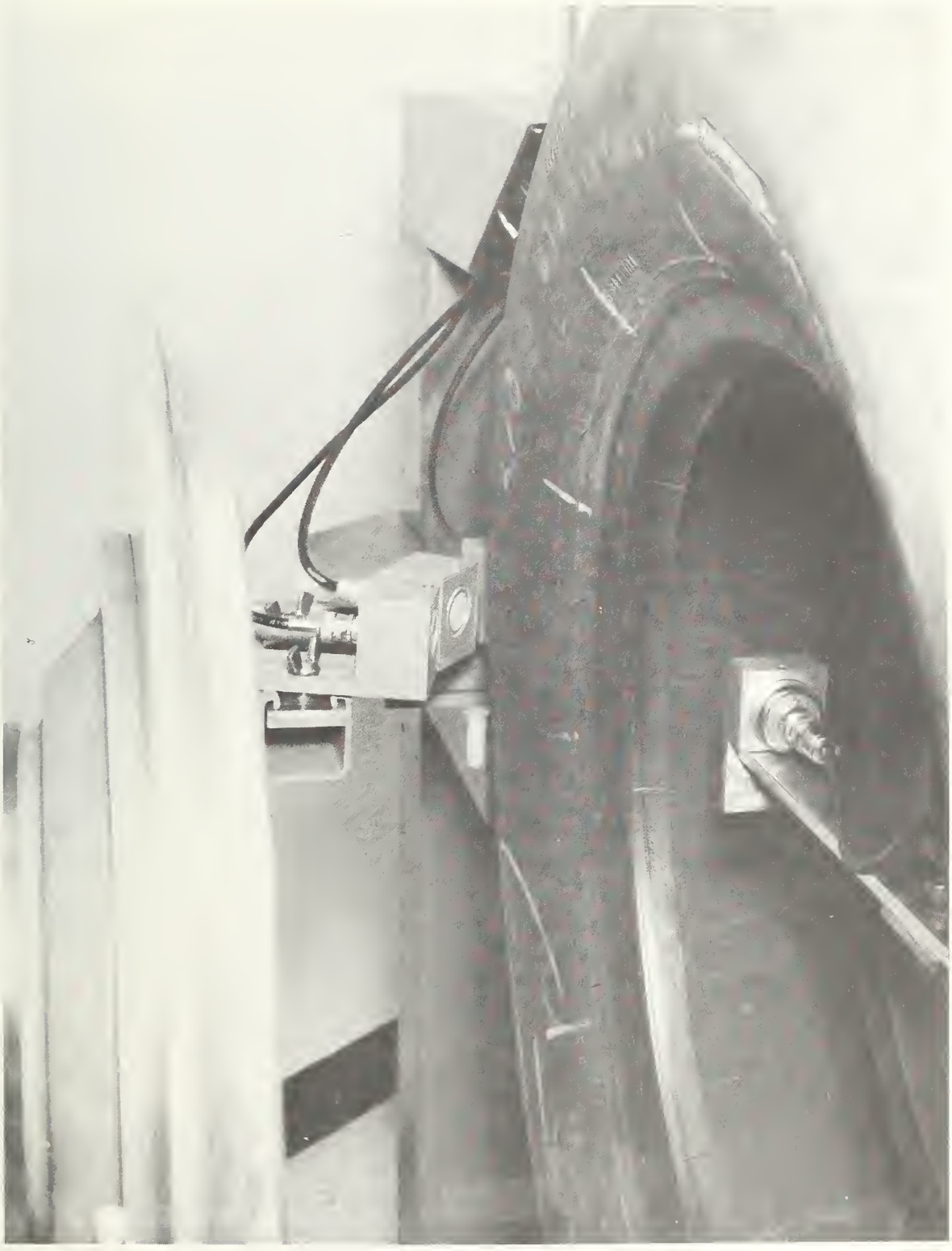


Figure 1-3. Relative Position of Tire and Transducers (Rim Removed from Tire)

The transmitter transducer is excited by a 25-kHz ultrasonic signal which traverses the tire on its path to the receiver transducers. The receivers convert the ultrasonic signal into electrical signals, which undergo further processing in appropriate circuits to provide a storage tube waveform which can be interpreted to identify and position any contained tire anomaly. During tire rotation, the encountered anomalies such as separation of layers, bruises, and breaks will each cause a different signal attenuation, which will be evidenced by the obtained visual indication. By proper interpretation it is possible to evaluate the tire's suitability for retreading.

1.4 SYSTEM CHARACTERISTICS

The following characteristics and specifications are provided for the NHTSA/TSC prototype. The data are divided into the following categories:

a. Mechanical

b. Overall electrical characteristics

c. Specifications for agc (automatic gain control) amplifier board (receiver)

d. Power requirements for receiver.

Mechanical

(a) Overall dimensions:	4-1/2'W x 4'L x 4-1/2'H
(b) Total weight:	1000 lbs
(c) Test pressure applied to tire under test:	2 to 4 psi
(d) Rim size:	13", 14", or 15" interchangeable
(e) Quantity and location of ultrasonic transducers:	13 (12 receivers around tire, bead to bead, and 1 transmitter)
(f) Rotation rate of tire:	Adjustable 0 to 20 rpm; 15 rpm optimum
(g) Duration of test:	2-1/2 minutes

Overall Electrical

(a) Input voltage, frequency, and current rating:	110 Vac, 60 Hz, 20 A
(b) Characteristics of motor drive:	Dc motor, variable speed control
(c) Type of transducer output display:	Tektronix Model 613 storage display
(d) Type of transducer:	Piezoelectric, ultrasonic
(e) No. of transducers:	13 (12 receivers and 1 transmitter)
(f) Frequency of transmission:	25 kHz nominal

Agc Amplifier Board Specifications

Input resistance:	27K ohms
Noise figure, R_o = 20K ohms:	2.0 dB
Maximum input voltage:	100 mV
Maximum gain:	86 dB
Agc range:	60 dB
Bandwidth, f_o = 23.7 kHz	10 kHz
Peak detector acquisition time:	200 μS
Peak detector hold time to 10 mV:	20 mS
Peak detector range:	>40 dB
Peak detector maximum output level:	13 volts
Peak detector output impedance:	<10 ohms

Power Requirements for Receiver

+20	Vdc	±5%	@ 10 mA
+15	Vdc	±0.5%	@ 500 mA
+12	Vdc	±5%	@ 500 mA
+5	Vdc	±0.5%	@ 1.0 A
-15	Vdc	±5%	@ 300 mA

2. FUNCTIONAL DESCRIPTION

2.1 SIMPLIFIED BLOCK DIAGRAM OF SYSTEM FUNCTION

The NDT (nondestructive test) system function is described below and illustrated in figure 2-1. The transmitter transducer is excited with a 25-kHz signal which is directed, from within, at the tire casing, and in traversing the tire body is attenuated, detected by the receivers, amplified, processed, and finally depicted on the storage tube for interpretation. The interpretation will enable an observer to distinguish defective tire casings from the sound quality casings.

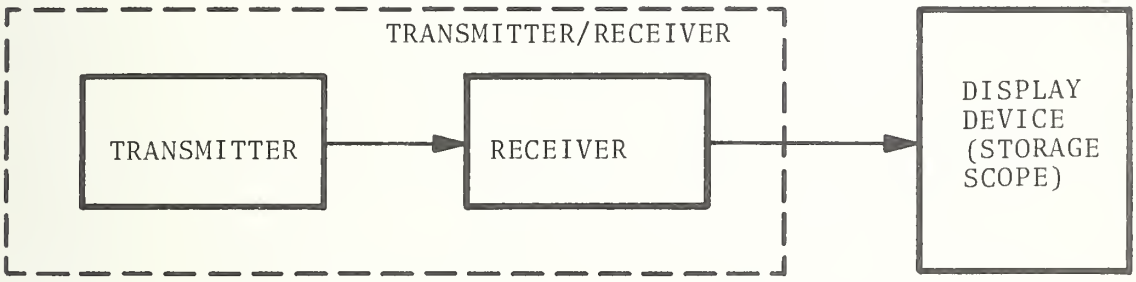
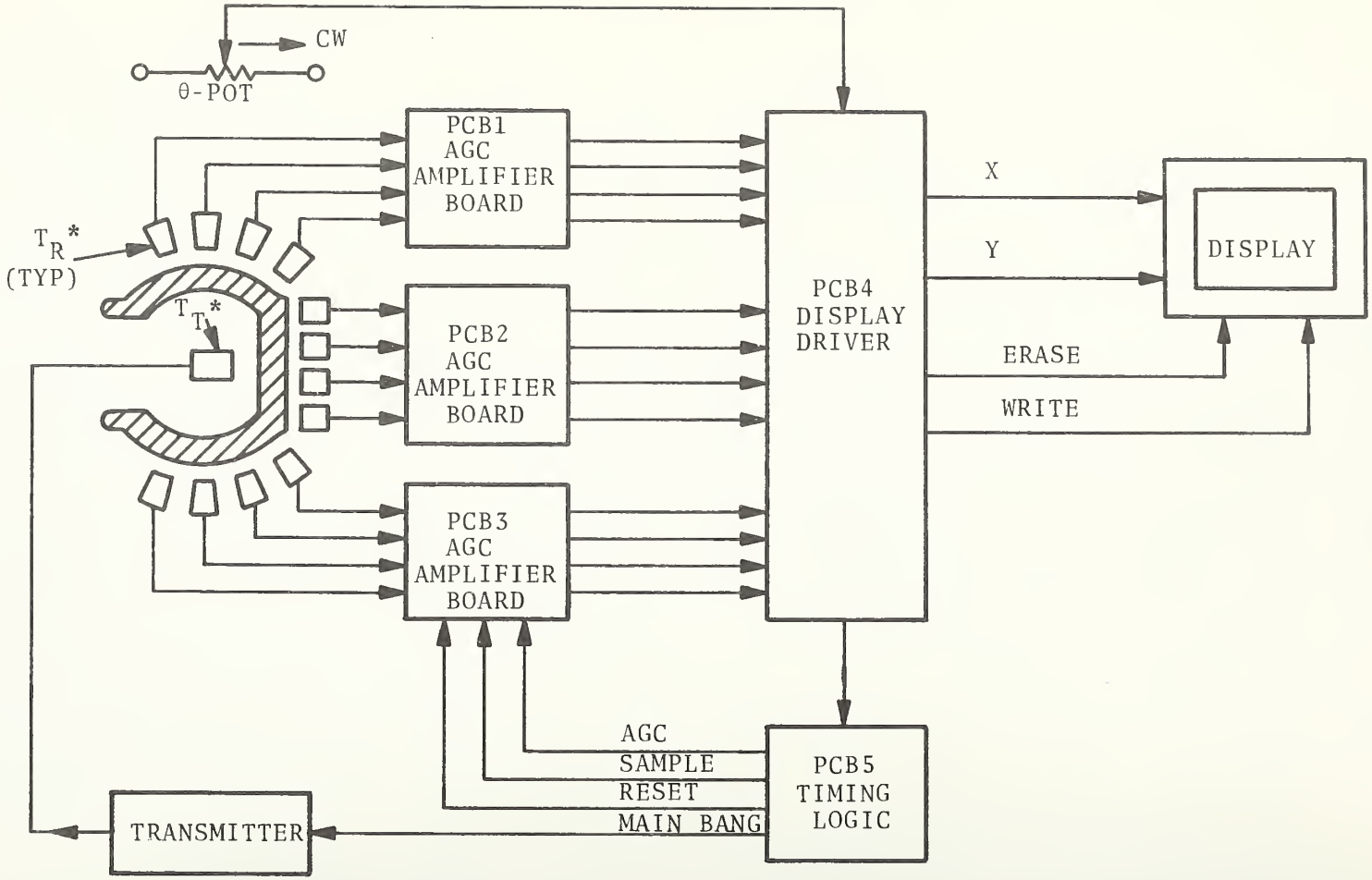


Figure 2-1. Basic Concept of the System Function

2.2 BLOCK DIAGRAM DISCUSSION OF THE TEST SYSTEM (Figure 2-2)

2.2.1 General Discussion

a. Figure 2-2 is essentially an electronic-signal-flow block diagram depicting the major components that comprise the system. An electrical signal initiated in the transmitter transducer as shown in figure 2-2 at the center of the receiver array will impinge on the section of tire which lies in the same plane as that of the transducers, and the resulting instantaneous signal obtained at the display device will identify that portion of the tire which was ensonified by the transmitter. Since this indication represents only one position of the tire casing, a complete tire inspection would require at least one revolution. In practice, more revolutions are completed during a tire test to ensure that the required data are contained with respect to a starting rotation



*T_T = TRANSMITTER TRANSDUCER

T_R = RECEIVER TRANSDUCER

Figure 2-2. Overall System Block Diagram

reference. (This is discussed further in paragraph 2.3.3g.)

b. The inspection system contains twelve identical channels, corresponding to the twelve receiver transducer inputs of figure 2-2. Each channel is related to a particular portion of the tire, and each portion is characterized visually on the display device. Thus, with the receiver transducer layout shown in figure 2-2, the total periphery of the tire cross section is inspected at each incremental position of the tire during its rotation.

2.2.2 System Input (Transmitter/Transducers)

The system input consists of pulses from a transmitter (part of figure 2-3) which provides 25-kHz ultrasonic pulses at a pulse repetition rate of 60 per second. The transmitter transducer emits the signals through an air/tire casing medium to the receivers.

2.2.3 Agc Amplifier Board

a. The agc amplifier board accepts and processes received output signals from four channels simultaneously. Since twelve similar channels are utilized in system operation, three identical agc amplifier boards are used, and except for the coexistence of identical components for different channels on the same integrated circuit chips, each channel operates independently of all the others.

b. The agc amplifier circuit (figures 2-2 and 2-4) for one channel includes a preamplifier, clipper, agc amplifier, and peak detector circuit. Each input to the agc amplifier circuit is amplified, amplitude-limited, gain-controlled, and ultimately converted to a dc output voltage by the respective circuit whose peak dc level is proportional to the signal level out of the receiver transducer.

2.2.4 Display Driver

a. The display driver (figures 2-2 and 2-5), which receives the agc amplifier board signals, provides twelve vertically spaced line plots on the storage scope corresponding to the twelve

receiver channels. The vertical displacement represents the receiver spacing about the tire in a bead-to-bead direction. Each of the twelve lines generated within the display driver is at a specific dc voltage level above a common reference. When the voltage level of a line is combined with the signal voltages from the agc amplifier board, there results a modulated line with voltage variations corresponding to the variations from one of the twelve receiver channel outputs.

b. The method whereby twelve simultaneous signal outputs from the agc amplifier board are processed through one multiplexer circuit in the display driver is described in paragraph 2.3.3b.

c. The display driver also provides erase and write signals. The erase signal appears at the switch-on of the inspection interval, and removes from the display screen any previously existing information. After the erase signal has served its function, a write signal is activated which permits the line plots to be generated.

d. Horizontal sweep for the storage scope display is initiated by a ramp voltage obtained from the rotating arm of a potentiometer (θ-POT, figure 2-2, and R8, figure 2-5). A full trace is indicated on the display on completion of one revolution of the potentiometer arm. Since the rate of rotation of the arm is identical to that of the tire, a full trace on the display also represents one revolution of the tire.

2.2.5 Timing Logic

The timing logic board (figures 2-2 and 2-6) provides sequenced pulses which will permit processing of signals from the transducers to system display outputs. The timing operation is detailed further in the discussion of the timing logic board diagram (subsection 2.3.4).

2.3 DETAILED BLOCK DIAGRAM DISCUSSION

2.3.1 System Clock/Transmitter (Figure 2-3)

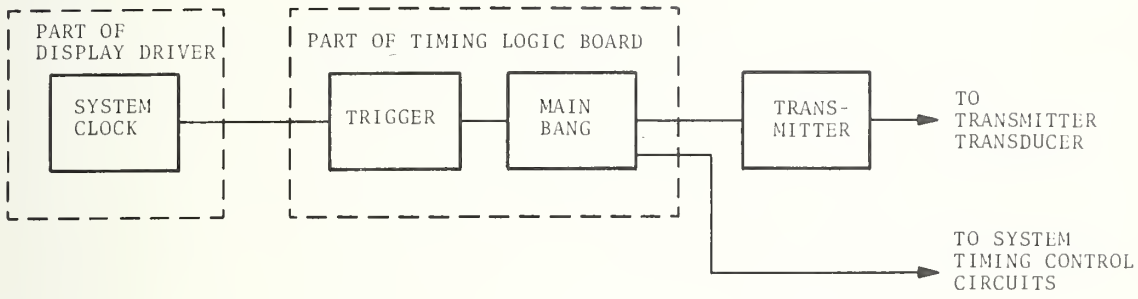


Figure 2-3. System Clock/Transmitter

A 60-Hz clock for overall timing control of the system is used with the transmitter, where power to drive the piezoelectric-type transducer is generated. The clock circuit also controls the timing sequences for the remaining system functions. A monostable multivibrator driven by the system clock triggers another monostable multivibrator (main bang) to provide a 25-kHz input to the transmitter, which provides high-voltage excitation to the transmitter transducer. The system clock is an integrated circuit located physically on the display driver board. The transmitter is located on a separate chassis and the multivibrators are part of the timing logic board.

2.3.2 Agc Amplifier Board (Figure 2-4)

a. The agc amplifier has provision for permitting the test system to detect separations of different extent between adjacent parts of a tire. The transmitter-to-receiver signal is attenuated a nominal amount in traversing the tire body. If in its rotation, the portion of tire illuminated by the transducer has an anomaly, the signal will be altered in relation to the nonhomogeneity encountered. Therefore, the agc amplifier is provided with fast-attack and slow-decay time constants to account for the

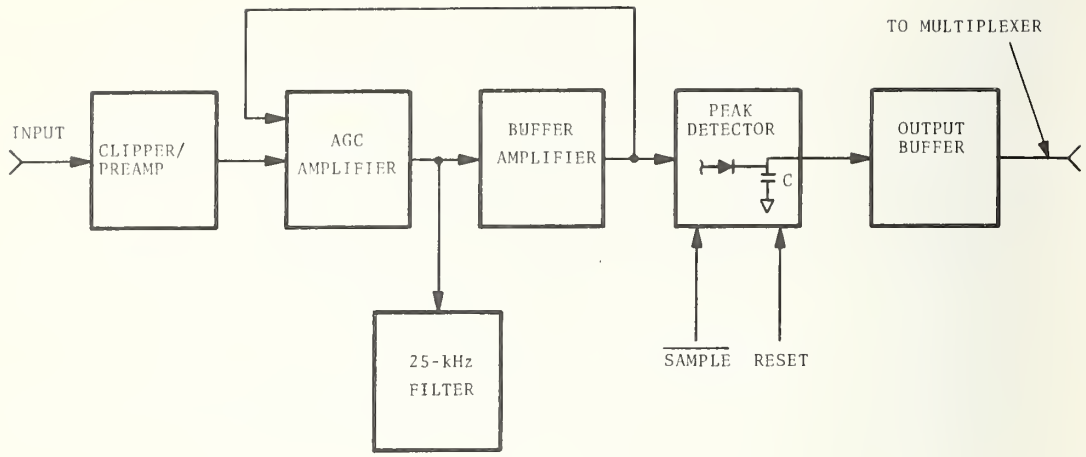


Figure 2-4. Block Diagram Detail of Agc Amplifier Board

nonhomogeneity. In this way the gain of the amplifier will respond so as to compensate for the sudden discontinuities of the tire.

b. The signal from the receiver transducers is sequentially applied to the input of a preamplifier/clipper circuit, where it is amplified up to a maximum of 20 dB above the input level. Amplification in excess of this value is prevented by means of the clipper circuit following the preamplifier. This signal is then fed to an agc amplifier, whose gain is controlled in response to the signal input to maintain a proper signal level to the succeeding peak detector circuit. The signal input to the peak detector is converted to a dc output voltage which charges a capacitor in the peak detector output circuit (C, figure 2-4) to the peak value of the signal input. This peak dc voltage is then applied through an output buffer to the analog multiplexer of the display driver.

c. A 25-kHz filter (figure 2-4), connected from the agc amplifier output to ground, is used to bypass noise from the peak detector circuit. This filter is a 25-kHz parallel resonant circuit, which presents a high impedance to the 25-kHz signal and a low impedance to extraneous noise frequencies. The 25-kHz signal is permitted to pass on to the input of the peak detector, and the noise introduced from the agc amplifier during its gain control function is bypassed to ground.

d. The peak detector of the agc amplifier board provides peak dc voltages in response to transmitter transducer signals which traverse the tire casing and continue on to the receiver transducers. The peak detector output voltage is permitted, for a predetermined enable period, to charge a capacitor (C, figure 2-4) in the output circuit of the peak detector. The voltage across this capacitor is applied to the analog multiplexer of the display driver (by way of an output buffer in the agc amplifier board), and is further processed to provide modulation indications on the display device. After the peak detector enable period has passed, the voltage still remains on the capacitor. This voltage must be removed before the beginning of the next peak detector enable period, so that a new peak voltage can occur in response to the next input (main bang) pulse. Removal of the voltage from the capacitor is accomplished by a bleeder circuit which effectively shorts the capacitor to ground for an extremely short period. This effective shorting is accomplished by a circuit which is triggered by a RESET pulse.

e. The following text considers the enable period and its relationship to a SAMPLE voltage:

(1) The peak detector enable period referred to in paragraph d is initiated on the trailing edge of the RESET pulse. On removal of the RESET pulse, the effective short is removed from the peak detector circuit capacitor (C, figure 2-4), and during the ensuing enable period the voltage once more builds up on the capacitor until a new peak value related to the transducer input is reached. On completion of the enable period, the peak voltage on the capacitor is available for input to the analog multiplexer. This peak voltage remains on the capacitor until the trailing edge of the next RESET pulse appears, and the cycle repeats with the next peak detector enable period.

(2) The enable period is of short duration when compared with the time between successive peak detector enable periods. Therefore, for most of the time between successive enable periods, the peak detector circuit is effectively shorted to ground, and no signal arrives at the input to the analog multiplexer. This

effective shorting is accomplished by application of a positive-polarity SAMPLE voltage level to the circuit which creates the effective short. When the enable period is to be initiated, the SAMPLE signal is removed (in digital terminology, the complement of the SAMPLE voltage is applied to the circuit).

(3) In summary of the sequence of events described in paragraphs d and (1) and (2) of e, the RESET pulse goes from high to low (on the trailing edge); the peak detector enable period is initiated by the complement of the SAMPLE voltage; and the peak detector output voltage is transferred from the agc amplifier board to the display driver.

2.3.3 Display Driver (Figure 2-5)

a. The system clock, although physically part of the display driver board, functions independently to create the time interval within which the ultrasonic transmissions are propagated from the piezoelectric transmitter transducer. The time pulses initiate the generation of 25-kHz main bang pulses, which are applied as excitation to the transmitter input. The transmitter output provides sufficient voltage amplitude to drive the transmitter transducer.

b. The display driver provides signals to the vertical and horizontal inputs of the display whereby visual indications are established corresponding to the ultrasonic inputs. Signals from the peak detector of the agc amplifier boards are applied to the input terminals of an analog multiplexer, which accepts the twelve inputs and transfers them through a one-line output to a summing amplifier. This is accomplished by chopping up the incoming signals into very small segments, and passing these segments sequentially through the multiplexer. In effect, a small bit of information from each signal is passed through in rapid sequence at a rate determined by the address logic, and this sequence is repeated until the complete information from all the incoming signals has been processed to the summing amplifier.

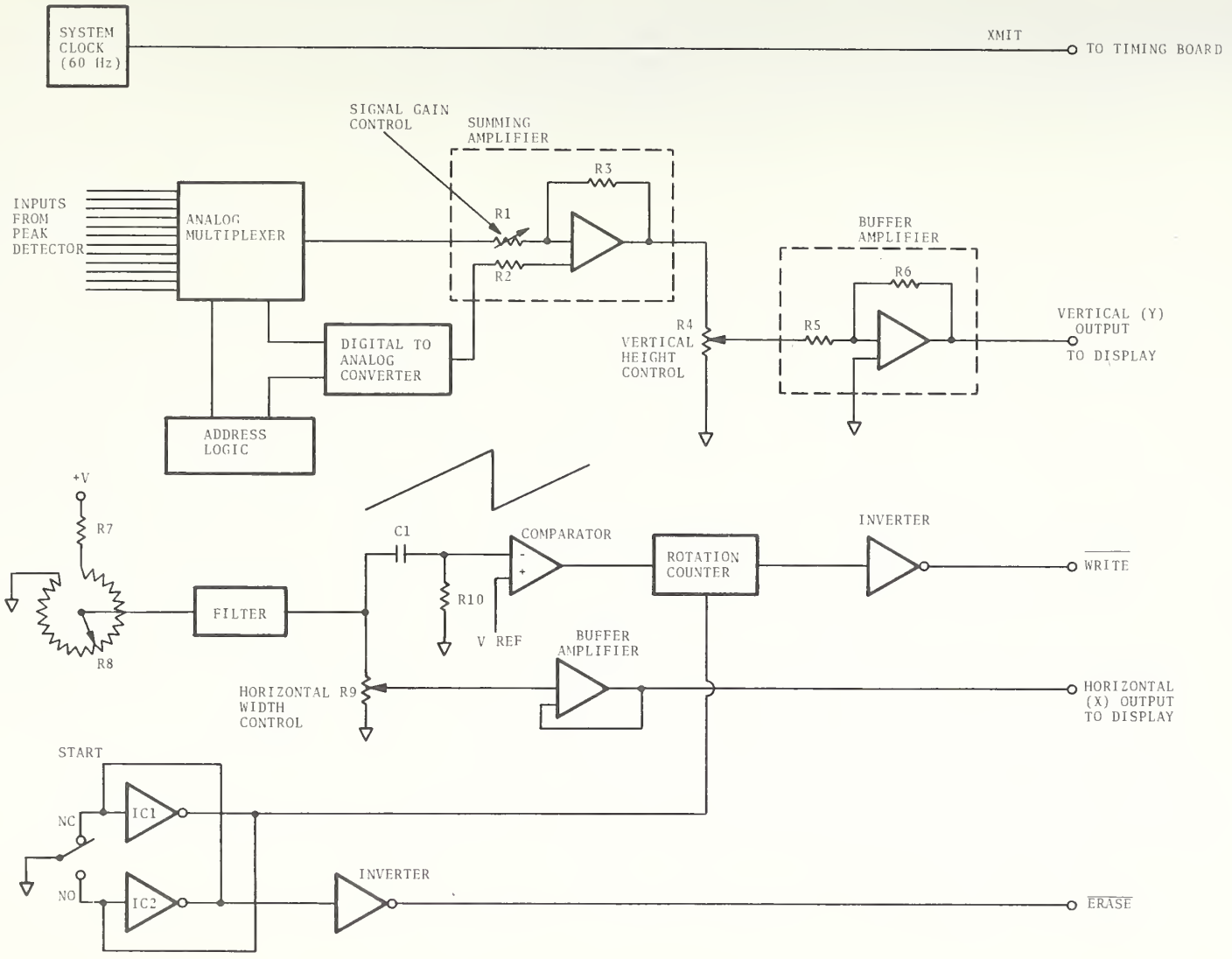


Figure 2-5. Display Driver, Block Diagram

c. The signal information discussed in paragraph b refers to modulation information which is superimposed upon twelve vertically separated signals already present at the display device. These separate signals, created by voltage levels much greater than the modulation voltages, are obtained by use of a digital-to-analog converter and a summing amplifier. The summing resistors R1 and R2 (figure 2-5), together with feedback resistor R3, provide an output sum voltage, the parts of which are proportional to the ratio of R3 to R1 and R3 to R2 respectively. Although R2 is shown as an individual resistor, it actually represents different combinations of parallel resistors, with the resistor grouping depending on the logic output provided by the address logic. Also, resistor R1, which serves additionally as a gain control for the signal input, is fixed in value once the signal gain has been set. Therefore, with the address logic designed to provide twelve possible combinations of R2, there will be twelve different voltage levels at the output of the summing amplifier, and, corresondingly, twelve different vertically separated lines on the display screen. The vertical height of the respective lines is further controlled by control resistor R4. The buffer amplifier amplifies all incoming signals uniformly, and also isolates the summing amplifier from the display device.

d. The address logic consists of a counter driven by a high-frequency clock. The counter provides binary voltage outputs corresponding to the decimal count from 0 to 11, at which time a feedback gate resets the counter for initiation of another sequence of similar binary outputs. These outputs are obtained from the counter on four lines which connect to both the analog multiplexer and the digital-to-analog converter. As the binary count increases from the equivalent decimal count 0 to 11, different combinations of the four output lines attain high or low voltage levels corresponding to the respective binary designations for the count. This combining action causes one of the twelve input signal lines to be transferred to the multiplexer output in the time segment determined by the clock driving the counter. The same output voltages from the counter are simultaneously applied to the digital-to-analog

converter, so that a particular set of resistors will be paralleled to form R2 of figure 2-5. In this way, a particular input line to the analog multiplexer has been matched to a particular R2 input to the summing amplifier, and a segment of that line is recorded on the display screen. This combined action establishes the voltage level for a particular line, and hence its vertical height on the display screen. The next binary count causes another input line to be matched to a different grouping of parallel resistors for R2, and a different line segment is recorded on the display screen. This process continues until all twelve lines have been recorded for the total duration of incoming signals from the peak detector of the agc amplifier board.

e. The horizontal trace for the screen of the display is derived from a periodic ramp voltage waveform across a potentiometer whose arm rotates continuously, and with the same angular speed as that of the tire being tested. This arm rotation is accomplished by having a potentiometer mounted adjacent to the main shaft of the test equipment, with the potentiometer shaft geared to the main shaft so that the turns ratio between the two is effectively one-to-one. The potentiometer is electrically connected to the display driver circuit as shown in figure 2-5 by R8 of the voltage divider R7-R8. Since the angular rotation is uniform (four seconds per revolution), the voltage across the potentiometer is linear; hence, the voltage increases linearly until the potentiometer arm attains its peak value; i.e., the voltage between ground and the junction of R8 with R7. (Note the ramp waveform in figure 2-5 located above the C1-R10 network.) At that instant, the voltage falls very rapidly to zero, and begins once more to rise linearly with continued rotation of the potentiometer arm. (There is a very small gap in the potentiometer winding. The short interval within which the potentiometer arm passes this gap coincides with the time of electrical separation between the peak and minimum values of the voltage waveform.) The potentiometer arm is connected to a filter which bypasses noise created in the potentiometer winding during rotation of the potentiometer arm. The filtered voltage is applied to a second potentiometer (R9), which

controls the width of the horizontal trace. Finally, the voltage from the horizontal width control is passed to the horizontal width input of the display device through a buffer amplifier.

f. The ramp voltage from R8, in conjunction with a START switch, contributes to the creation of a WRITE signal for insertion to the display, thereby permitting sweep indications on the display screen. (Actually, the complement of the WRITE signal is applied to accommodate the requirements of the display input.) As the arm of potentiometer R8 rotates from its ground end, the ramp voltage builds up to its peak value at the extremity of its forward travel. At the instant when the arm passes the gap in the potentiometer, the voltage drops very rapidly from its peak value to zero. This rapid voltage drop is applied to a high-pass network C1-R10, which permits transfer to one input of a comparator. The applied voltage is compared with a second input to the comparator (a reference voltage pickoff from a voltage divider network). The resulting comparator output is applied to a rotation counter, and the circuit is completed to ground through the armature of the START switch. When the START switch button is pressed and the rotation counter circuit ground is provided, the counter provides a count for two tire revolutions. On completion of the count, the display screen permits visual indications corresponding to the sweeps from the digital-to-analog converter and the audio modulation from the transducer channel inputs. The visual display persists for a specified time related to the display device function, after which the indication disappears from the screen. The tire may continue to rotate, but for another visual indication it is necessary to press the START button.

g. The reason for providing two revolutions is based on the relationship between the ramp voltage and the time at which the START button is pressed. The zero value of the ramp voltage corresponds to initiation of the horizontal trace, and the peak value corresponds to the end of the trace. Therefore, if only one revolution of the tire were considered, it would be necessary for the START button to be pressed exactly when the ramp voltage is zero in order for the entire trace to be recorded. Since the START

button can be pressed at any time desired by the operator, the likelihood of this coincidence occurring regularly is small. Therefore, in order to ensure that the entire trace will definitely be recorded at every pressing of the START button, an additional tire revolution is permitted in the operation. The second revolution of the tire makes certain that the entire trace is utilized for all twelve lines.

h. The WRITE signal is made available only after all previous information stored in the display device is removed by an ERASE signal. The latter signal [actually the complement ($\overline{\text{ERASE}}$) input to the display device] is obtained on pressing of the START button. This action provides a ground to the erase input to the display, and clears all stored information from the storage scope prior to application of the WRITE signal.

2.3.4 Timing Logic Board (Figure 2-6)

a. The timing logic board provides the circuits used for sequencing of pulses during signal transfer from the transducer channel inputs to the display device outputs. The block diagram of figure 2-6 shows the functional components which serve as sources for the pulses, and the timing diagram of figure 2-7 indicates the sequence of pulse generation and the relative durations of the respective pulses.

b. The overall system operation is under the initial control of a 60-Hz master clock. This clock serves three functions: (1) it triggers the generation of ultrasonic pulses and the subsequent signal processes in the ultrasonic receiver components; (2) it provides a gating interval within which the other pulses are generated; and (3) it determines the timing separation between successive groups of pulses.

c. The system clock pulses are applied to the first of a group of monostable multivibrators (figure 2-6). The first multivibrator provides a triggering signal which synchronizes an external monitoring oscilloscope with the system clock. An additional output triggers the second multivibrator to provide 25-kHz main

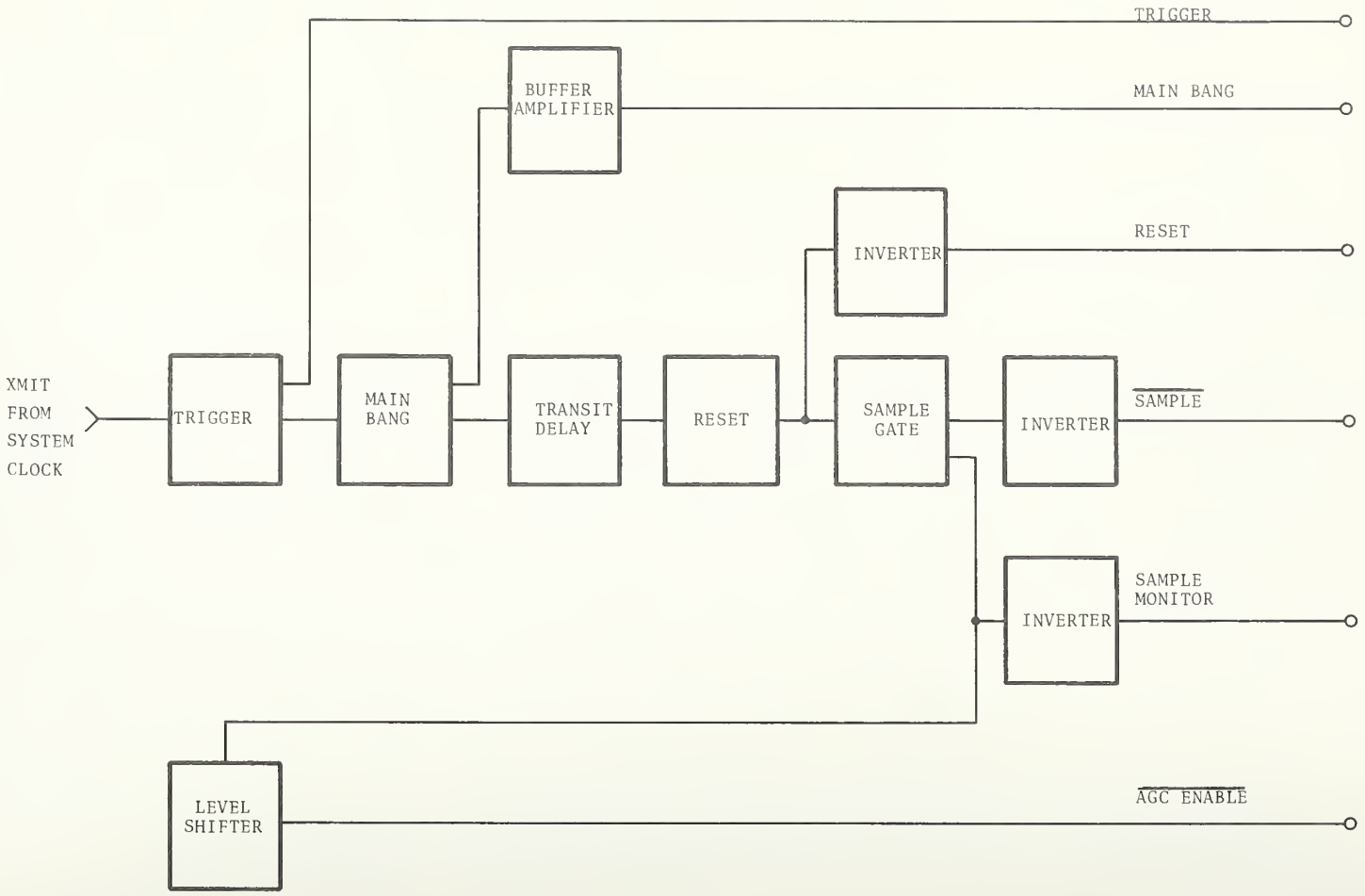


Figure 2-6. Timing Logic Board, Block Diagram

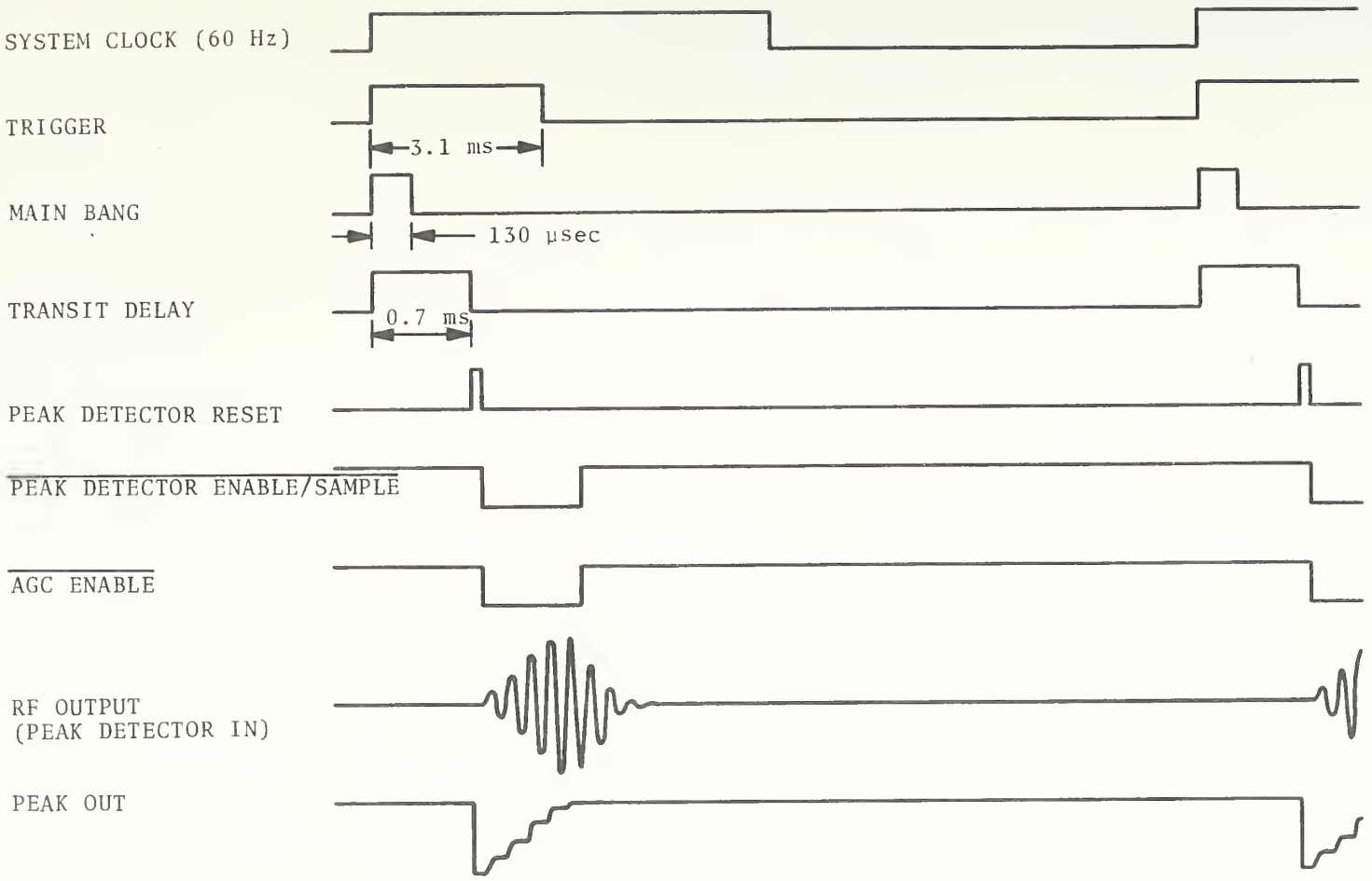


Figure 2-7. Timing Diagram for Air Ultrasonic Receiver Waveforms

bang output pulses. The main bang output is applied to a voltage amplifier circuit, referred to in this text as the transmitter, which provides amplified 25-kHz excitation to the transmitter transducer. The transmitter transducer, by its piezoelectric characteristic, causes ultrasonic energy to propagate through the tire casing to the air-coupled receiver transducers.

d. The transit delay circuit is used to maintain receiver operation inactive until the main bang excitation has been completed. This is done to avoid the possibility of noise interference from the main bang transmission.

e. The reset and sample gate pulses serve the functions described with respect to obtaining dc output levels at the peak detector of the agc amplifier board (see paragraphs 2.3.2d and e). The sample signal can be monitored by use of the inverter at the output of the sample gate block.

f. Operation of the agc amplifier (paragraph 2.3.2a) is based on the application of an enabling voltage of proper polarity and magnitude with respect to the original signal input to the agc amplifier. This enabling voltage is obtained from a level shifter circuit on the timing logic board.

2.4 CIRCUIT ANALYSIS

The discussion in this section relates the actual circuits used in the system with the block diagrams of figures 2-3 through 2-6. Correspondence of portions of the circuit diagram with particular functional blocks is noted.

2.4.1 Transmitter (Figure 2-8)

The circuit referred to as the transmitter is a voltage amplifier which provides a high voltage to the transmitter transducer, to which it connects. Its TRIG input is excited by a main bang (25-kHz) signal from the timing logic board. The transmitter is located on a separate chassis (see Section 6), and is powered by its own power supply, as shown in figure 2-8.

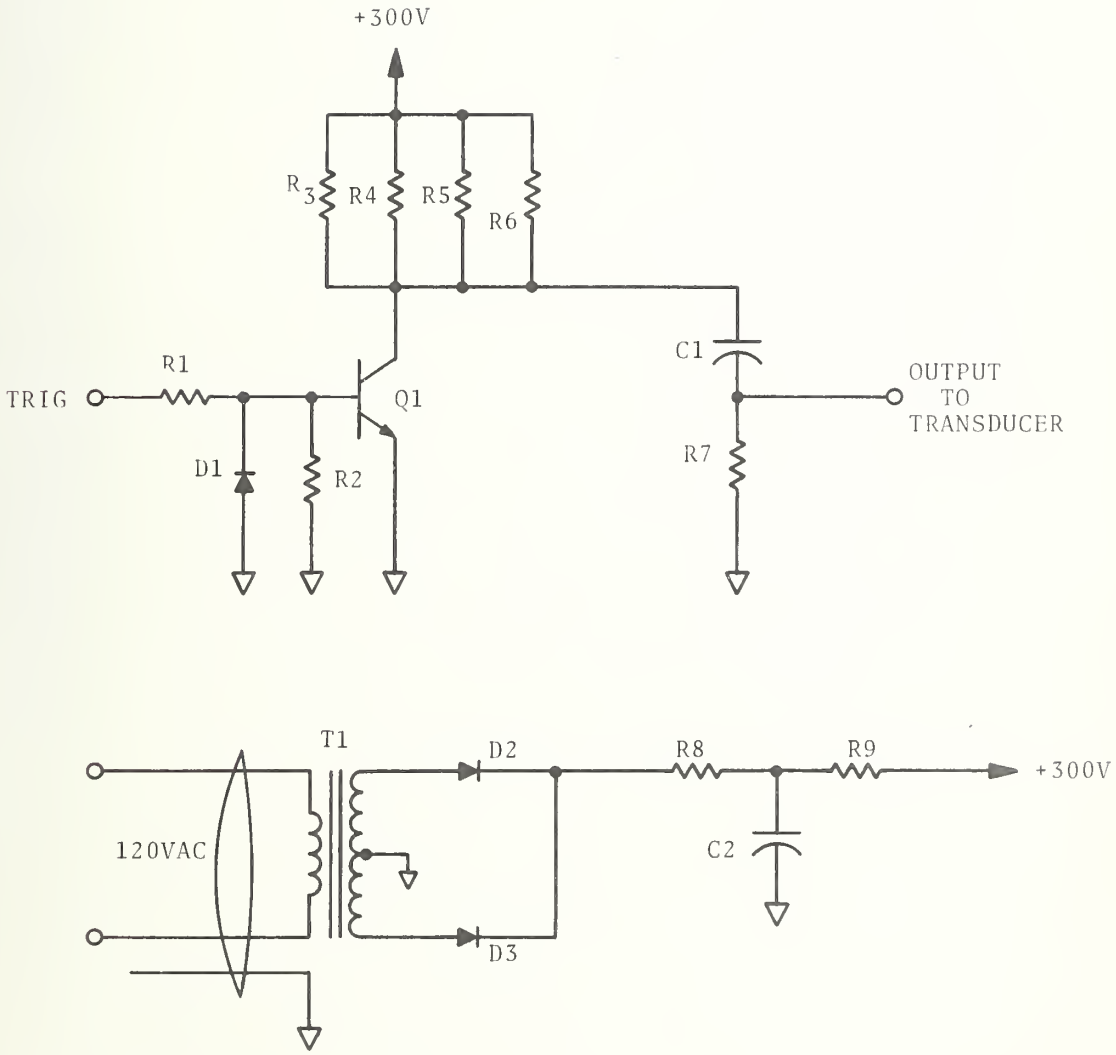


Figure 2-8. Transmitter, Schematic Diagram

2.4.2 Agc Amplifier Board (Figure 2-9)

a. The circuit shown in figure 2-9 is actually one of twelve such circuits used in the system; i.e., one for each of the twelve receiver transducer channels. The twelve circuits are contained on three printed circuit boards (see figure 6-4 for a typical board), each of which houses four of these identical circuits. The block diagram of figure 2-4 also applies to one such circuit, and the functional block designations also correspond to the designations referred to in the discussion of the circuit.

b. The signal from one of the receiver transducers is applied to the input of the agc amplifier board, and amplified and limited by the preamplifier/clipper IC1A and diodes D1, D2, D3, and D4. The signal is then applied to the agc amplifier IC2, which provides a controlled gain, upward or downward, such that the resulting amplitudes at feedback pin connection IC2-10 and input connection IC2-6 are equal. The output of the agc amplifier at pin IC2-7 is passed on to buffer amplifier IC3A, whose output is applied both to the peak detector circuit and the feedback connection IC2-10. The agc action is made operative on application from the timing logic board of the AGC ENABLE (actually its complement) signal to the input pin IC2-5. The duration and instant of application of this pulse coincide with those of the $\overline{\text{SAMPLE}}$ gate signal, which is discussed in paragraph d below.

c. The output at pin IC2-7 may have noise components in addition to the desired 25-kHz signal. Bypassing of these components to ground is achieved by use of a parallel-resonant filter network L1-C6. This network, resonant at 25 kHz, presents high impedance to the desired 25-kHz signal, and permits it to continue its signal path. For noise interference frequencies far removed from the resonant frequency the network impedance is low, and the interference is bypassed to ground through the network.

d. The peak detector accepts an ac signal at the non-inverting input of IC4, and converts it to a dc signal equal to the peak of the ac input. This dc signal is passed on to an output buffer amplifier, and from there to the analog multiplexer input of the

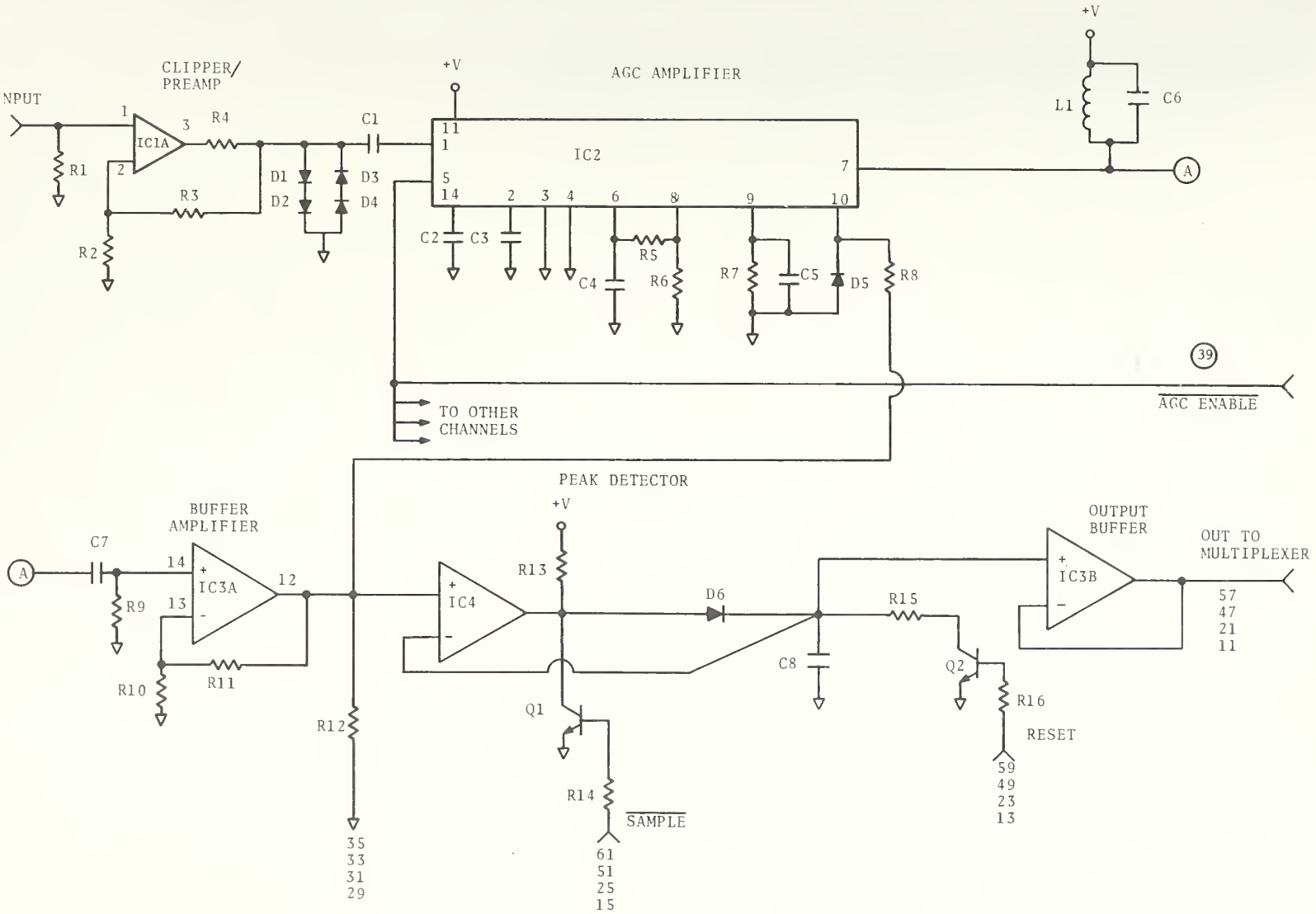


Figure 2-9. Agc Amplifier Board, Schematic Diagram

display driver. The peak detector functions to permit successive independent dc voltage levels to appear at its output. These voltage levels vary in accordance with the transducer channel outputs, which, in turn, are related to the tire separation in the test tire. Therefore, the peak detector output provides one voltage level as the result of one input pulse, and is ready to provide a different voltage level on the next input pulse. In the following discussion, reference is made also to the timing diagram of figure 2-7.

(1) The ac input to the peak detector is amplified by IC4 and applied to diode D6, where it is rectified to a positive voltage. This voltage is applied to capacitor C8, where it builds up to the peak of the ac input to D6. (The voltage buildup is indicated in the PEAK OUT waveform of figure 2-7.) The peak voltage on C8, after passing through the output buffer IC3B, is applied to one of the twelve input lines to the analog multiplexer of the display driver.

(2) The peak voltage across C8 is built up during the period when the AGC ENABLE signal is applied. Although the AGC ENABLE gate is removed after a short interval, the capacitor tends to retain its voltage. If this voltage is retained by the capacitor into the next application of the AGC ENABLE gate, the retained capacitor voltage will prevent a true reflection of the peak ac value of the next input pulse. Therefore, when the AGC ENABLE gate is removed, the capacitor voltage must also be removed. This is done by application of a RESET pulse to transistor Q2 (figure 2-9) through resistors R15 and R16. As noted in the timing diagram (figure 2-7), the RESET pulse is applied on the trailing edge of the TRANSIT DELAY pulse, at which time the receiver becomes enabled. As soon as the RESET pulse is applied, capacitor C8 becomes discharged, and is now ready to build up a new charge based on the magnitude of the new input pulse. This discharge is effected by applying the positive RESET voltage to the base of Q2 (figure 2-9), thus forward-biasing it, and creating an effective short from collector to ground. The capacitor is therefore shorted through R15 and Q2 to ground, and the capacitor C8 becomes discharged.

(3) The action described in paragraph (2) is very rapid, and the RESET pulse is quickly removed. On the trailing edge of the RESET pulse, the AGC ENABLE gate is again introduced, and an additional gate, known as the SAMPLE gate, is applied at the same instant to the base of transistor Q1 through resistor R14. Prior to application of the SAMPLE gate, the transistor Q1 is forward-biased by the positive SAMPLE voltage, and Q1 is therefore effectively shorted from collector to ground. This short also shorts the output of IC4 to ground. Thus, there is no input to D6, and hence no peak dc voltage to apply to the analog multiplexer of the display driver. However, when the AGC ENABLE period again arrives, the SAMPLE voltage is simultaneously removed (i.e., the SAMPLE gate is applied). With forward bias removed, Q1 stops conducting; the short is removed from the input to D6; capacitor C8 again builds up to a new peak dc voltage; and a new voltage is applied to an input line at the analog multiplexer.

(4) The RESET and SAMPLE pulses, when applied to the circuits indicated in figure 2-9 and in accordance with the timing of figure 2-7, ensure that the twelve inputs to the analog multiplexer will receive successive voltage levels which reflect correctly the degree of tire separation for each successive input pulse from the transducer channels.

2.4.3 Display Driver (Figure 2-10)

a. The outputs from the twelve peak detector circuits of the three agc amplifier boards (four circuits to each board) are applied as inputs to analog multiplexer IC1 of the display driver. This circuit processes the multiple inputs so that they appear serially on a single-output line from the multiplexer. The outputs from the single line are applied to potentiometer R17, which also serves as signal gain control. This signal is then applied to one input of summing amplifier IC2A. The same input connection to the summing amplifier receives a signal from the digital-to-analog converter, consisting of inverters IC4A, IC4B, IC4C, IC4D, diodes D1 through D4, R2 through R5, and R19. The digital-to-analog converter operates in such a manner as to provide twelve distinct

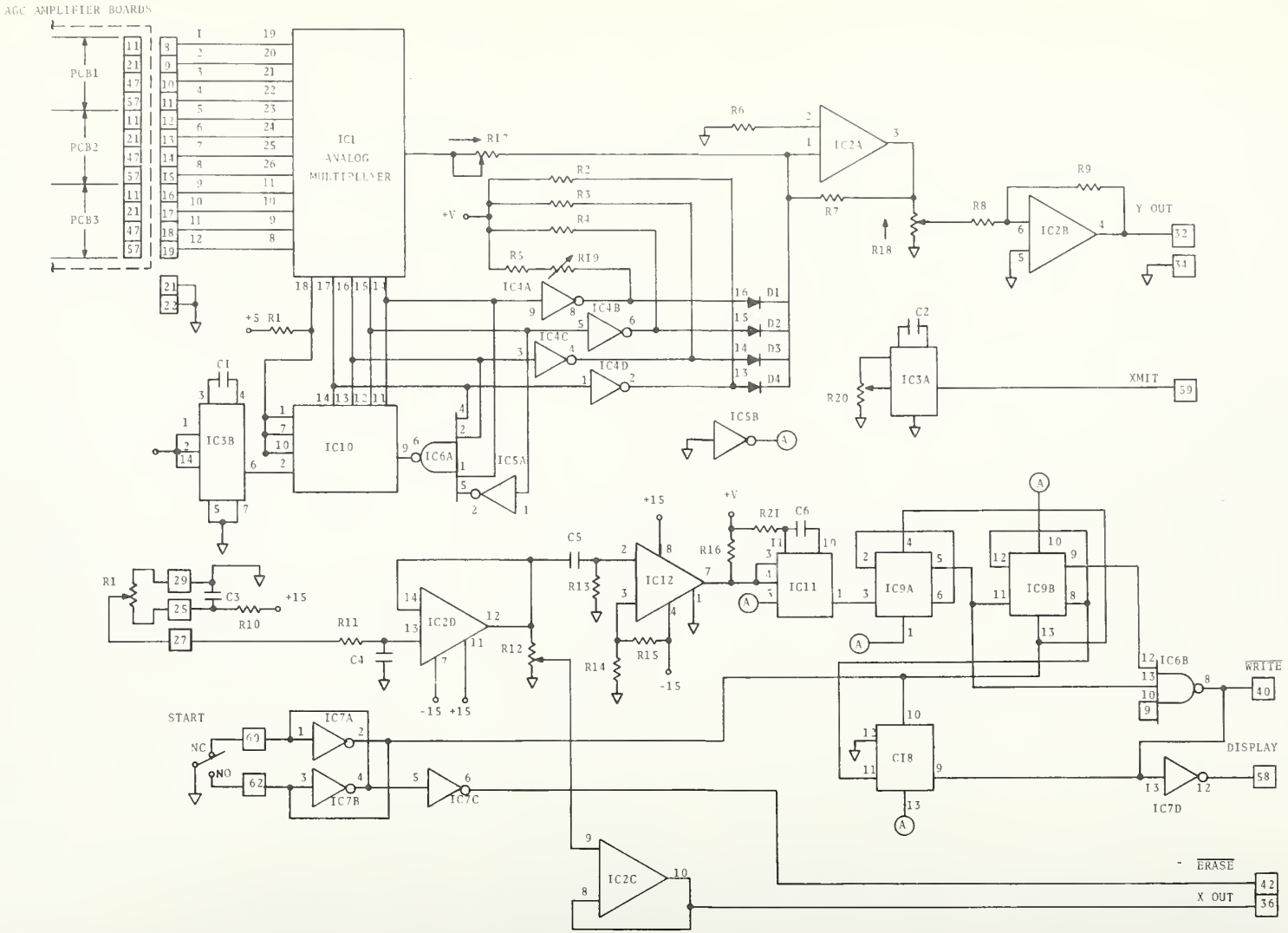


Figure 2-10. Display Driver, Schematic Diagram

voltage levels at the input to the summing amplifier. The combination of inputs to summing amplifier IC2A determines the lines which are shown on the storage scope display, together with the modulating signals from the peak detector outputs. Figure 2-11 shows a typical 12-line display, with variations in the respective line levels indicating the degree of separation within a tire.

b. The basic description for the display driver operation is given in paragraphs a through h of subsection 2.3.3. The following comments complement the description with consideration of correspondence between figures 2-5 and 2-10.

c. The address logic consists of a high-frequency clock IC3B (figure 2-10) and counter IC10. The counter output signals drive a feedback loop which resets the counter after a binary count (1011) equivalent to decimal 11. The four output signals from the counter represent binary numbers from 0000 (decimal zero) to 1011 (decimal eleven), with terminal IC10-11 representing the most significant bit and terminal IC10-14 the least significant bit. The feedback loop consists of inverter IC5A and NAND gate IC6A. The NAND gate output goes low (and initiates counter reset) only when all the inputs to the NAND gate are high. This condition is satisfied by converting the zero bit at terminal IC10-12 to a 1-bit; i.e., by applying inverter IC5A between IC10-12 and pin 5 of IC6A. The binary count 1011 now causes all inputs to IC6A to be high, and its output to go low. Thus, the reset is accomplished, and the counter repeats the cycle with the clock from IC3B.

d. The same signals connect to inverters IC4A through IC4D of the digital-to-analog converter. Depending on whether the counter outputs are high or low, diodes D1 through D4 are correspondingly nonconducting or conducting. Therefore, different combinations of R2, R3, R4, and the series pair R5 and R19 are connected in parallel to input to summing amplifier IC2A. This input, together with the signal from the multiplexer, provides the output at IC2A and, through buffer amplifier IC2B, to the vertical input of the storage scope display (Y OUT in figure 2-10).

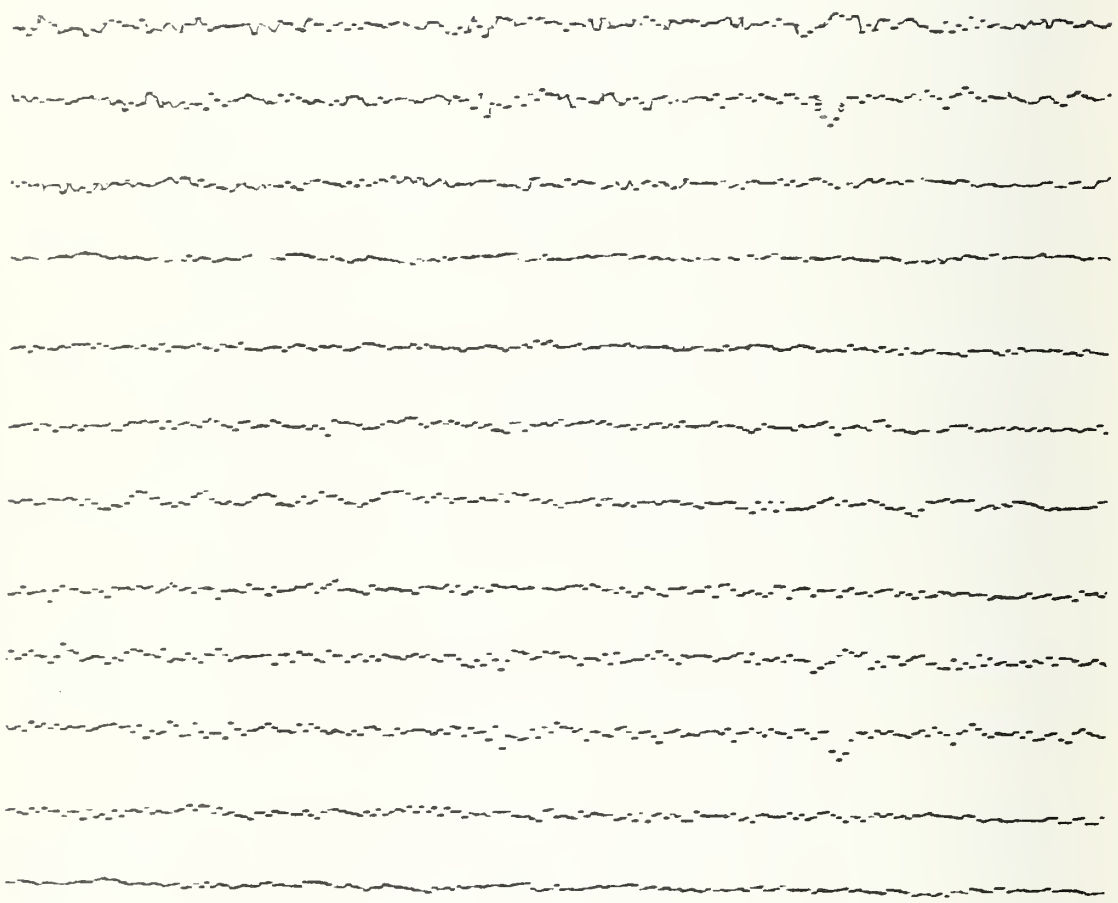


Figure 2-11. Typical Display

e. In the derivation of the horizontal trace for the storage scope, the ramp voltage is obtained from the rotation of potentiometer R1 of the tire assembly on the main test equipment (R1 of figure 2-10). The basic discussion of paragraph 2.3.3e applies here also for obtaining the horizontal trace (X OUT).

f. In the circuit for obtaining the $\overline{\text{WRITE}}$ signal, C5-R13, and the grouping of IC12, IC9A, and IC9B of figure 2-10 correspond to the previously discussed C1-R10, COMPARATOR, and ROTATION COUNTER of figure 2-5.

2.4.4 Timing Logic Circuit (Figure 2-12)

The timing signals are initiated by applying the master 60-Hz clock to IC1, the first of a group of one-shot (monostable) multivibrators (IC1, IC2A, IC2B, IC3A, and IC3B). In addition to the RESET, $\overline{\text{SAMPLE}}$, MB, $\overline{\text{AGC ENABLE}}$, and SAMPLE MONITOR signals previously referred to (see paragraphs 2.3.2d and e, 2.3.4e, and 2.4.1), the timing logic board also provides a TRIGGER signal for use in a test oscilloscope. The basic description of the circuit closely parallels the description furnished in paragraphs 2.3.4a through f. The level shifting circuit mentioned in paragraph 2.3.4f with respect to obtaining an $\overline{\text{AGC ENABLE}}$ signal consists of the transistor circuits Q1 and Q2 in figure 2-12.

2.4.5 Monitor Channel Select Circuit (Figure 2-13)

This circuit contains a twelve-contact switch (S1) which picks off any one of the twelve output signals from the peak detector circuit of the agc amplifier board. The switch is followed by buffer amplifier IC1, and its output is fed to a test oscilloscope for monitoring any of the twelve transducer channel signals.

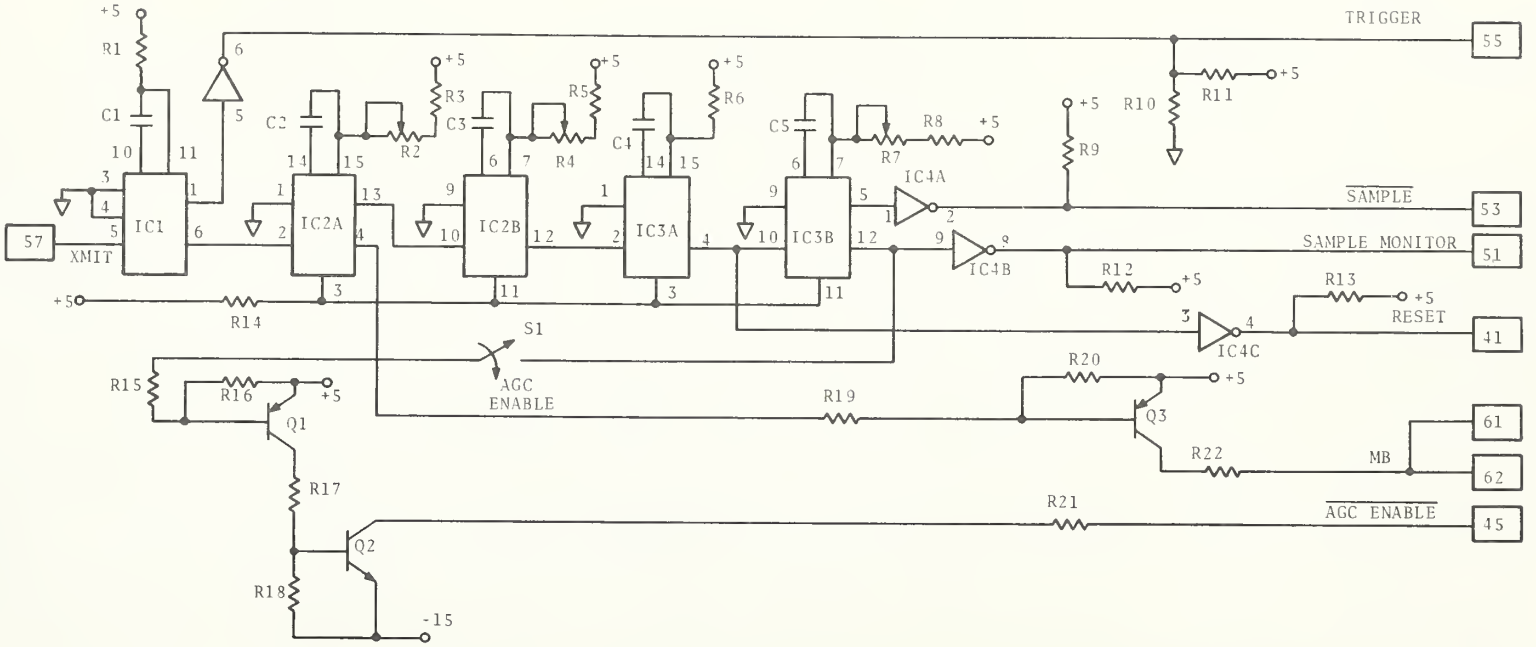


Figure 2-12. Timing Board, Schematic Diagram

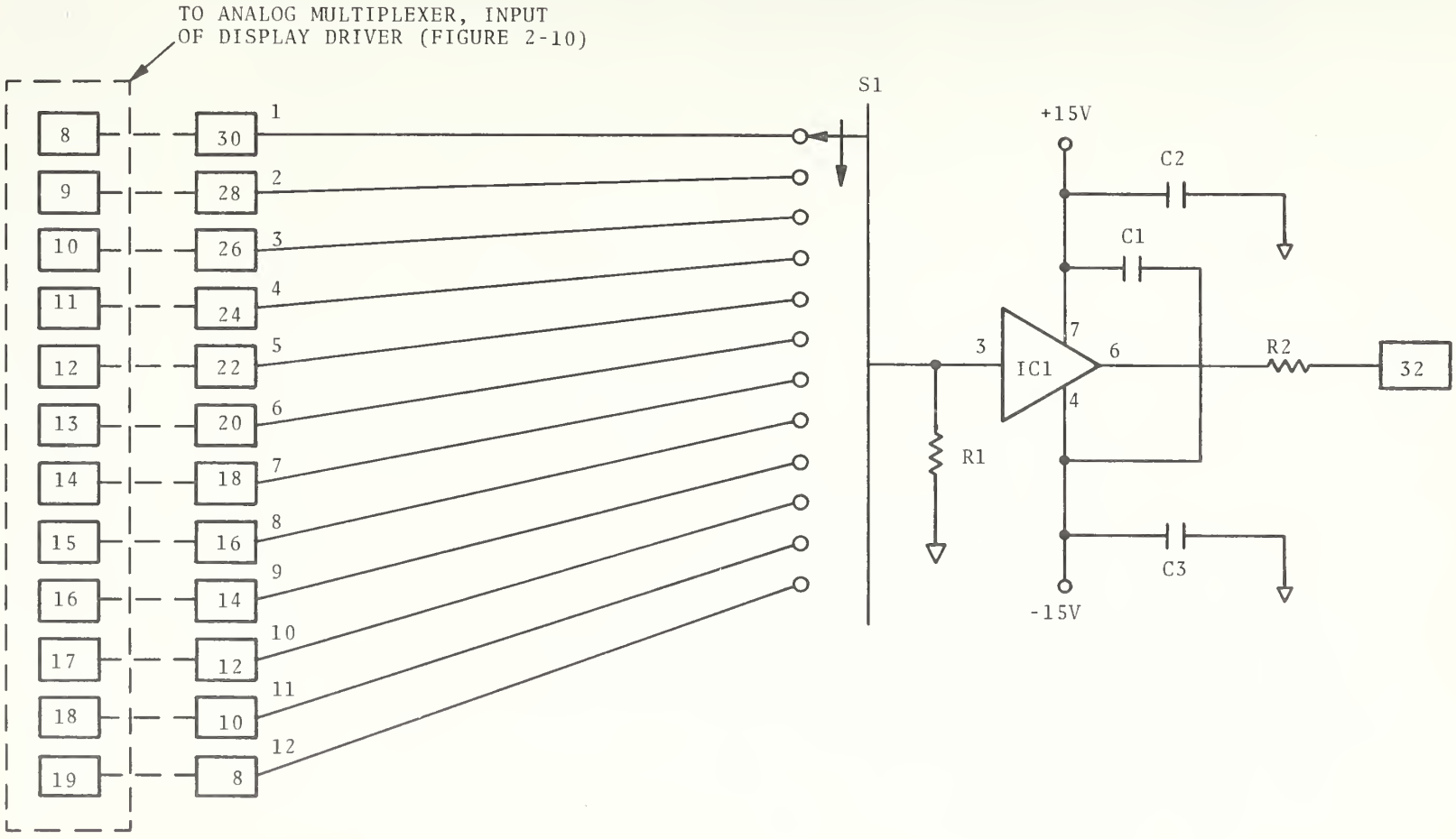


Figure 2-13. Monitor Channel Select Circuit

3. INSTALLATION

3.1 INSTALLATION REQUIREMENTS

There are relatively few constraints with respect to installation of the test equipment. Two basic needs merit consideration, as noted below.

3.1.1 Siting

The test equipment is to be installed in a level, free-access area capable of supporting a weight of 100 pounds per square foot.

3.1.2 Noise Avoidance

a. The test equipment is to be installed in a relatively noise-free environment. In particular, it is important to maintain distance from noise of escaping pressurized air (hiss) type. A general rule, which is subject to modification by the individual user, is that an air hiss within 15 feet of the operating tire inspection system is to muffled.

b. The equipment itself should be soundproofed in noise-sensitive areas. Specifically, the receiver transducers can be enclosed in a metal box filled with fiberglass for protection against undesired noise as well as equipment mechanical vibrations. In addition, the rims which support the tire casing can also have fiberglass board (Owens Corning Fiberglas Panel Type 704 or equivalent) attached to their inner flat surfaces. This feature adds to the acoustic noise suppression capability of the equipment. (The NHTSA/TSC prototype has applied these features to its equipment with noticeable improvement over the previous susceptibility to noise.)

3.2 SAFETY PRECAUTIONS

There are no safety precautions necessary for potential mechanical mishaps other than ordinary care in the presence of heavy equipment. From an electrical standpoint, it is extremely

important to exercise caution when connecting and disconnecting power supplies, and when working on backplane pins carrying power busses.

3.3 INTERCONNECTION DIAGRAM

Figure 3-1 provides an interconnection diagram which permits connections between the terminals of the respective boards.

3.4 INITIAL ADJUSTMENTS

The adjustments consist primarily of turning on the main power switch for the electronics (figure 3-2), the on/off switch for the drive motor, and the speed control on the RATIOPAX I panel.

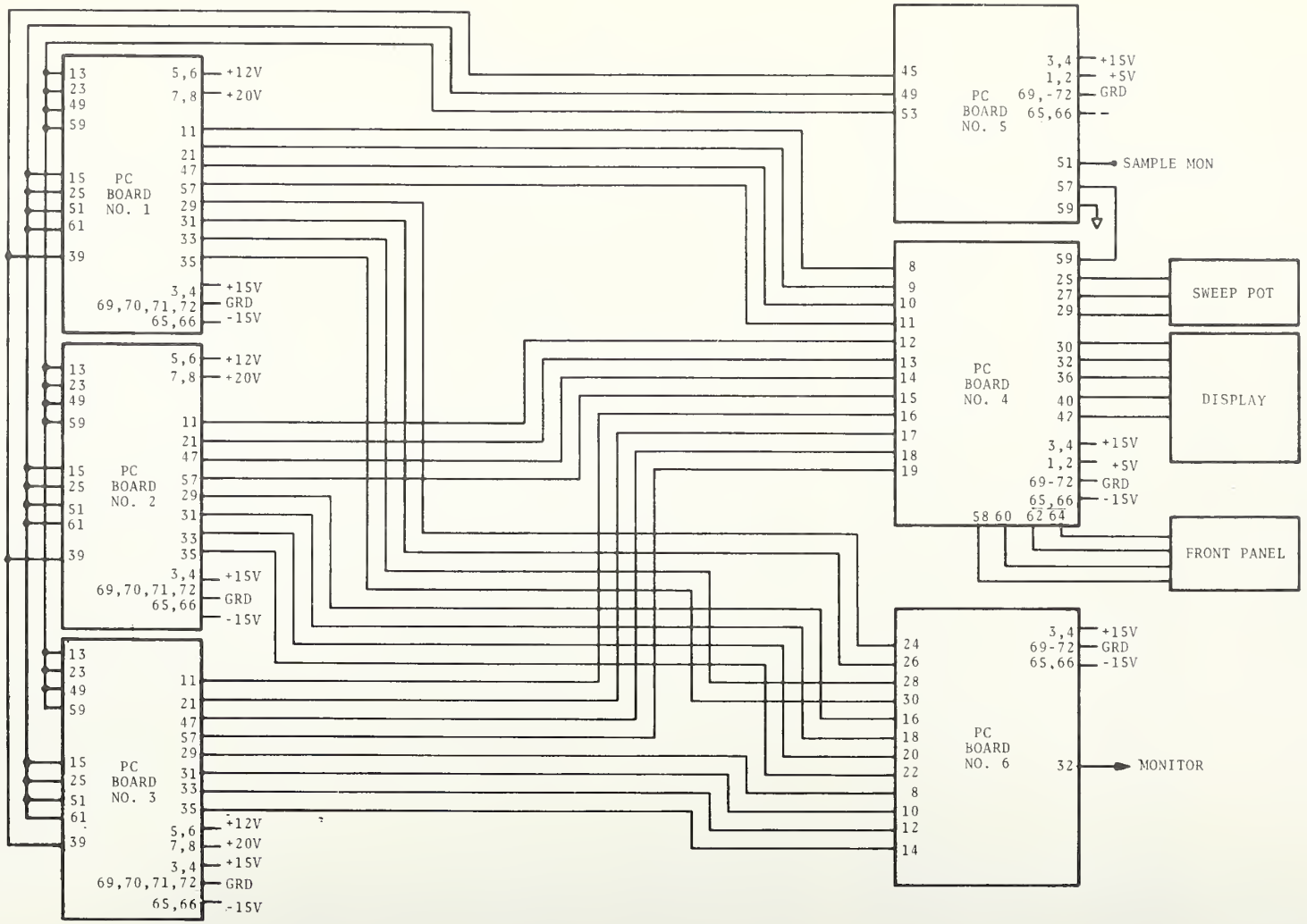


Figure 3-1. Interconnection Diagram

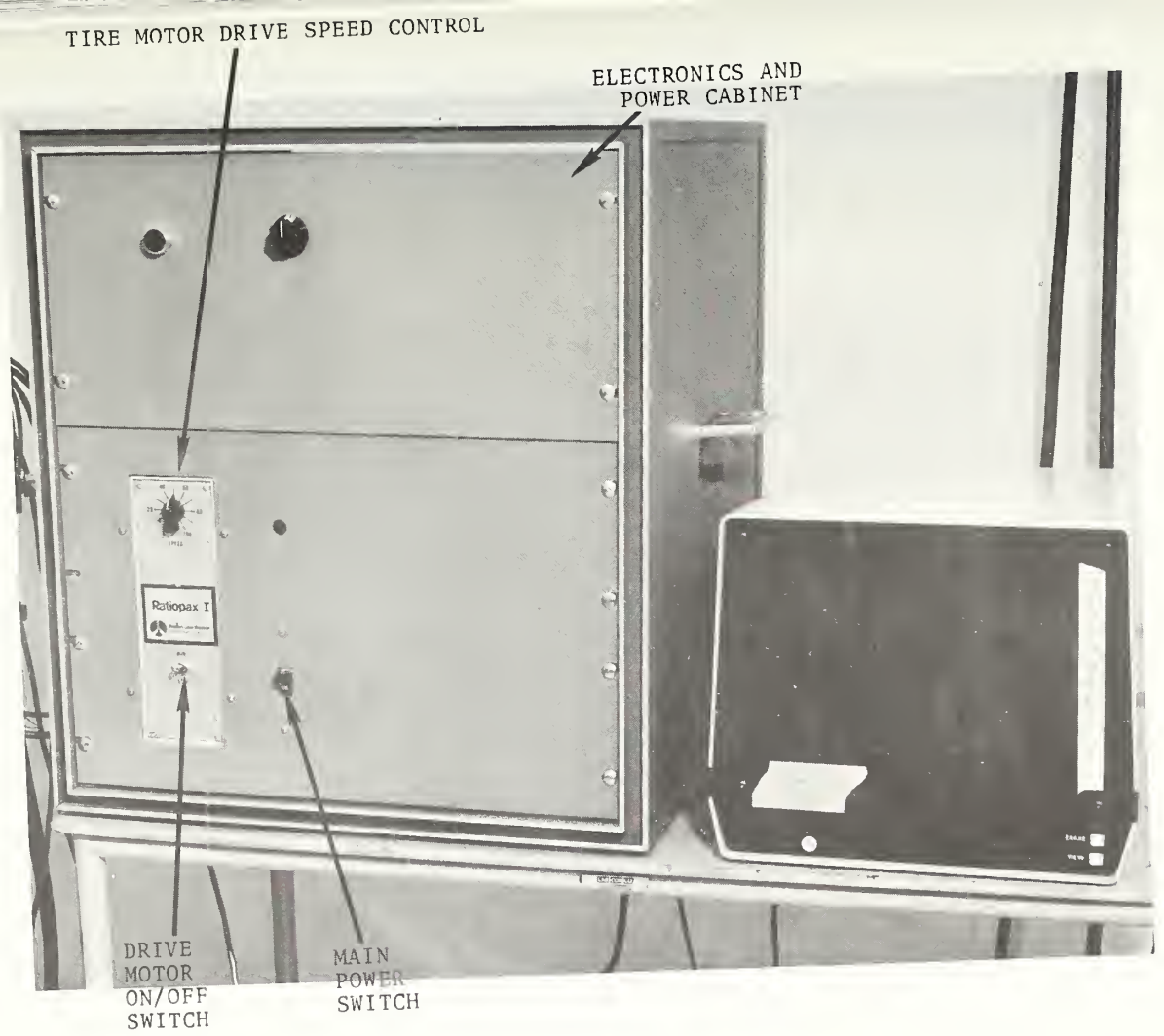


Figure 3-2. Controls for Initial Adjustments

4. OPERATION

Operation of the equipment requires minimal operator action beyond the adjustments of paragraph 3.4. Once the equipment has been turned on and the rotational speed has been determined, nominally 15 rpm, it is only necessary to press the START push-button (figure 4-1) for the twelve channel signals with the associated modulation to be displayed on the storage scope. The only other available control is the twelve-contact channel selector switch (actually a part of PCB6), which will permit analysis of individual traces.

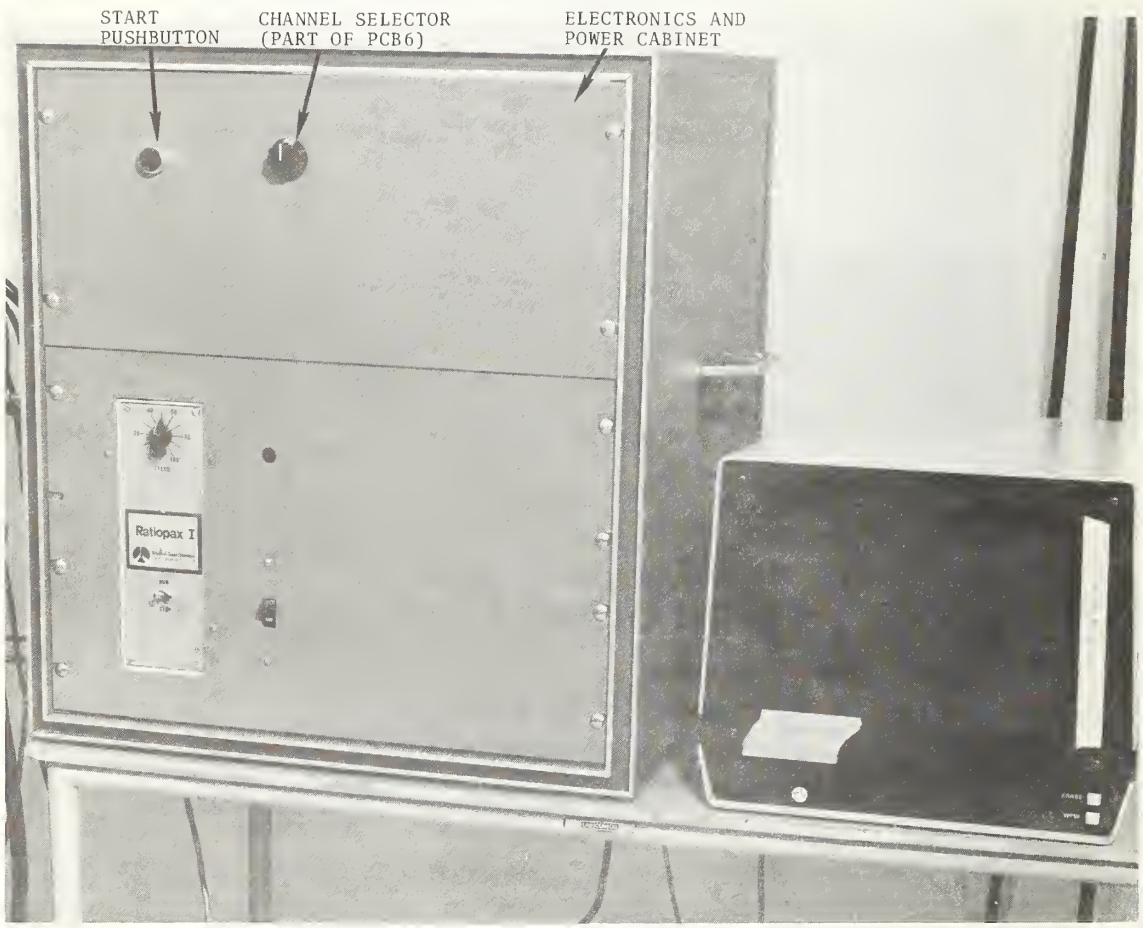


Figure 4-1. Operating Controls

5. MAINTENANCE

5.1 PREVENTIVE MAINTENANCE

Because of the makeup of the prototype testing equipment, only a minimum of preventive maintenance is required. A periodic oiling of the test equipment drive motor and gearing and inspection of the component parts form the basic preventive maintenance procedure. For any auxiliary equipment used with the prototype, maintenance instructions will be followed as directed in its related instruction manual.

5.2 TROUBLESHOOTING

Troubleshooting the test equipment demands minimal analysis of both mechanical and electrical features of the equipment. The equipment structure is mechanically rugged, so that there is small likelihood of mechanical failure. Securing the tire between the rims is routine, as are application of air pressure to the tire and control of tire rotational speed with motor drive speed control. Failures related to these functions are easily detectable; the remedies are straightforward, and need no elaboration.

Troubleshooting the printed circuit boards is also of a limited nature at the operating site. If a fault is traced to a particular circuit board, that board is replaced by a spare board known to be in good working condition. The faulty board is shipped to the manufacturer for repair, including alignment. This procedure provides immediate remedy to the current problem, and also makes certain that the repaired board will have been restored to its original specification capabilities.

A typical problem arises when an equipment operator observes an erratic indication on the storage scope display. The significance of its characterization as erratic is evident in figure 5-1, which indicates simultaneous noise spikes on several channels; e.g., channels 1 through 4 and 6 through 9. (Contrast this presentation with that of figure 2-11, where every line shows different characteristics from the lines above and below it.)

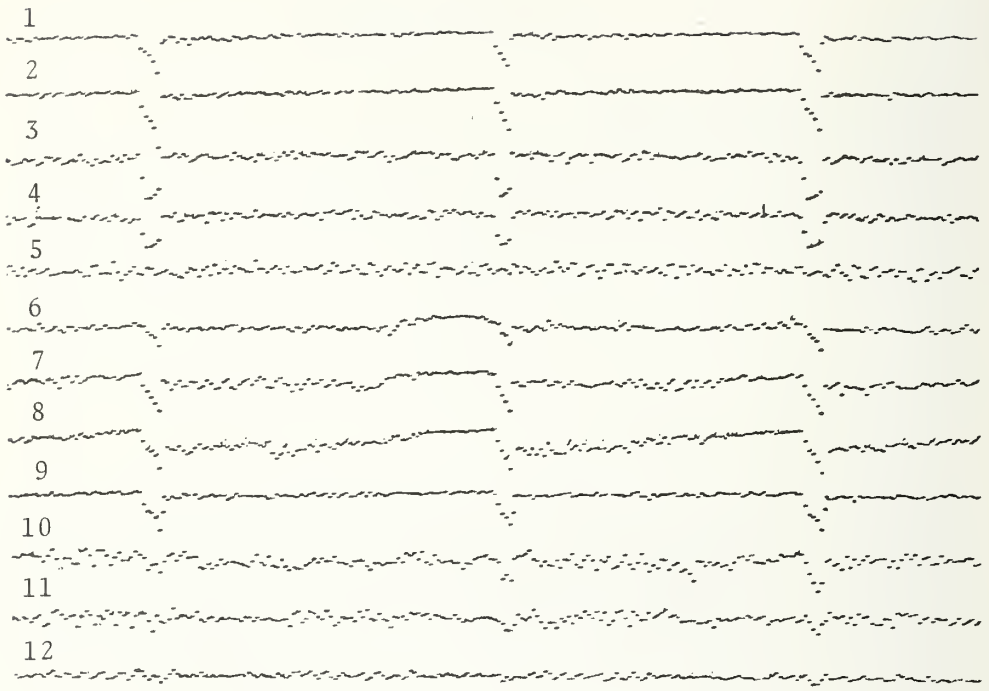


Figure 5-1. Sample of Erratic Signal Output

The basis for this display is that insufficient sound is getting through the tire. Therefore, to ensure that sufficient sound does get through the tire, reposition the receiver transducers so that a receiver transducer is oriented over each groove in the tread. This change in transducer orientation will make possible the inspection of tires with heavy tread sections.

5.3 DIAGRAMS AND PHOTOGRAPHS

The circuit diagrams for the printed circuit boards and transmitter are contained as part of the circuit analysis discussion in subsection 2.4, and the board and transmitter photographs with component callouts are located in Section 6, in connection with the parts listing.

6. PARTS LIST

This section provides a tabular listing of the component parts of various circuit boards, frames, and chassis. Tables 6-1 through 6-10 list the reference designations of the parts, their values, and the figure numbers of the photographs on which the called-out parts are located. Where applicable, associated schematic diagrams are also referenced. For convenience, the related photographs are positioned adjacent to the groups of parts listed for those photographs. The tables also include the names of the manufacturers of parts which have special characteristics. Replacement with parts fabricated by other manufacturers is permissible if the replacement parts have characteristics identical to the characteristics of the replaced parts.

(Note: In the listing, resistors, unless otherwise noted, are rated at 1/4 watt and ± 5% tolerance.)

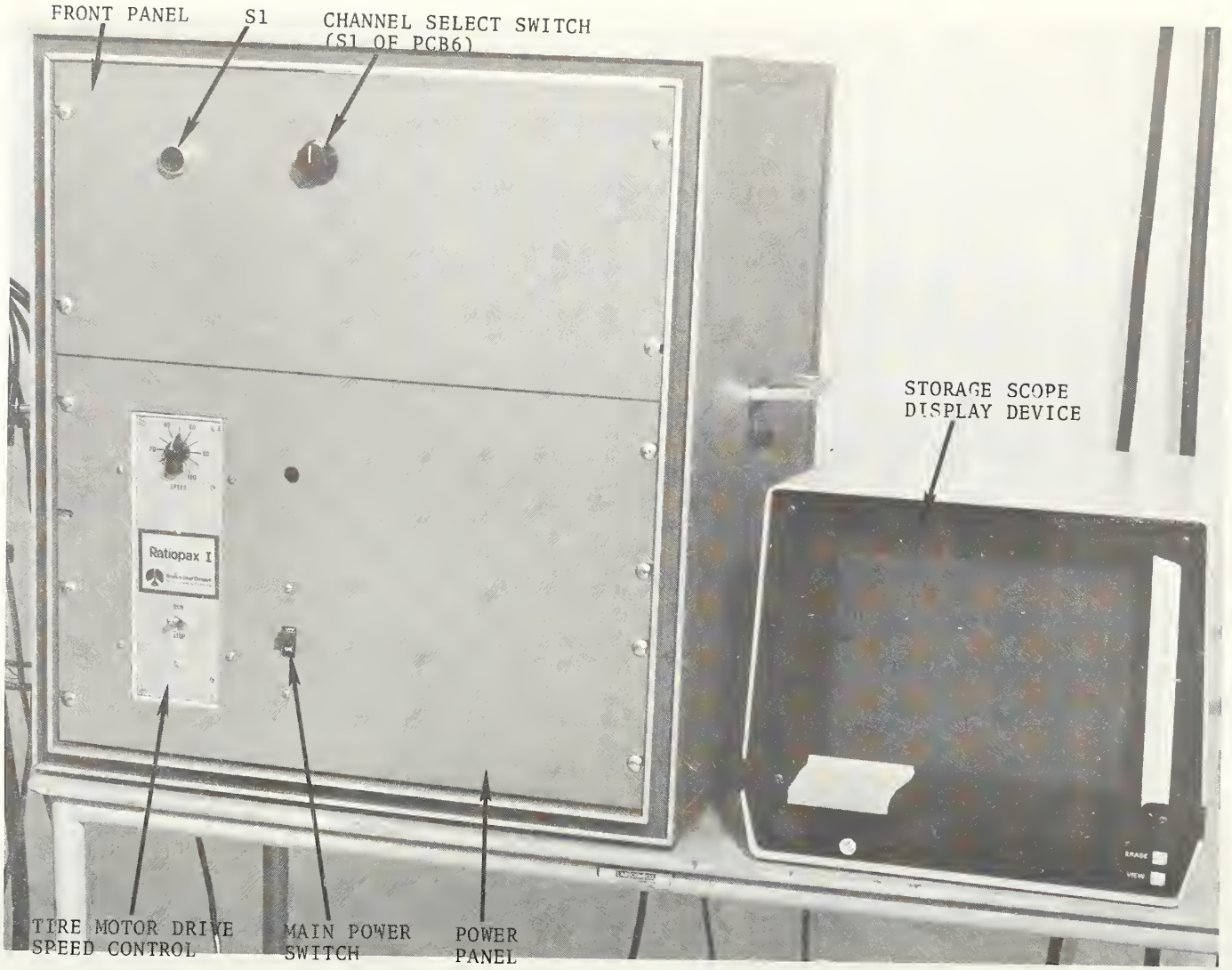


Figure 6-1. Front Panel, Parts Location

TABLE 6-1. PARTS LIST - FRONT PANEL*

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
S1	START switch (DPST)		
MAIN POWER	Equipment turn-on		
	switch, SPST		
TIRE MOTOR		Boston Gear Division,	RATIOPAX I
DRIVE SPEED		North American	
CONTROL		Rockwell	
CHANNEL SELECT	Switch, single-pole,		
SWITCH	12-position (S1 of PCB6)		

*Schematic Diagram – Figures 2-10, 2-13.

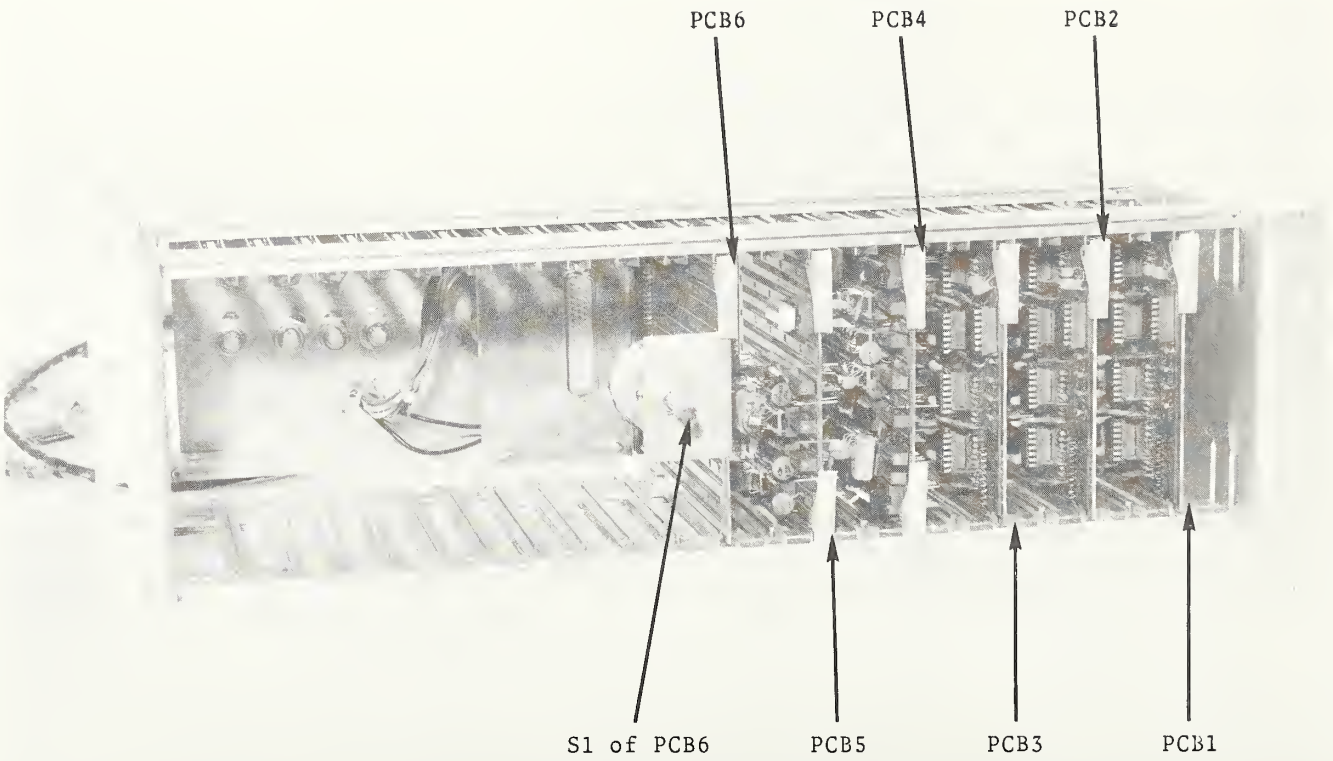


Figure 6-2. Main Frame, Parts Location

TABLE 6-2. PARTS LIST - MAIN FRAME

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
PCB 1	AGC Amplifier Board (Fig. 6-4)	Teknekron	
PCB 2	AGC Amplifier Board (Fig. 6-4)	Teknekron	
PCB 3	ACG Amplifier Board (Fig. 6-4)	Teknekron	
PCB 4	Display Driver - Figure 6-5	Teknekron	
PCB 5	Timing Board - Figure 6-6	Teknekron	
PCB 6	Monitor Channel Select - Figure 6-7	Teknekron	

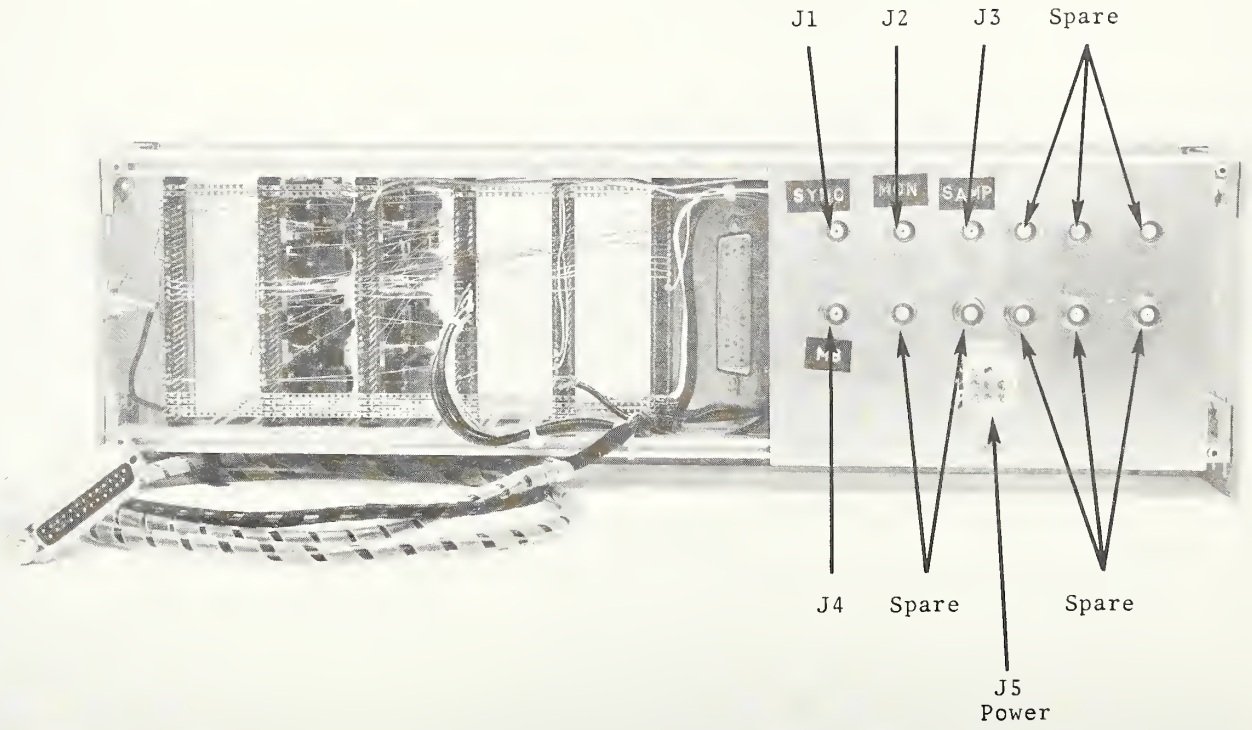


Figure 6-3. Rear Panel, Parts Location

TABLE 6-3. PARTS LIST - REAR PANEL

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
J1	Connector, Sync, BNC		
J2	Connector, Monitor, BNC		
J3	Connector, Sample, BNC		
J4	Connector, Main Bang, BNC		
J5	Connector, Power, BNC		

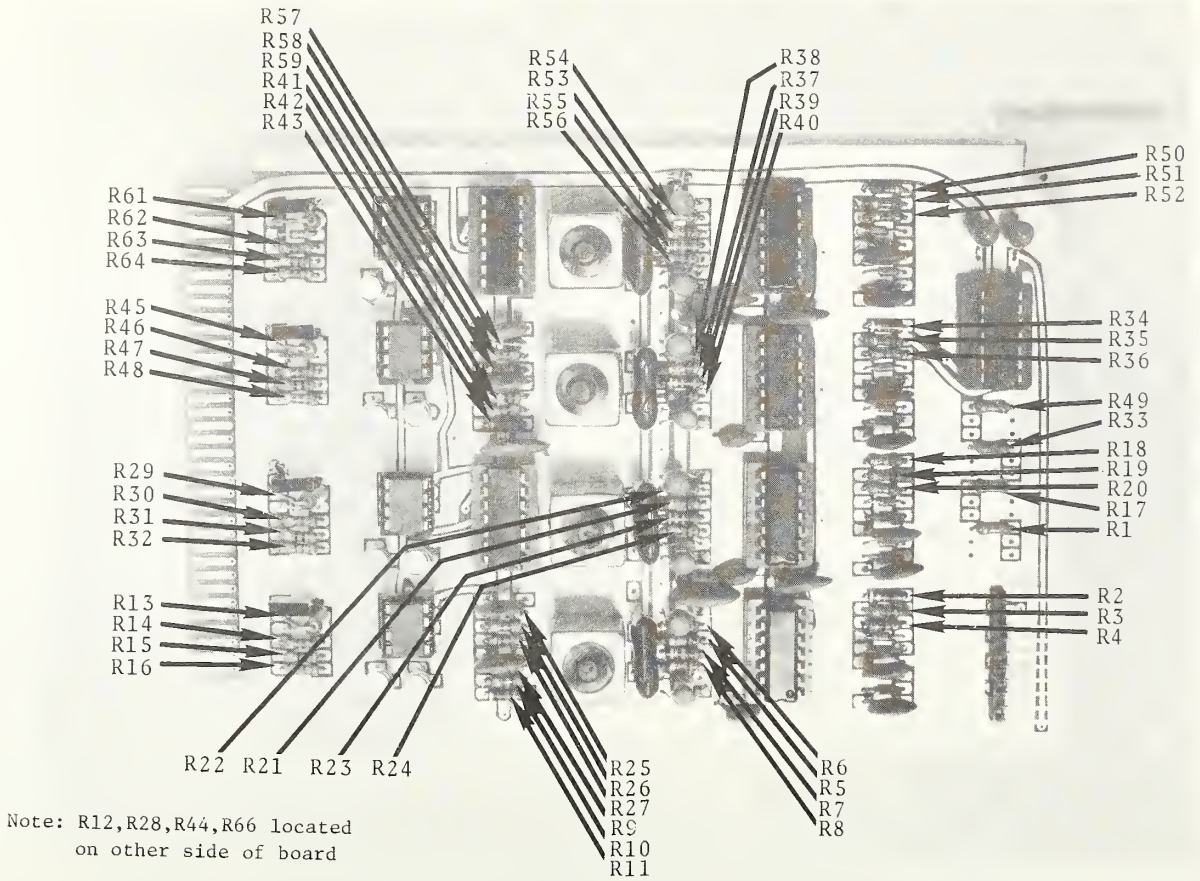


Figure 6-4a. Agc Amplifier Board (PCB 1,2,3), Parts Location (Resistors)

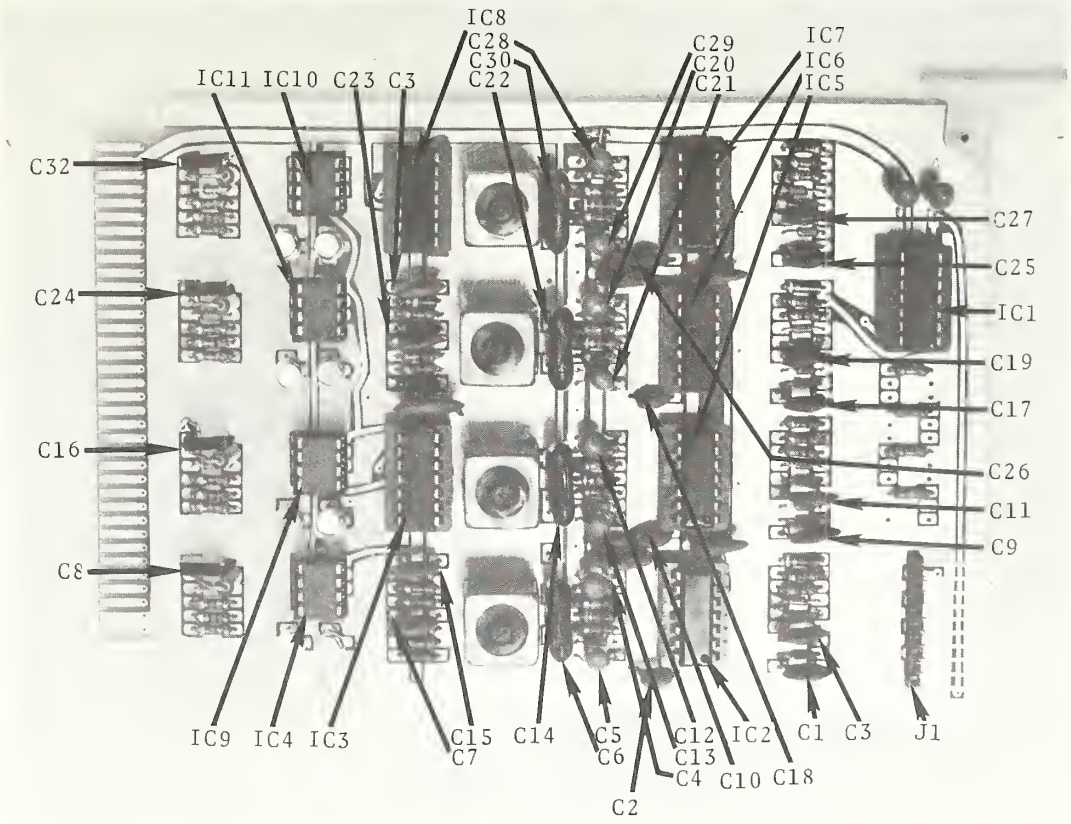


Figure 6-4b. Agc Amplifier Board (PCB 1,2,3), Parts Location (Capacitors, Integrated Circuits)

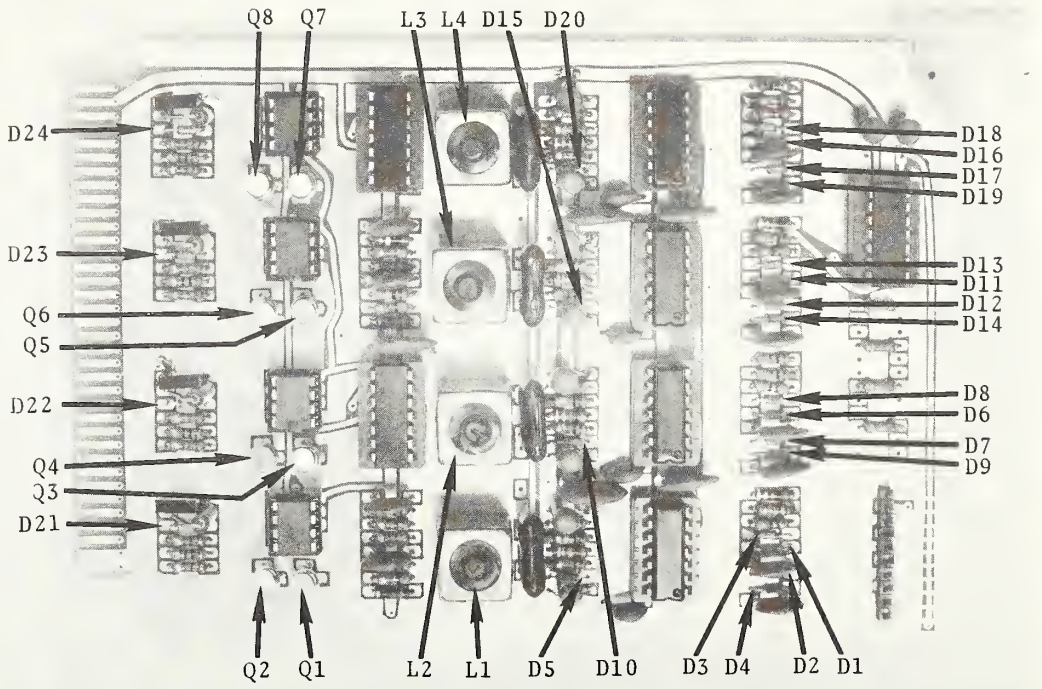


Figure 6-4c. Agc Amplifier Board (PCB 1,2,3), Parts Location (Diodes, Filters, Transistors)

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)*

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R1	Resistor, 27K ohms		
R2	Resistor, 100 ohms		
R3	Resistor, 1K ohms		
R4	Resistor, 51 ohms		
R5	Resistor, 10K ohms		
R6	Resistor, 1.5K ohms		
R7	Resistor, 10M ohms		
R8	Resistor, 1K ohms		
R9	Resistor, 100K ohms		
R10	Resistor, 5.1K ohms		
R11	Resistor, 5.1K ohms		
R12	Resistor, 4.7K ohms		
R13	Resistor, 470 ohms-1/2 watt		
R14	Resistor, 2.7K ohms		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R15	Resistor, 20 ohms		
R16	Resistor, 2.7K ohms		
R17	Resistor, 27K ohms		
R18	Resistor, 100 ohms		
R19	Resistor, 1K ohms		
R20	Resistor, 51 ohms		
R21	Resistor, 10K ohms		
R22	Resistor, 1.5K ohms		
R23	Resistor, 10M ohms		
R24	Resistor, 1K ohms		
R25	Resistor, 100K ohms		
R26	Resistor, 5.1K ohms		
R27	Resistor, 5.1K ohms		
R28	Resistor, 4.7K ohms		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R29	Resistor, 470 ohms - 1/2 watt		
R30	Resistor, 2.7K ohms		
R31	Resistor, 20 ohms		
R32	Resistor, 2.7K ohms		
R33	Resistor, 27K ohms		
R34	Resistor, 100 ohms		
R35	Resistor, 1K ohms		
R36	Resistor, 51 ohms		
R37	Resistor, 10K ohms		
R38	Resistor, 1.5K ohms		
R39	Resistor, 10M ohms		
R40	Resistor, 1K ohms		
R41	Resistor, 100K ohms		
R42	Resistor, 5.1K ohms		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R43	Resistor, 5.1K ohms		
R44	Resistor, 4.7K ohms		
R45	Resistor, 470 ohms-1/2 watt		
R46	Resistor, 2.7K ohms		
R47	Resistor, 20 ohms		
R48	Resistor, 2.7K ohms		
R49	Resistor, 27K ohms		
R50	Resistor, 100 ohms		
R51	Resistor, 1K ohms		
R52	Resistor, 51 ohms		
R53	Resistor, 10K ohms		
R54	Resistor, 1.5K ohms		
R55	Resistor, 10M ohms		
R56	Resistor, 1K ohms		

*Schematic Diagram - Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R57	Resistor, 100 K ohms		
R58	Resistor, 5.1K ohms		
R59	Resistor, 5.1K ohms		
R60	Resistor, 4.7K ohms		
R61	Resistor, 470 ohms-1/2 watt		
R62	Resistor, 2.7K ohms		
R63	Resistor, 20 ohms		
R64	Resistor, 2.7K ohms		
C1	Capacitor, 0.1µF/10V		
C2	Capacitor, 0.001µF/1KV		
C3	Capacitor, 0.1µF/10V		
C4	Capacitor, 10µF/20V		
C5	Capacitor, 2.2µF/35V		
C6	Capacitor, Mica, 0.0015µF/500V		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
C7	Capacitor, 0.1μF/10V		
C8	Capacitor, 0.22μF/50V		
C9	Capacitor, 0.1μF/10V		
C10	Capacitor, 0.001μF/1KV		
C11	Capacitor, 0.1μF/10V		
C12	Capacitor, 10μF/20V		
C13	Capacitor, 2.2μF/35V		
C14	Capacitor, Mica, 0.0015μF/500V		
C15	Capacitor, 0.1μF/10V		
C16	Capacitor, 0.22μF/50V		
C17	Capacitor, 0.1μF/10V		
C18	Capacitor, 0.001μF/1KV		
C19	Capacitor, 0.1μF/10V		
C20	Capacitor, 10μF/20V		
C21	Capacitor, 2.2μF/35V		

*Schematic Diagram – Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
C22	Capacitor, Mica ,0.0015μF/500V		
C23	Capacitor, 0.1μF/10V		
C24	Capacitor, 0.22μF/10V/ 50V		
C25	Capacitor, 0.1μF/10V		
C26	Capacitor, 0.001μF/1KV		
C27	Capacitor, 0.1μF/10V		
C28	Capacitor, 10μF/20V		
C29	Capacitor, 2.2μF/35V		
C30	Capacitor, Mica, 0.0015μF/500V		
C31	Capacitor, 0.1μF/10V		
C32	Capacitor, 0.22μF/50V		
IC1	Quad op-amp	Raytheon	4136
IC2	Agc amplifier	Motorola	MC1352
IC3	Same as IC1		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
IC4	Comparator	National	LM 311
IC5	Quad op amp	Raytheon	4136
IC6	Quad op amp	Raytheon	4136
IC7	Quad op amp	Raytheon	4136
IC8	Quad op amp	Raytheon	4136
IC9	Comparator	National	LM 311
IC10	Comparator	National	LM 311
IC11	Comparator	National	LM 311
L1	Inductor, 270 mH		
L2	Inductor, 270 mH		
L3	Inductor, 270 mH		
L4	Inductor, 270 mH		
D1	Diode, 1N4148		
D2	Diode, 1N4148		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
D3	Diode, 1N4148		
D4	Diode, 1N4148		
D5	Diode, 1N4148		
D6	Diode, 1N4148		
D7	Diode, 1N4148		
D8	Diode, 1N4148		
D9	Diode, 1N4148		
D10	Diode, 1N4148		
D11	Diode, 1N4148		
D12	Diode, 1N4148		
D13	Diode, 1N4148		
D14	Diode, 1N4148		
D15	Diode, 1N4148		
D16	Diode, 1N4148		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3)*(CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
D17	Diode, 1N4148		
D18	Diode, 1N4148		
D19	Diode, 1N4148		
D20	Diode, 1N4148		
D21	Diode, 1N4148		
D22	Diode, 1N4148		
D23	Diode, 1N4148		
D24	Diode, 1N4148		
Q1	Transistor, 2N2222		
Q2	Transistor, 2N2222		
Q3	Transistor, 2N2222		
Q4	Transistor, 2N2222		
Q5	Transistor, 2N2222		
Q6	Transistor, 2N2222		

*Schematic Diagram — Figure 2-9.

TABLE 6-4. PARTS LIST - AGC AMPLIFIER BOARD (PCB 1,2,3,)* (CONCLUDED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
Q7	Transistor, 2N2222		
Q8	Transistor, 2N2222		
J1	Input connector to Agc amplifier board		

*Schematic Diagram — Figure 2-9.

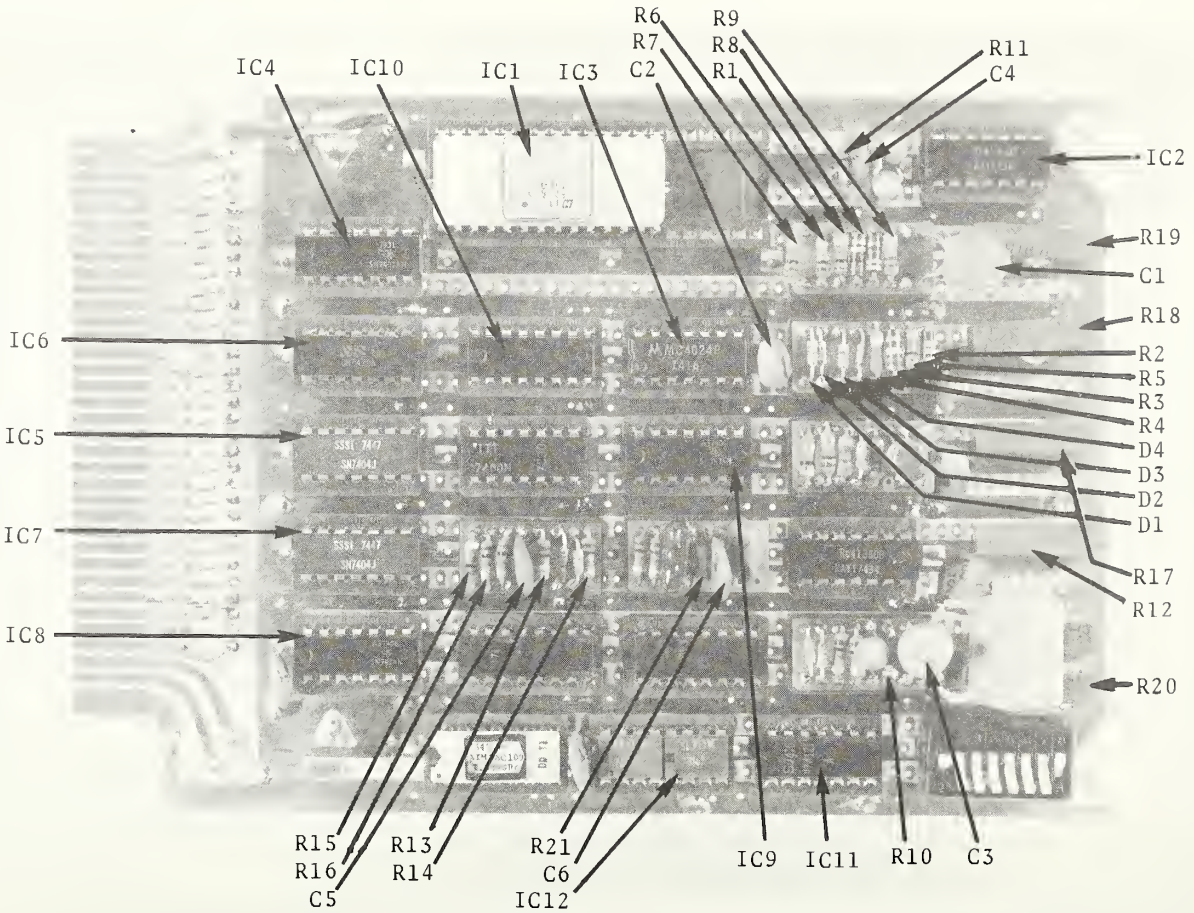


Figure 6-5. Display Driver (PCB 4), Parts Location

TABLE 6-5. PARTS LIST - DISPLAY DRIVER (PCB 4)*

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R1	Resistor, 1K ohms		
R2	Resistor, 24K ohms		
R3	Resistor, 12K ohms		
R4	Resistor, 6.2K ohms		
R5	Resistor, 1K ohms		
R6	Resistor, 1K ohms		
R7	Resistor, 1K ohms		
R8	Resistor, 20K ohms		
R9	Resistor, 11K ohms		
R10	Resistor, 510 ohms		
R11	Resistor, 10K ohms		
R12	Potentiometer, 10K ohms		
R13	Resistor, 10K ohms		
R14	Resistor, 1K ohms		

*Schematic Diagram – Figure 2-10.

TABLE 6-5. PARTS LIST - DISPLAY DRIVER (PCB 4)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R15	Resistor, 10K ohms		
R16	Resistor, 1K ohms		
R17	Potentiometer, 20K ohms		
R18	Potentiometer, 10K ohms		
R19	Potentiometer, 5K ohms		
R20	Potentiometer, 1K ohms		
R21	Resistor, 22K ohms		
C1	Capacitor, 0.047µF/25V		
C2	Capacitor, 10µF/35V		
C3	Capacitor, 33µF/25V		
C4	Capacitor, 0.01µF/25V		
C5	Capacitor, 0.1µF/10V		
C6	Capacitor, 0.1µF/10V		
D1	Diode, 1N4148		

*Schematic Diagram – Figure 2-10.

TABLE 6-5. PARTS LIST - DISPLAY DRIVER (PCB 4)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
D2	Diode, 1N4148		
D3	Diode, 1N4148		
D4	Diode, 1N4148		
IC1	Analog multiplexer	Harris Semiconductor	Model 506A
IC2	Quad op amp	Raytheon	4136
IC3	Dual multivibrator	Motorola	MC4024
IC4	Hex open collector buffer	Texas Instruments	SN7407
IC5	Hex inverter	Texas Instruments	SN7404
IC6	Dual 4-input NAND gate	Texas Instruments	SN7420
IC7	Same as IC5		
IC8	Dual D-type flip-flop	Texas Instruments	SN7474
IC9	Same as IC8		
IC10	Synchronous binary counter 4-bit	Texas Instruments	SN74161

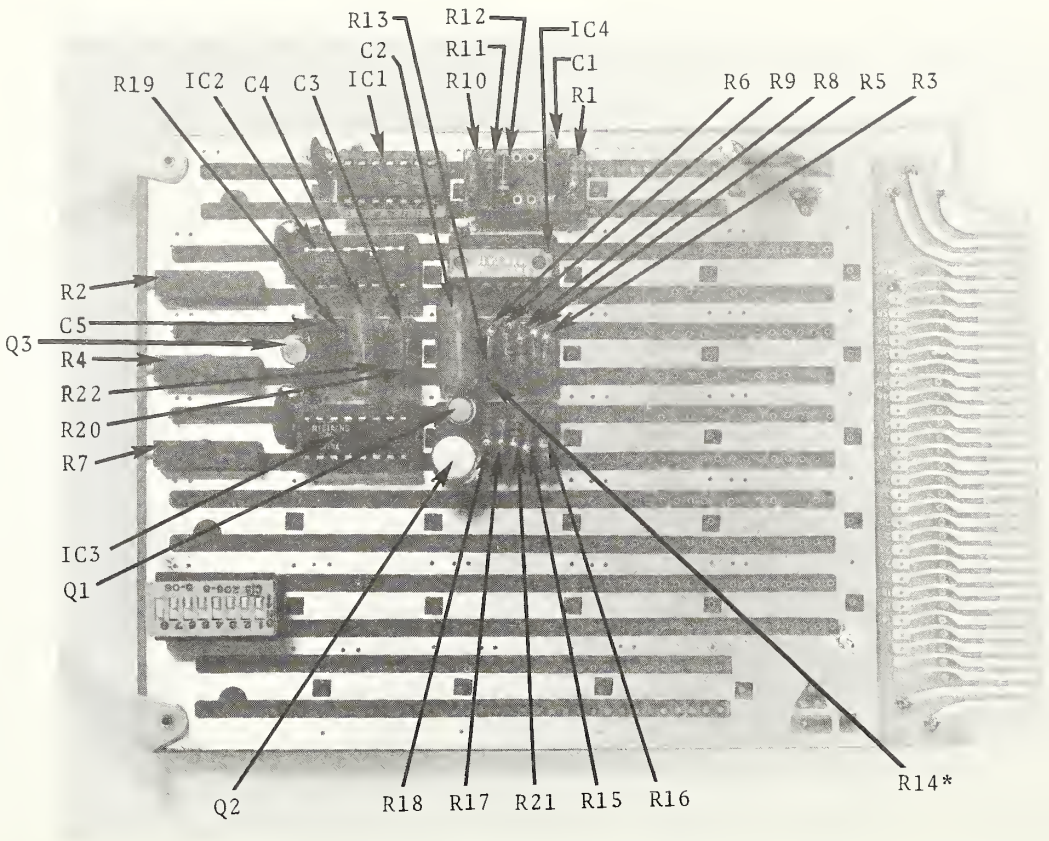
*Schematic Diagram — Figure 2-10.

TABLE 6-5. PARTS LIST - DISPLAY DRIVER (PCB 4)* (CONCLUDED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
IC11	Monostable multivibrator	Texas Instruments	SN74121
IC12	Comparator	National	LM311

*Schematic Diagram – Figure 2-10.

Figure 6-6 and Table 6-6 follow.



*R14 located under C2

Figure 6-6. Timing Logic Board (PCB 5), Parts Location

TABLE 6-6. PARTS LIST - TIMING LOGIC BOARD (PCB 5)*

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R1	Resistor, 33K ohms		
R2	Trimmer, 50K ohms		
R3	Resistor, 5.1K ohms		
R4	Trimmer, 50K ohms		
R5	Resistor, 5.1K ohms		
R6	Resistor, 100K ohms		
R7	Trimmer, 50K ohms		
R8	Resistor, 5.1K ohms		
R9	Resistor, 150 ohms		
R10	Resistor, 330 ohms		
R11	Resistor, 220 ohms		
R12	Resistor, 510 ohms		
R13	Resistor, 150 ohms		
R14	Resistor, 1K ohms		

*Schematic Diagram – Figure 2-12.

TABLE 6-6. PARTS LIST - TIMING LOGIC BOARD (PCB 5)* (CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R15	Resistor, 2.7K ohms		
R16	Resistor, 1K ohms		
R17	Resistor, 3.3K ohms		
R18	Resistor, 1K ohms		
R19	Resistor, 510 ohms		
R20	Resistor, 1K ohms		
R21	Resistor, 200 ohms		
R22	Resistor, 22 ohms		
C1	Capacitor, 0.1µF/10V		
C2	Capacitor, 0.033µF/100V		
C3	Capacitor, 0.1µF/25V		
C4	Capacitor, 0.033µF/100V		
C5	Capacitor, 0.1µF/10V		
S1	Switch, SPST, PC type		

*Schematic Diagram – Figure 2-12.

TABLE 6-6. PARTS LIST - TIMING LOGIC BOARD (PCB 5)* (CONCLUDED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
IC1	Monostable multivibrator	Texas Instruments	SN74121
IC2	Dual monostable multivibrator	Texas Instruments	SN74123
IC3	Same as IC2		
IC4	Hex inverter, open collector	Texas Instruments	SN7406
Q1	Transistor, 2N2907A		
Q2	Transistor, 2N2219		
Q3	Transistor, 2N2907A		

*Schematic Diagram — Figure 2-12.

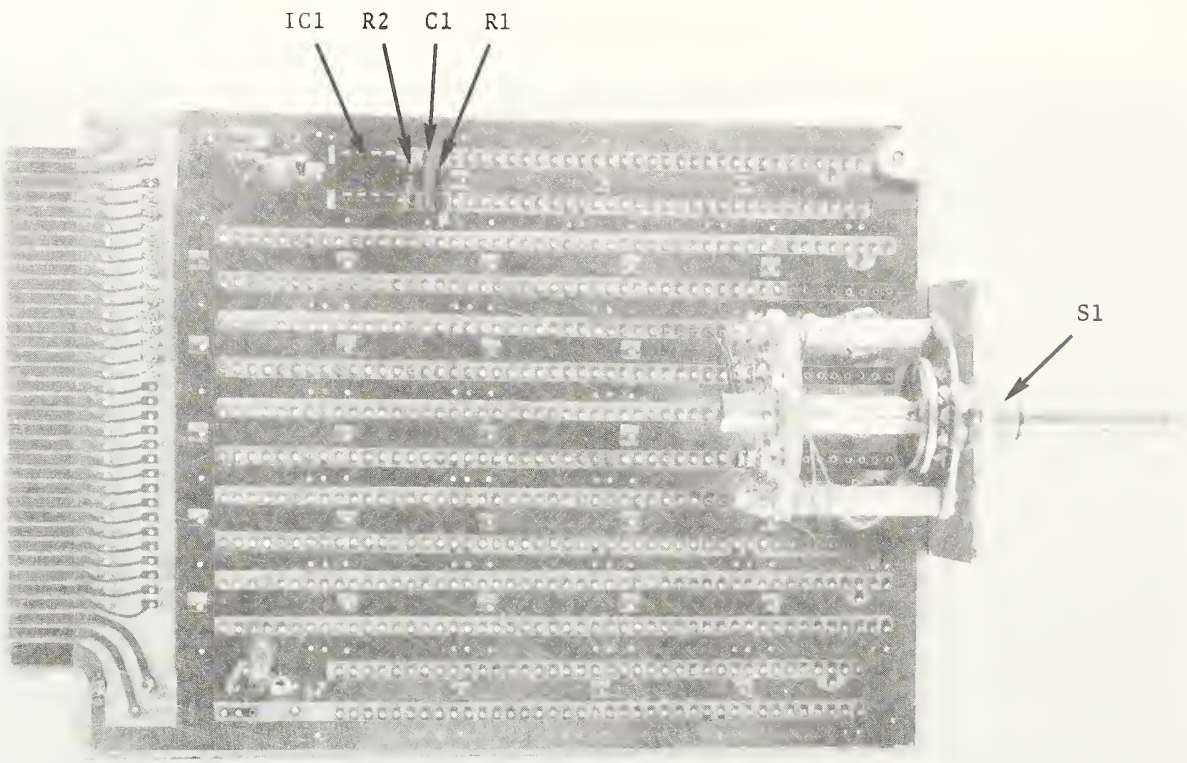


Figure 6-7. Monitor Channel Select Board (PCB 6), Parts Location

TABLE 6-7. PARTS LIST - MONITOR CHANNEL SELECT BOARD (PCB 6)*

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R1	Resistor, 51K ohms		
R2	Resistor, 51 ohms		
C1	Capacitor, 0.1μF/50V		
IC1	Buffer amplifier	National	LM310N
S1	Switch, single-pole,	Centralab	
	12-position		

*Schematic Diagram — Figure 2-13.

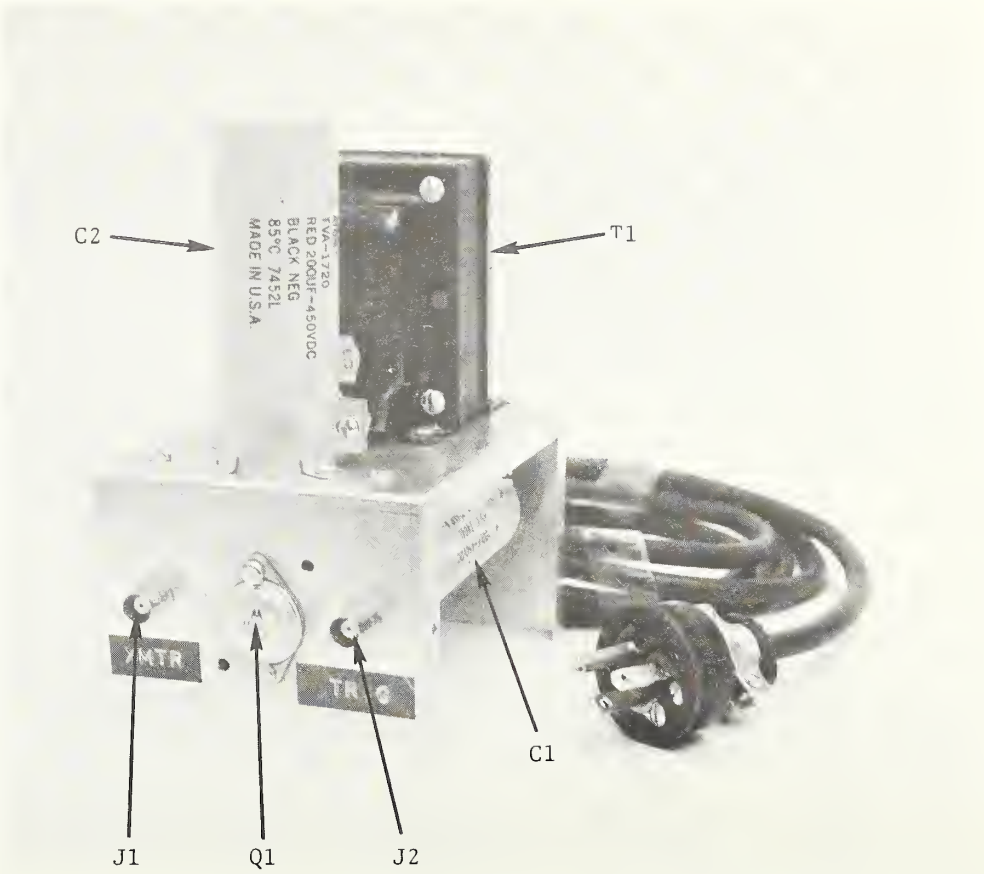


Figure 6-8a. Transmitter (Top View), Parts Location

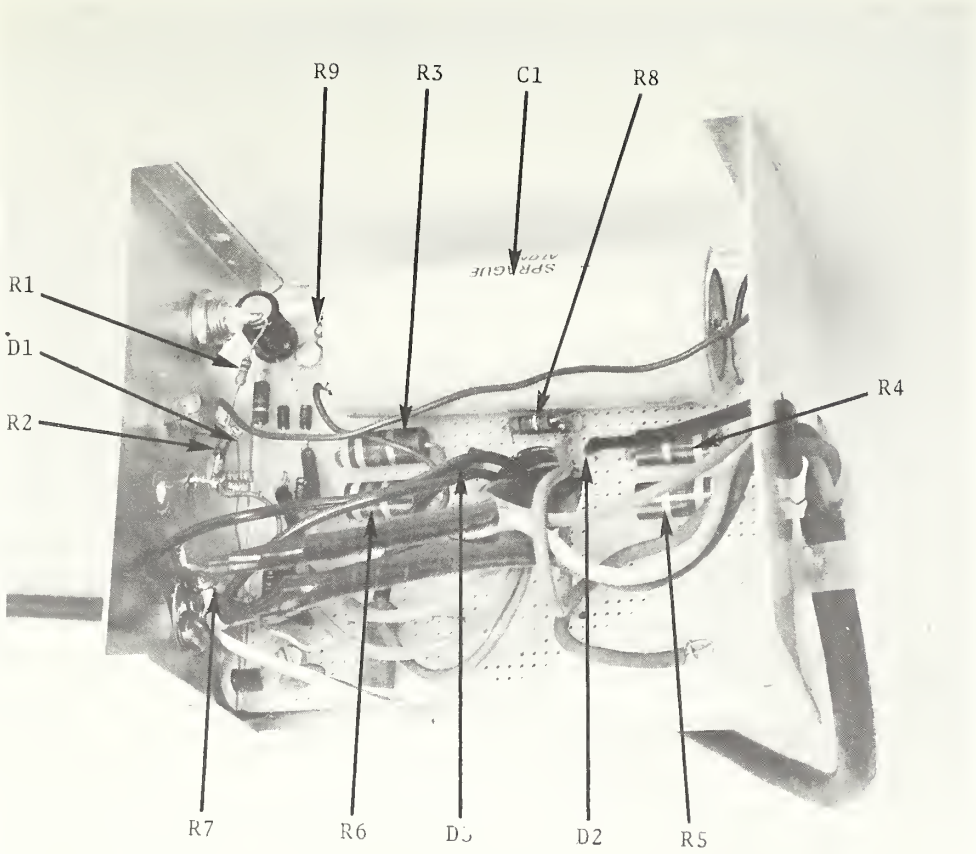


Figure 6-8b. Transmitter (Bottom View), Parts Location

TABLE 6-8. PARTS LIST - TRANSMITTER*

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R1	Resistor, 100 ohms		
R2	Resistor, 510 ohms		
R3	Resistor, 3.3K ohms, 2 watts		
R4	Resistor, 3.3K ohms, 2 watts		
R5	Resistor, 3.3K ohms, 2 watts		
R6	Resistor, 3.3K ohms, 2 watts		
R7	Resistor, 200K ohms		
R8	Resistor, 100 ohms		
R9	Resistor, 10 ohms		
Q1	Transistor	Motorola	MJ413
T1	Transformer:Primary, 120VAC		
	Secondary, 600V C.T.		
C1	Capacitor, 100μF/450V		
C2	Capacitor, 200μF/450V		

*Schematic Diagram – Figure 2-8.

TABLE 6-8. PARTS LIST - TRANSMITTER*(CONTINUED)

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
D1	Diode, 1N4335		
D2	Diode, 1N4006		
D3	Diode, 1N4006		
J1	Connector, BNC		
J2	Connector, BNC		

*Schematic Diagram — Figure 2-8.

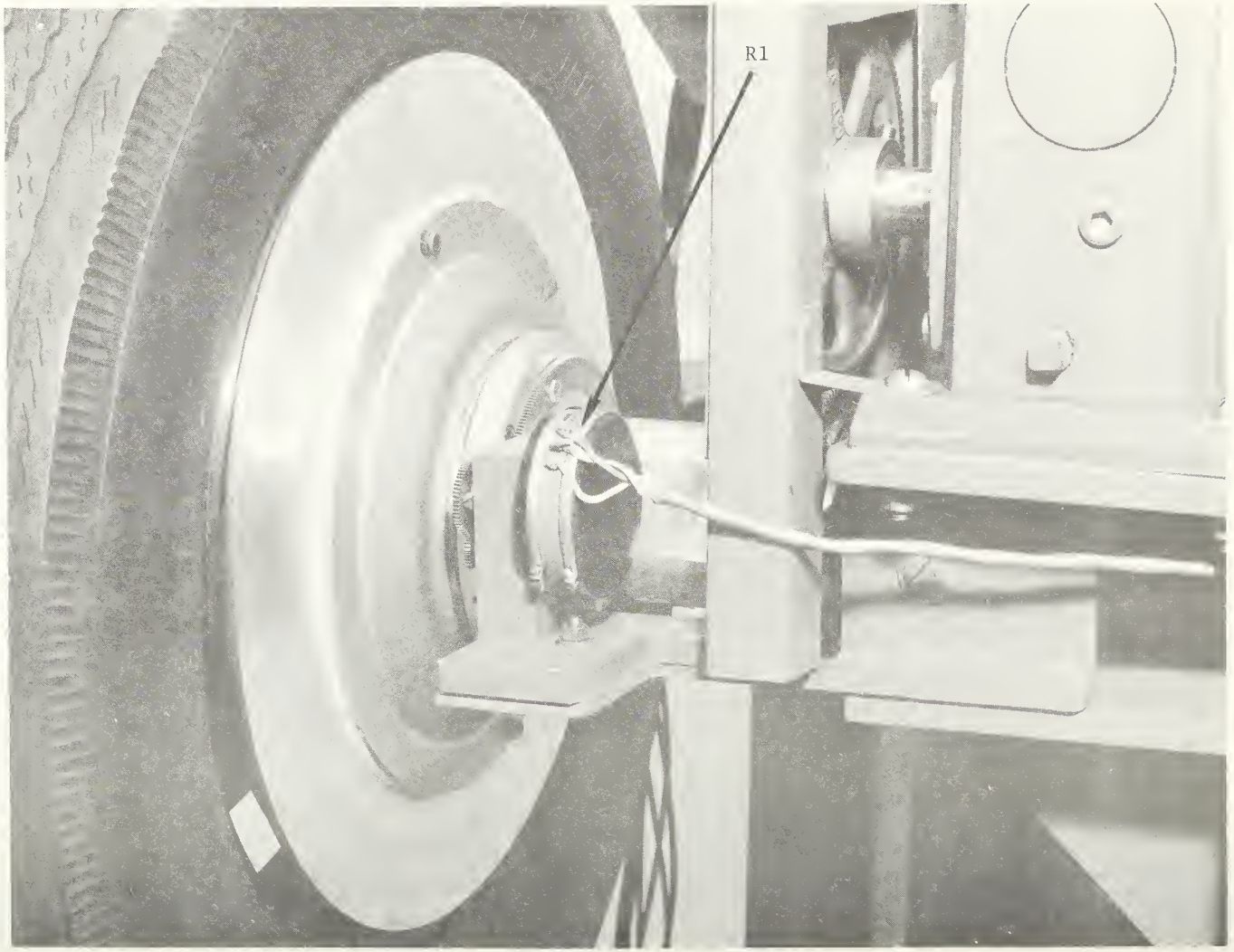


Figure 6-9. Tire Assembly, Part Location

TABLE 6-9. PART LIST - TIRE ASSEMBLY

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
R1	Potentiometer, sweep, 1K ohms	Samarius, Inc.	Type 5714

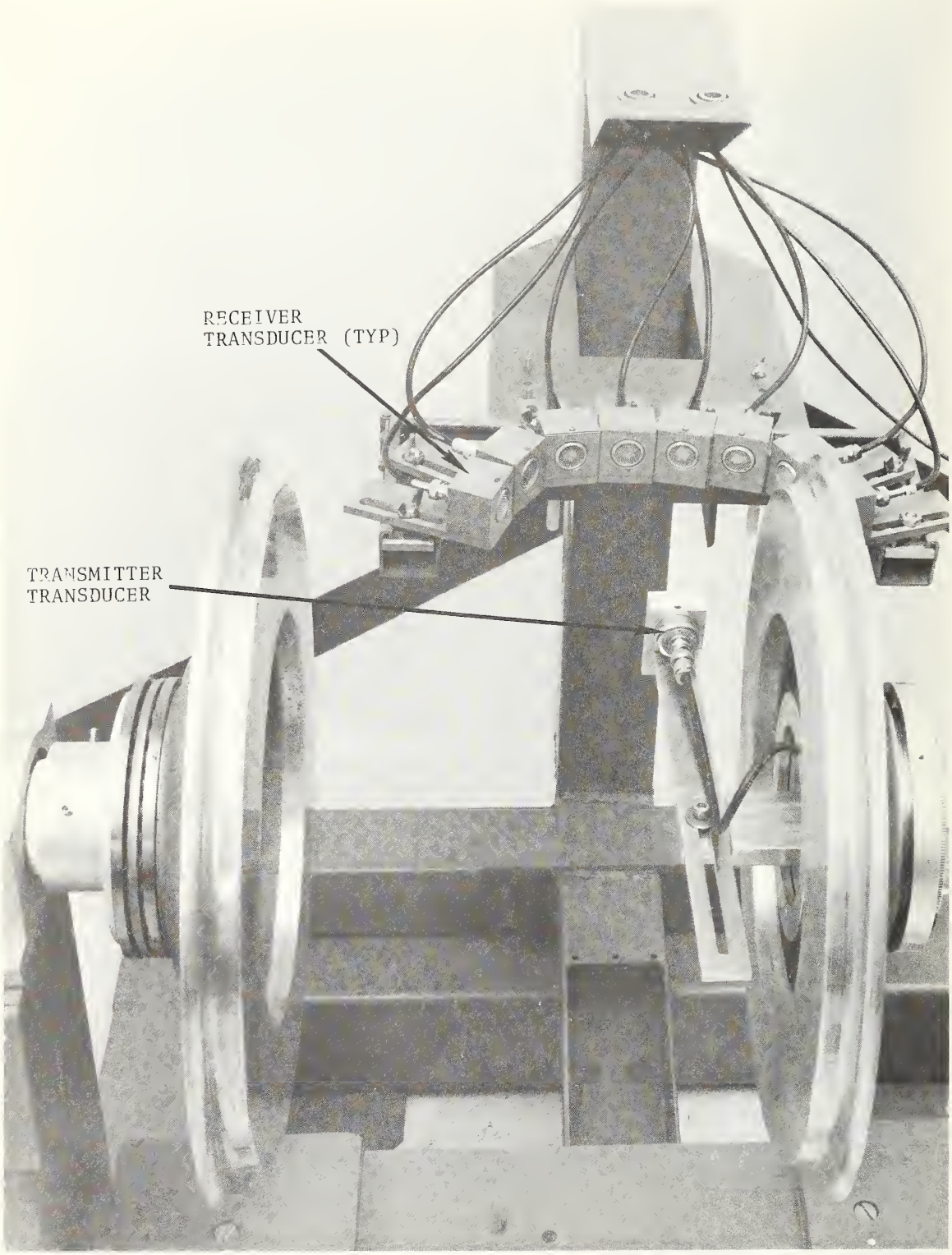


Figure 6-10. Transducers, Parts Location

TABLE 6-10. PARTS LIST - TRANSDUCERS

Reference Designation	Description	Manufacturer	Manufacturer's Type/Part No.
	Transducer, receiver	Vernitron	Color Code - Yellow
	Transducer, transmitter	Automation Industries, Inc.	Type SSA,25.0 kHz